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U1.1 S32K344
                                                                                                                                                           PTA0/GPIO[0]/EMIOS\_0\_CH[17]\_Y/LCU0\_OUT4/FXIO\_D2/EMIOS\_1\_CH[0]\_X/LPSPI0\_PCS7/TRGMUX\_OUT3/LPUART0\_CTS/EIRQ[0]/ADC0\_S8/CMP1\_IN0
                                                                                                                                                           PTA1/GPIO[1]/EMIOS_0_CH[9]_H/LPUART0_RTS/FXIO_D3/LCU0_OUT5/LPSPI0_PCS6/TRGMUX_OUT0/EIRQ[1]/ADC0_S9/CMP1_IN1/WKPU[5]
                                                                                     PTA
                                                                                                                                                          PTA2/GPIO[2]/FCCU_ERR0/EMIOS_1_CH[19]_Y/FXIO_D4/LCU0_OUT3/FCCU_ERR_IN0/LPSPI1_SIN/LPUART0_RX/EIRQ[2]/ADC1_X[0]/WKPU[0]/CMP1_IN2 PTA3/GPIO[3]/FCCU_ERR1/EMIOS_1_CH[20]_Y/LPSPI1_SCK/LCU0_OUT2/FXIO_D5/LPUART0_TX/FCCU_ERR_IN1/EIRQ[3]/ADC1_S17
                                                                                    PTA3
                                              JTAG TMS PTA
                                                                                                                                                           PTA4/GPIO[4]/FXIO_D6/CMP0_OUT/JTAG_TMS/SWD_DIO/EIRQ[4]/ADC1_S15
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                                                                   RST_PTA5
                                                                                                                                                           PTA5/GPIO[5]/RESET_B/EIRQ[5]
                                                                                    PTA6
                                                                                                                                                           PTA6/GPI0[6]/LPSPI1_PCS1/EMIOS_1_CH[13]_H/FXI0_D19/LPSPI3_PCS1/CAN0_RX/LPUART1_CTS/LPUART3_RX/EIRQ[6]/WKPU[15]/ADC0_S18
                                                                                                                                          100
                                                                                    PTA7
                                                                                                                                                           PTA7/GPIO[7]/LPUART3\_TX/LPSPI0\_PCS1/EMIOS\_1\_CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]\_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1\_RTS/FXIO\_D9/EIRQ[7]/ADC0\_S11-CH[11]_H/CAN0\_TX/LPUART1_RTS/FXIO\_D9/EIRQ[7]/ADC0\_TX/LPUART1_RTS/FXIO\_D9/EIRQ[7]/ADC0\_TX/LPUART1_RTS/FXIO\_D9/EIRQ[7]/ADC0\_TX/LPUART1_RTS/FXIO\_D9/EIRQ[7]/ADC0\_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUART1_TX/LPUAR
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PTA11/GPIO[11]/CAN1_TX/EMIOS_0_CH[13]_H/EMIOS_1_CH[1]_H/FXIO_D1/CMP0_RRT/LPSPI1_PCS0/EIRQ[19]/ADC1_S10
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155
                                                                                  PTA1
                                                                                                                                                           PTA12/GPIO[12]/LPSPI1\_PCS5/EMIOS\_0\_CH[14]\_H/CLKOUT\_STANDBY/FXIO\_D9/EMIOS\_1\_CH[2]\_H/CMP1\_OUT/CAN1\_RX/EIRQ[20]/ADC1\_POPICAL ADDITIONAL ADDITION
                                                                                 PTA1
                                                                                                                                                          PTA13/GPIO[13]/LPSPI1_PCS4/EMIOS_0_CH[15]_H/FXIO_D8/EMIOS_1_CH[3]_H/EIRQ[21]/WKPU[4]/ADC1_P1 PTA14/GPIO[14]/EMIOS_1_CH[4]_H/LPSPI1_PCS3/FXIO_D14/EIRQ[22]/ADC1_P4
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PTA19/GPIO[19]/EMIOS_1_CH[1]_H/LPSPI1_SCK/LPUART1_RX/EIRQ[1]/TRGMUX_IN13
PTA20/GPIO[20]/EMIOS_1_CH[2]_H/LPSPI1_SIN/EIRQ[2]/TRGMUX_IN14/WKPU[59]
                                                                                PTA1
                                                                                 PTA1
                                                                                 PTA2
                                                                                 PTA21
                                                                                                                                                          PTA21/GPIO[21]/LPSPI2_PCS2/EMIOS_1_CH[3]_H/FXIO_D0/LPSPI1_PCS0/EIRQ[3]/TRGMUX_IN15 PTA24/GPI[24]/EMIOS_1_CH[7]_H/FXIO_D3/OSC32K_XTAL
                                                                                PTA24
                                                                                                                                                           PTA25/GPI[25]/EMIOS_1_CH[8]_X/FXIO_D2/EIRQ[5]/OSC32K_EXTAL/WKPU[34]
                                                                                PTA25
                                          PTA27/VDD DCDC
                                                                                                                                                          PTA27/GPIO[27]/FXIO\_D5/EMIOS\_1\_CH[10]\_H/EMAC\_PPS1/LPUART0\_TX/CAN0\_TX\\ PTA28/GPIO[28]/EMIOS\_1\_CH[11]\_H/LPSPI1\_SCK/CAN0\_RX/LPUART0\_RX/EIRQ[6]\\
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                                                                                 PTA29
                                                                                                                                                           PTA29/GPIO[29]/EMIOS_1_CH[12]_H/EMAC_PPS2/LPUART2_TX/LPSPI1_SIN
                                                                                                                                                           PTA30/GPIO[30]/EMIOS_1_CH[13]_H/LPSPI1_SOUT/LPSPI0_SOUT/LPUART2_RX/EIRQ[7]/WKPU[37]
                                                                                                                                                           PTA31/GPIO[31]/EMIOS_1_CH[14]_H/FXIO_D0/LPSPI0_PCS1/TRGMUX_OUT8
                                                                                                                                                      S32K344_172HDQFP
                                                                                                                                                                                                                                                                                                                           U1.2 S32K344
                                                                         PTB0/GPIO[32]/LPI2C0\_SDAS/FXIO\_D14/LPSPI0\_PCS0/EMIOS\_0\_CH[3]\_G/LCU1\_OUT5/EMIOS\_1\_CH[6]\_H/HSE\_TAMPER\_LOOP\_OUT0/CAN0\_RX/LPUART0\_RX/EIRQ[8]/ADC1\_S14/ADC0\_S14/WKPU[7]\\ PTB1/GPIO[33]/LPI2C0\_SCLS/LPUART0\_TX/LPSPI0\_SOUT/EMIOS\_0\_CH[7]\_G/CAN0\_TX/EMIOS\_1\_CH[5]\_H/LCU1\_OUT4/HSE\_TAMPER\_EXTIN0/EIRQ[9]/ADC1\_S15/ADC0\_S15\\ PTB2/GPIO[34]/ADC1\_MA[0]/EMIOS\_0\_CH[8]\_X/LPSPI2\_SIN/LCU1\_OUT3/SAI0\_D0/FXIO\_D18/EIRQ[10]/TRGMUX\_IN3/WKPU[8]
                                                           74
   PTB:
                                                                          PTB3/GPIO[35]/EMIOS\_0\_CH[9]\_H/LPSPI2\_SOUT/ADC0\_MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_OUT2/FXIO\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/LCU1\_D17/SAI0\_MCLK/EIRQ[11]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX\_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN2-MA[0]/TRGMUX_IN
   PTB
                                                                         PTB4/GPIO[36]/EMAC_MII_RMII_TXD[1]/EMIOS_0_CH[4]_G/LPSPI0_SOUT/EMAC_MII_RMII_MDIO/EMIOS_1_CH[10]_H/EIRQ[12]/TRGMUX_IN1
PTB5/GPIO[37]/EMAC_MII_RMII_TXD[0]/EMIOS_0_CH[5]_G/LPSPI0_PCS1/LPSPI0_PCS0/CLKOUT_RUN/EMIOS_1_CH[11]_H/EMAC_MII_RMII_MDC/EIRQ[13]/TRGMUX_IN0
PTB8/GPIO[40]/EMIOS_1_CH[15]_H/LCU0_OUT11/LPSPI0_PCS5/FXIO_D29/EIRQ[14]/ADC0_X[0]/WKPU[25]
PTB9/GPIO[40]/EMIOS_1_CH[16]_X/LCU0_OUT10/FXIO_D28/EIRQ[15]/ADC0_X[1]/WKPU[17]
PTB1/GPIO[40]/EMIOS_1_CH[16]_X/LCU0_OUT10/FXIO_D28/EIRQ[15]/ADC0_X[1]/WKPU[17]
   PTB:
   PTB
                                                         130
  PTB
                                                        129
126
PTB1
                                                                          PTB10/GPIO[42]/EMIOS_1_CH[17]_Y/LCU0_OUT9/FXIO_D27/EIRQ[24]/ADC0_X[2]
                                                                         PTB11/GPIO[43]/EMIOS_1_CH[17]_1/I/COU_OUT8/FXIO_D2//EIRQ[24]/ADCU_X[2]
PTB11/GPIO[43]/EMIOS_1_CH[18]_Y/LCU0_OUT8/FXIO_D26/LPI2C0_HREQ/EIRQ[25]/ADC0_X[3]/WKPU[16]
PTB12/GPIO[44]/LPSPI3_PCS3/EMIOS_0_CH[0]_X/LCU0_OUT2/FXIO_D25/EIRQ[26]/ADC1_X[1]/WKPU[12]
PTB13/GPIO[45]/LPSPI3_PCS2/EMIOS_0_CH[1]_G/FXIO_D8/LCU0_OUT3/FXIO_D24/EIRQ[27]/ADC0_S8/ADC1_S8/WKPU[11]
PTB14/GPIO[46]/EMIOS_0_CH[2]_G/LPSPI1_SCK/LCU0_OUT7/FXIO_D23/EIRQ[28]/ADC0_S9/ADC1_S9
PTB15/GPIO[47]/EMIOS_0_CH[3]_G/LPSPI1_SIN/FXIO_D22/EIRQ[29]/ADC1_S11/WKPU[33]
PTB1
                                                         117
PTB<sub>1</sub>
                                                         116
PTB<sub>1</sub>
                                                         114
PTB1
                                                        113
PTB<sub>1</sub>
                                                        112
110
PTB1
                                                                          PTB1
                                                                          PTB17/GPIO[49]/EMIOS_0_CH[5]_G/LPSPI1_PCS3/EMIOS_1_CH[7]_H/LPSPI3_PCS0/FXIO_D20/EIRQ[31]/ADC1_X[2]/WKPU[14] PTB18/GPIO[50]/EMIOS_1_CH[15]_H/FXIO_D1/LPSPI1_PCS1/TRGMUX_OUT9
                                                           42
PTB1
                                                           43
PTB1
                                                                          PTB19/GPIO[51]/EMIOS_1_CH[15]_H/FXIO_D2/TRGMUX_OUT10/WKPU[38]
                                                           44
PTB20
                                                                          PTB20/GPIO[52]/EMIOS_1_CH[16]_X/FXIO_D3/TRGMUX_OUT11
PTB21/GPIO[53]/EMIOS_1_CH[17]_Y/FXIO_D4/TRGMUX_OUT12/EIRQ[8]/WKPU[39]
                                                           45
PTB2
                                                                         PTB22/GPI0[54]/CAN1_TX/EMIOS_1_CH[18]_Y/LPSPI3_PCS1/LPUART1_TX/FXIO_D15/TRGMUX_OUT13/EMAC_MII_CRS/EIRQ[9]
PTB23/GPI0[55]/ADC1_MA[0]/EMIOS_1_CH[19]_Y/FXIO_D4/TRGMUX_OUT14/CAN1_RX/EMAC_MII_COL/LPUART1_RX/EIRQ[10]/WKPU[40]
PTB24/GPI0[56]/ADC1_MA[1]/EMIOS_1_CH[20]_Y/FXIO_D5/EIRQ[11]
PTB25/GPI0[57]/EMIOS_1_CH[21]_Y/FXIO_D6/LPSPI2_PCS0/EIRQ[12]
PTB25/GPI0[57]/EMIOS_1_CH[21]_Y/FXIO_D6/LPSPI2_PCS0/EIRQ[12]
PTB2
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PTB23
                                                           70
PTB24
PTB2
PTB2
                                                                          PTB26/GPIO[58]/EMIOS_1_CH[22]_X/FXIO_D7/EIRQ[13]/WKPU[41]
PTB2
                                                                          PTB27/GPIO[59]/EMIOS_1_CH[23]_X/FXIO_D8/LPSPI2_SOUT
PTB2
                                                                          PTB28/GPIO[60]/ADC1_MA[2]/FXIO_D9/LPSPI2_SIN/LCU1_OUT11/EMAC_PPS3/EIRQ[14]/WKPU[42]
PTB29
                                                                          PTB29/GPIO[61]/FXIO\_D10/LPSPI2\_SCK/LCU1\_OUT10/SAI0\_D1
                                                                     S32K344_172HDQFP
                                                                                                                                                                                                                                                                                                                                                                                                                  TITLE:
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