							C0	S0 S1 S2 S3		MDR_MEM/BUS	A寄存器选择	B寄存器选择	\WR	\RD			CP选择	HALT	后继微地址形成
指令	合并的微指令	微指令文字描述	地址	控存内容	23	22	21	20 | 19	18 | 17	16	15 | 14	13 | 12	11	10	9 | 8	7	6 | 5 | 4	3	2 | 1 | 0
取指令	00000000	PC->A, A->ALU->MAR	00	324061	0	0	1	10	01	0	01,A选PC	00	0	0			110	0	001, μPC+1
	00000001	M(MAR)->MDR	01	000451	0	0	0	00	00	0,内存到MDR	00	00	0	1			101	0	001, μPC+1
	00000010	PC+1->PC	02	000031	0	0	0	00	00	0	00	00	0	0			011	0	001, μPC+1
	00000011	MDR->ALU->IR	03	321041	0	0	1	10	01	0	00	01,B选MDR	0	0			100	0	001, μPC+1
	00000100	XJP	04	000004	0	0	0	00	00	0	00	00	0	0			000	0	100,按XJP寻址
	00000101		05	000000															
	00000110		06	000000															
	00000111		07	000000															
	00001000		08	000000															
	00001001		09	000000															
	00001010		0A	000000															
	00001011		0B	000000															
	00001100		0C	000000															
	00001101		0D	000000															
	00001110		0E	000000															
	00001111		0F	000000															
	00010000		10	000000															
	00010001		11	000000															
	00010010		12	000000															
	00010011		13	000000															
	00010100		14	000000															
	00010101		15	000000															
	00010110		16	000000															
	00010111		17	000000															
	00011000		18	000000															
	00011001		19	000000															
	00011010		1A	000000															
	00011011		1B	000000															
	00011100		1C	000000															
	00011101		1D	000000															
	00011110		1E	000000															
	00011111		1F	000000															
LOAD	00100000	MDR->ALU->ACC	20	321411	0	0	1	10	01	0	00	01,B选MDR	0	1			001	0	001, μPC+1
	00100001	JP无条件转移	21	000002	0	0	0	00	00	0	00	00	0	0			000	0	010, 无条件转移
	00100010		22	000000															
	00100011		23	000000															
	00100100		24	000000															
	00100101		25	000000															
	00100110		26	000000															
	00100111		27	000000															
	00101000		28	000000															
	00101001		29	000000															
	00101010		2A	000000															
	00101011		2B	000000															
	00101100		2C	000000															
	00101101		2D	000000															
	00101110		2E	000000															
	00101111		2F	000000															
STORE	00110000	ACC->ALU->MDR->M(MAR)	30	338851	0	0	1	10	01	1,MDR到内存	10, A选ACC	00	1	0			101	0	001, μPC+1
	00110001	JP无条件转移	31	000002	0	0	0	00	00	0	00	00	0	0			000	0	010, 无条件转移
	00110010		32	000000															
	00110011		33	000000															
	00110100		34	000000															
	00110101		35	000000															
	00110110		36	000000															
	00110111		37	000000															
	00111000		38	000000															
	00111010		3A	000000															
	00111011		3B	000000															
	00111100		3C	000000															
	00111101		3D	000000															
	00111110		3E	000000															
	00111111		3F	000000															
ADD	01000000	MDR+ACC->ACC	40	329011	0	0	1	10	01	0	10,A选ACC	01, B选MDR	0	0			001	0	001, μPC+1
	01000001	JP无条件转移	41	000002	0	0	0	00	00	0	00	00	0	0			000	0	010, 无条件转移
	01000010		42	000000															
	01000011		43	000000															

	01000100		44	000451	0	0	0	00	00	0,内存到MDR	00	00	0	1			101	0	001，μPC+1
	01000101		45	329011	0	0	1	10	01	0	10,A选ACC	01，B选MDR	0	0			001	0	001，μPC+1
	01000110		46	000002	0	0	0	00	00	0	00	00	0	0			000	0	010，无条件转移
	01000111		47	000000															
	01001000		48	000451	0	0	0	00	00	0,内存到MDR	00	00	0	1			101	0	001，μPC+1
	01001001		49	329011	0	0	1	10	01	0	10，A选ACC	01,B选MDR	0	0			001	0	001，μPC+1
	01001010		4A	000002	0	0	0	00	00	0	00	00	0	0			000	0	010，无条件转移
	01001011		4B	000000															
	01001100		4C	000451	0	0	0	00	00	0，内存到MDR	00	00	0	1			101	0	001，μPC+1
	01001101		4D	329011	0	0	1	10	01	0	10，A选ACC	01，B选MDR	0	0			001	0	001，μPC+1
	01001110		4E	000002	0	0	0	00	00	0	00	00	0	0			000	0	010，无条件转移
	01001111		4F	000000															
MOVIN	01010000	MDR->ALU->ACC	50	321411	0	0	1	10	01	0	00	01，B选MDR	0	1			001	0	001，μPC+1
	01010001	JP无条件转移	51	000002	0	0	0	00	00	0	00	00	0	0			000	0	010，无条件转移
	01010010		52	000000															
	01010011		53	000000															
	01010100		54	000000															
	01010101		55	000000															
	01010110		56	000000															
	01010111		57	000000															
	01011000		58	000000															
	01011001		59	000000															
	01011010		5A	000000															
	01011011		5B	000000															
	01011100		5C	000000															
	01011101		5D	000000															
	01011110		5E	000000															
	01011111		5F	000000															
MOVOUT	01100000	ACC->ALU->R	60	328421	0	0	1	10	01	0	10,A选ACC	00	0	1			010	0	001，μPC+1
	01100001	JP无条件转移	61	000002	0	0	0	00	00	0	00	00	0	0			000	0	010,无条件转移
	01100010		62	000000															
	01100011		63	000000															
	01100100		64	000000															
	01100101		65	000000															
	01100110		66	000000															
	01100111		67	000000															
	01101000		68	000000															
	01101001		69	000000															
	01101010		6A	000000															
	01101011		6B	000000															
	01101100		6C	000000															
	01101101		6D	000000															
	01101110		6E	000000															
	01101111		6F	000000															
PLUS	01110000	R->ALU->ACC	70	322411	0	0	1	10	01	0	00	10,B选R	0	1			001	0	001，μPC+1
	01110001	ACC->ALU+1->ACC	71	008411	0	0	0	00	00	0	10,A选ACC	00	0	1			001	0	001，μPC+1
	01110010	JP无条件转移	72	000002	0	0	0	00	00	0	00	00	0	0			000	0	010,无条件转移
	01110011		73	000000															
	01110100		74	000000															
	01110101		75	000000															
	01110110		76	000000															
	01110111		77	000000															
	01111000		78	000000															
	01111001		79	000000															
	01111010		7A	000000															
	01111011		7B	000000															
SUB	01111100	M(MAR)->MDR	7C	000451	0	0	0	00	00	0,内存到MDR	00	00	0	1			101	0	001，μPC+1
	01111101	MDR-(ACC)->ACC	7D	0C9011	0	0	0	01	10	0	10，A选ACC	01,B选MDR	0	0			001	0	001，μPC+1
	01111110	JP无条件转移	7E	000002	0	0	0	00	00	0	00	00	0	0			000	0	010,无条件转移
	10000000		80	000000															
	10000001		81	000000															
	10000010		82	000000															
	10000011		83	000000															
	10000100		84	000000															
	10000101		85	000000															
	10000110		86	000000															
	10000111		87	000000															
	10001000		88	000000															
	10001001		89	000000															

	10001010		8A	000000															
	10001011		8B	000000															
	10001100		8C	000000															
	10001101		8D	000000															
	10001110		8E	000000															
	10001111		8F	000000															
HALT	10010000	HALT	90	000009	0	0	0	00	00	0	00	00	0	0			000	1	001
	10010001		91	000000															
	10010010		92	000000															
	10010011		93	000000															
	10010100		94	000000															
	10010101		95	000000															
	10010110		96	000000															
	10010111		97	000000															
	10011000		98	000000															
	10011001		99	000000															
	10011010		9A	000000															
	10011011		9B	000000															
	10011100		9C	000000															
	10011101		9D	000000															
	10011110		9E	000000															
	10011111		9F	000000															
00，存储器直接寻址	10100000	R->ALU->MDR	A0	332451	0	0	1	10	01	1	00	10,B选R	0	1			101	0	001，μPC+1
	10100001	QJP	A1	000003	0	0	0	00	00	0	00	00	0	0			000	0	011，按QJP寻址
	10100010		A2	000000															
	10100011		A3	000000															
	10100100		A4	000000															
	10100101		A5	000000															
	10100110		A6	000000															
	10100111		A7	000000															
01， 存储器直接寻址	10101000	PC->A，A->ALU->MAR	A8	324461	0	0	1	10	01	0	01,A选PC	00	0	1			110	0	001，μPC+1
	10101001	M(MAR)->MDR	A9	000451	0	0	0	00	00	0,内存到MDR	00	00	0	1			101	0	001，μPC+1
	10101010	MDR->ALU->MAR	AA	321061	0	0	1	10	01	0	00	01,B选MDR	0	0			110	0	001，μPC+1
	10101011	PC+1->PC	AB	000031	0	0	0	00	00	0	00	00	0	0			011	0	001，μPC+1
	10101100	M(MAR)->MDR	AC	000451	0	0	0	00	00	0,内存到MDR	00	00	0	1			101	0	001，μPC+1
	10101101	QJP	AD	000003	0	0	0	00	00	0	00	00	0	0			000	0	011，按QJP寻址
	10101110		AE	000000															
	10101111		AF	000000															
10 立即寻址	10110000	PC->A，A->ALU->MAR	B0	324461	0	0	1	10	01	0	01,A选PC	00	0	1			110	0	001，μPC+1
	10110001	PC+1->PC	B1	000031	0	0	0	00	00	0	00	00	0	0			011	0	001，μPC+1
	10110010	M(MAR)->MDR	B2	000451	0	0	0	00	00	0,内存到MDR	00	00	0	1			101	0	001，μPC+1
	10110011	QJP	B3	000003	0	0	0	00	00	0	00	00	0	0			000	0	011，按QJP寻址
	10110100		B4	000000															
	10110101		B5	000000															
	10110110		B6	000000															
	10110111		B7	000000															
11 寄存器间接寻址	10111000	R->ALU->MAR	B8	322461	0	0	1	10	01	0	00	10，B选R	0	1			110	0	001，μPC+1
	10111001	M(MAR)->MDR	B9	000451	0	0	0	00	00	0,内存到MDR	00	00	0	1			101	0	001，μPC+1
	10111010	QJP	BA	000003	0	0	0	00	00	0	00	00	0	0			000	0	011，按QJP寻址
	10111011		BB	000000															
	10111100		BC	000000															
	10111101		BD	000000															
	10111110		BE	000000															
	10111111		BF	000000															
JMP	11000000	PC->A，A->ALU->MAR	C0	324461	0	0	1	10	01	0	01，A选PC	00	0	1			110	0	001，μPC+1
	11000001	M(MAR)->MDR	C1	000451	0	0	0	00	00	0,内存到MDR	00	00	0	1			101	0	001，μPC+1
	11000010	MJP	C2	321035	0	0	1	10	01	0	00	01,B选MDR	0	0			011	0	101
	11000011	JP无条件转移	C3	000002	0	0	0	00	00	0	00	00	0	0			000	0	010,无条件转移