

EXTI GPIO Interrupt Map

- 0 - SWITCH2
- 1 - USB_PD_INT
- 2 - EXT_I2C1_INT
- 3 - EXT_I2C2_INT
- 4
- 5-9(6) - EXT_UART_CTS
- 10-15(13) - SWITCH1

Default Peripheral Mapping

- DEBUG_UART - USART1
- EXT_UART - LPUART1
- USB_PD_I2C/EXT_I2C1 - I2C3
- EXT_I2C1 - I2C1
- EXT_LS_MP - SPI2, LPUART1

PWM outputs with alternates

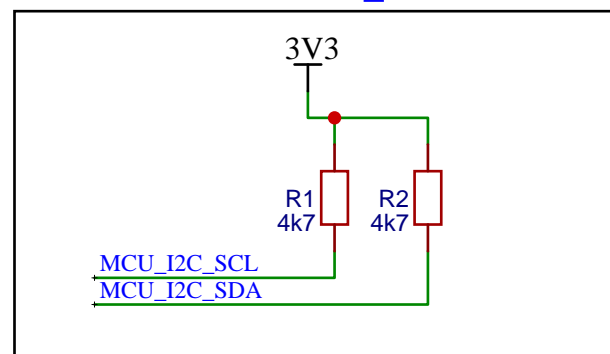
PWM outputs are provided with alternate pins to allow usage with different hardware timers. Note: Unused alternate pin must be configured as input.

- PWM_OUT_CH0: PA0
- PWM_OUT_CH1: PA1, PE1
- PWM_OUT_CH2: PA2, PE0
- PWM_OUT_CH3: PA3, PD14

EXT_LS Pins with alternate

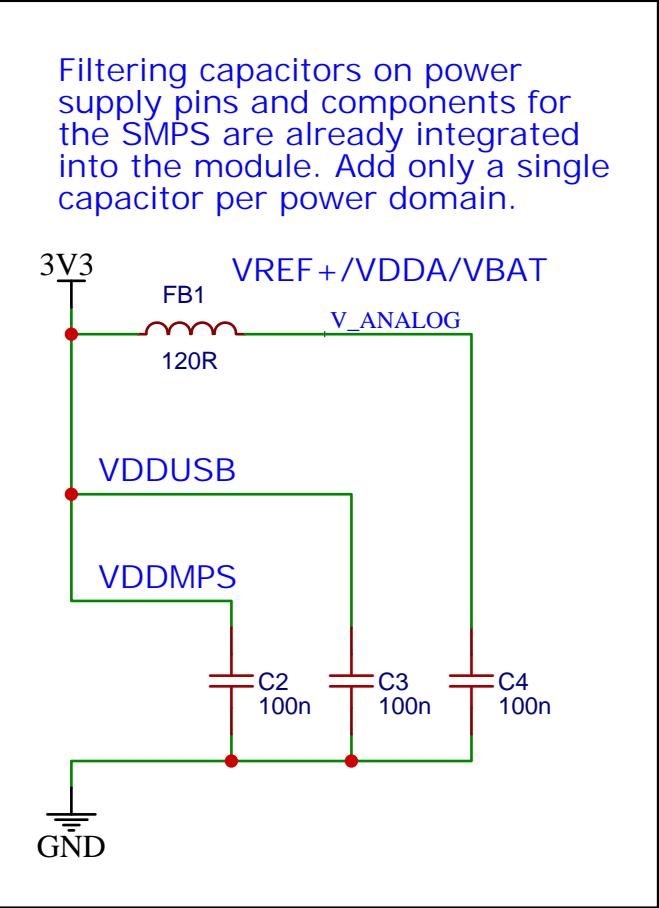
- EXT_LS_MP0: PB10
- EXT_LS_MP1: PB15, PB11

Shared I2C Pins USB_PD and I2C2

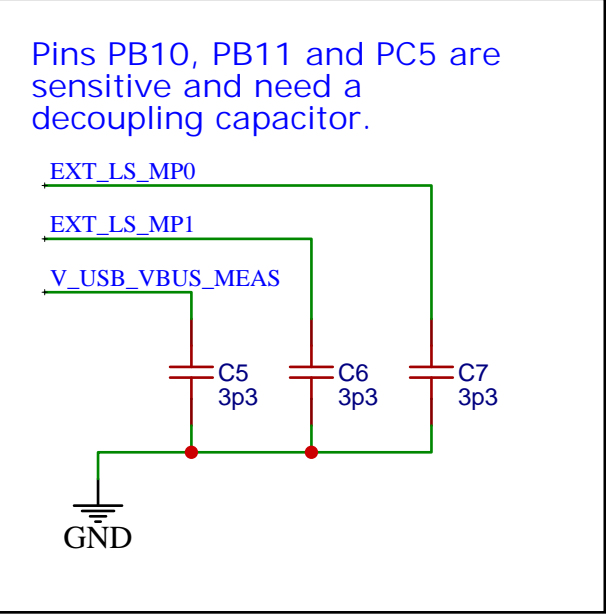


TITLE: MCU		REV: 1.0
	Company:	Sheet: 2/8
	Date:	Drawn By: raitraak

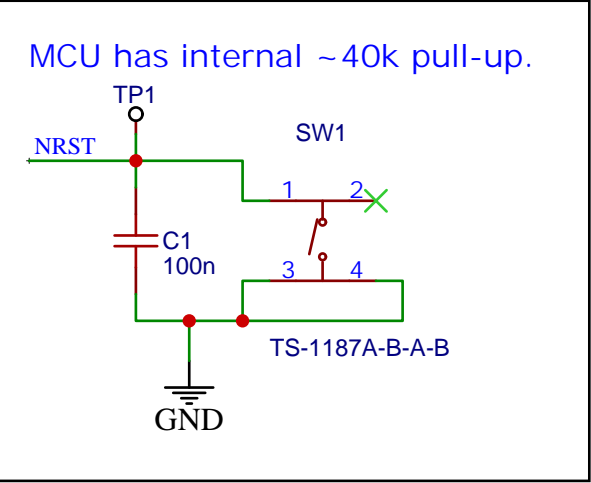
MCU Module Power



Sensitive Pin Decoupling

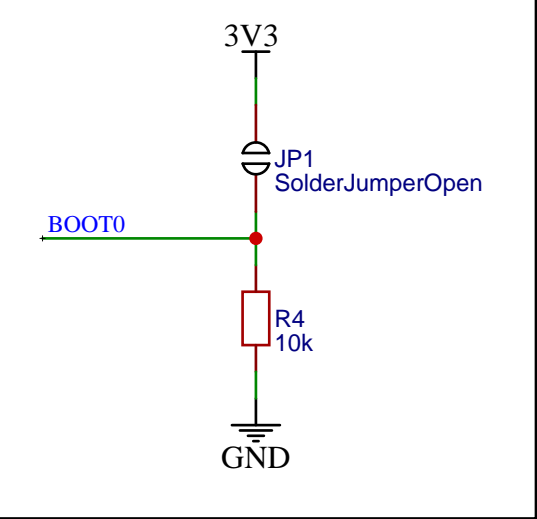


Reset Switch

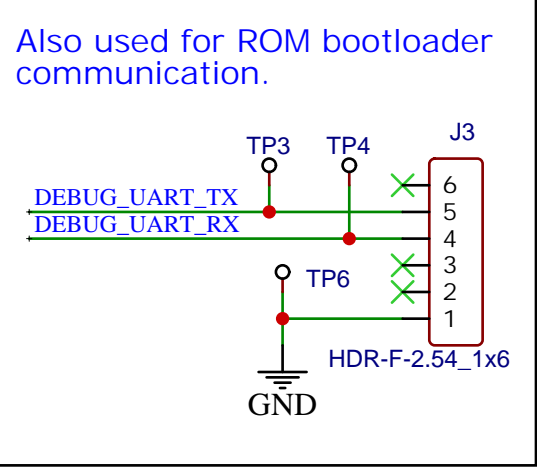


Boot Mode Select

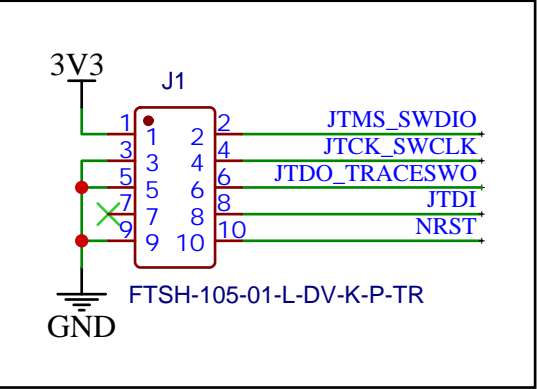
Short to enable ROM bootloader



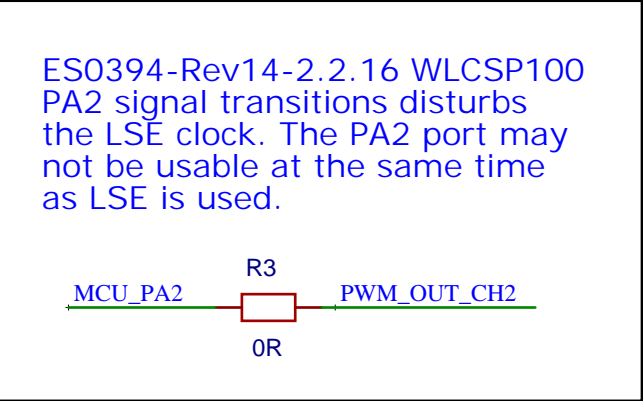
DEBUG_UART - FTDI Connector



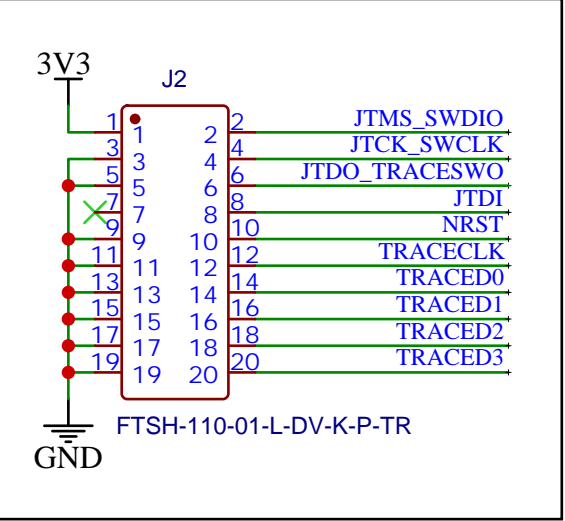
Cortex Debug connector



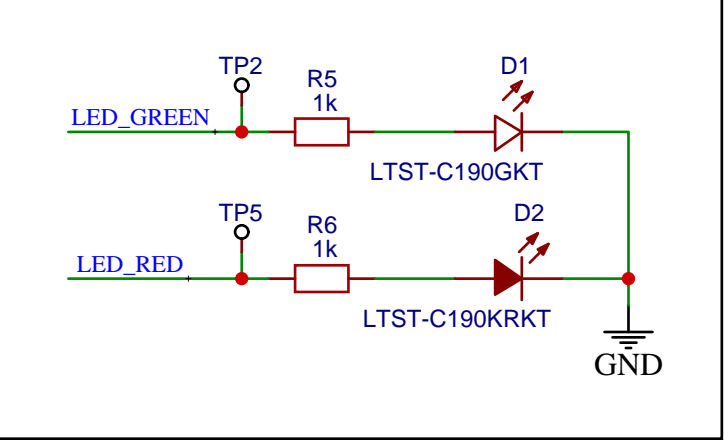
PA2 Disconnect Option



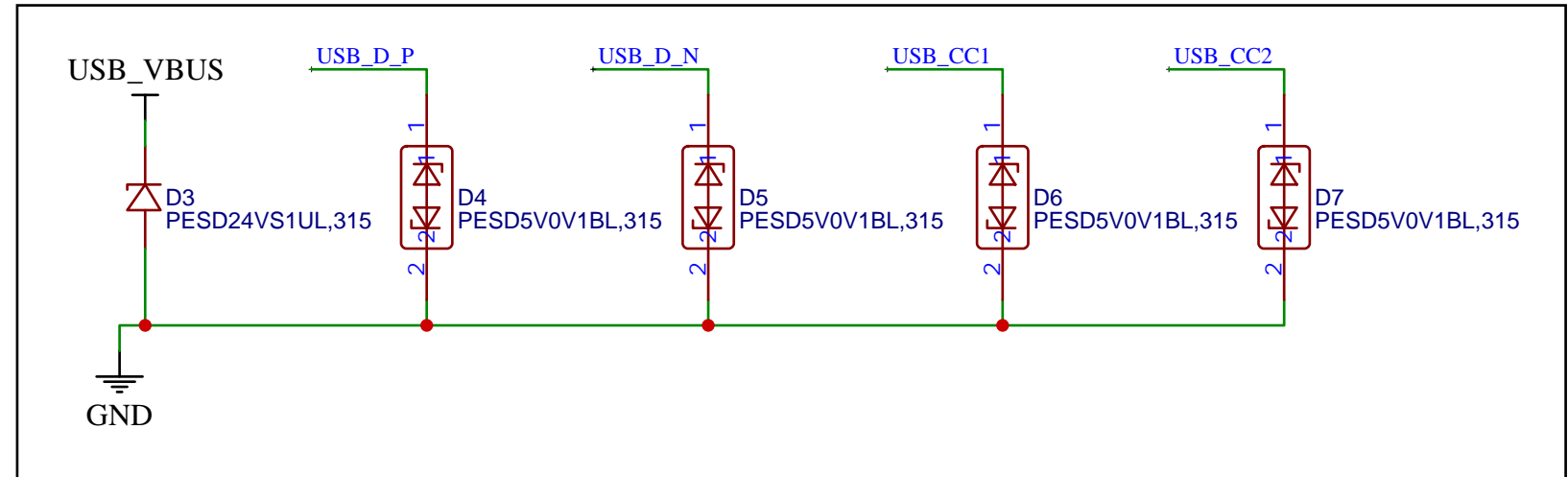
Cortex Debug+ETM connector



UI LEDs



USB ESD Protection



The schematic diagram illustrates the USB PD controller circuit (FUSB302BMPX, U2) connected to a USB Type-C port and a 3V3 supply. The USB Type-C port is connected to the controller via USB_CC1, USB_CC2, and USB_VBUS. The controller's pins are connected as follows:

- USB_CC1** and **USB_CC2** are connected to pins 14 and 13, respectively, through capacitors C11 and C12 (470pF).
- USB_VBUS** is connected to pin 1 (CC2).
- VCONN** (pins 13 and 12) is connected to USB_VBUS through a 100k resistor (R9).
- VDD** (pins 3 and 4) is connected to USB_VBUS.
- INT_N** (pin 5) is connected to the **USB_PD_INT** signal.
- SCL** (pin 6) is connected to the **MCU_I2C_SCL** signal.
- SDA** (pin 7) is connected to the **MCU_I2C_SDA** signal.
- EP** (pin 15) is connected to GND.
- GND** (pins 9 and 8) is connected to GND.

The 3V3 supply is connected to the controller's **VDD** pins (3 and 4) through a 100nF capacitor (C9) and a 1uF/10V capacitor (C10).

@20V 2.99V
@5V 0.75V
t=4.1us

USB_VBUS

TP11

R8 33k/1%

R10 4k7/1%

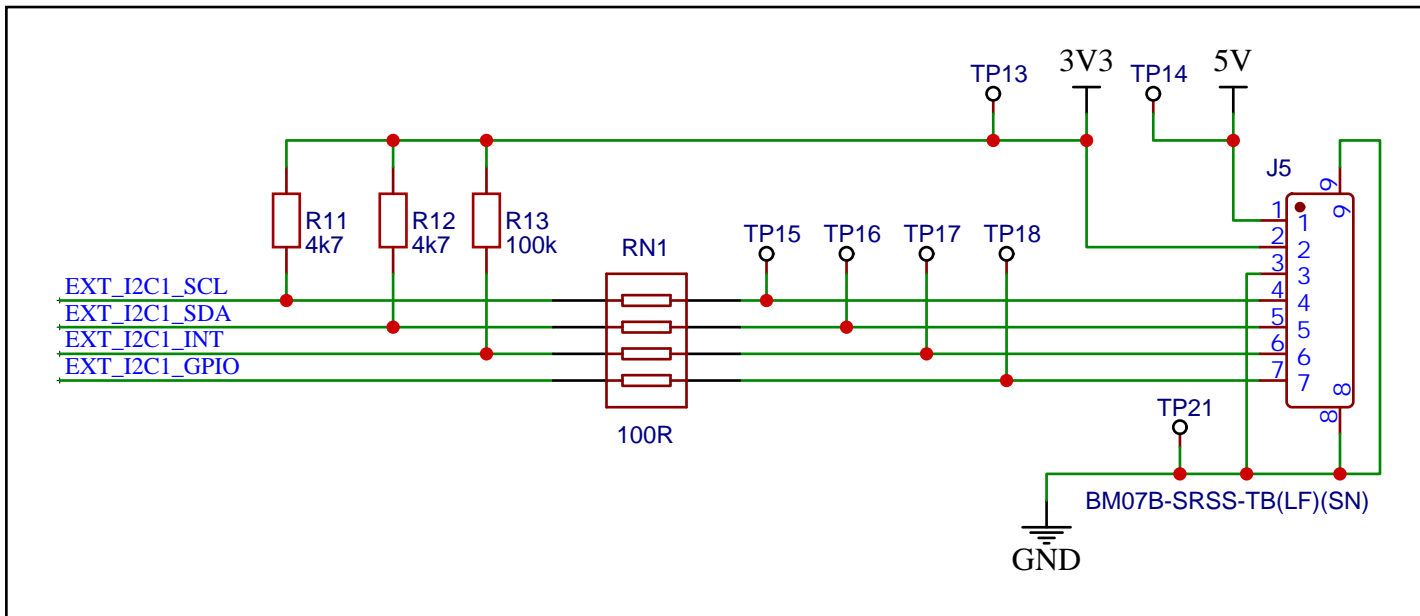
C13 1n

V_USB_VBUS_MEAS

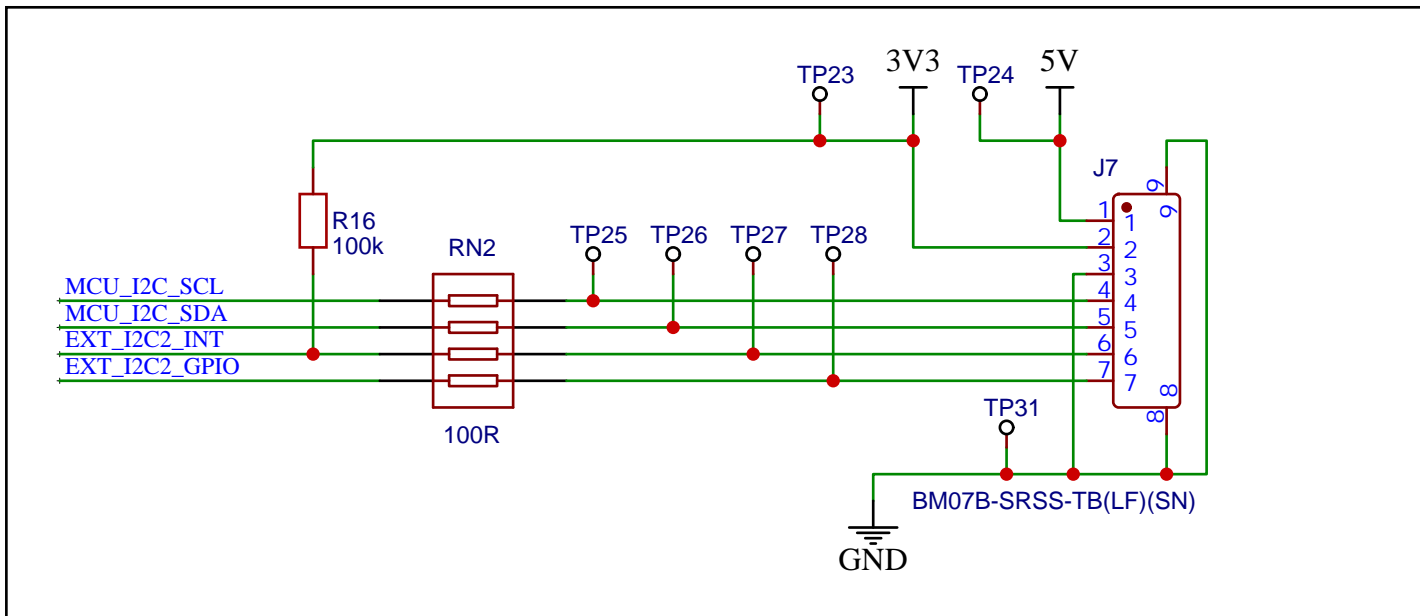
GND

TITLE: USB		REV: 1.0
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	Date: Drawn By: raitraak	

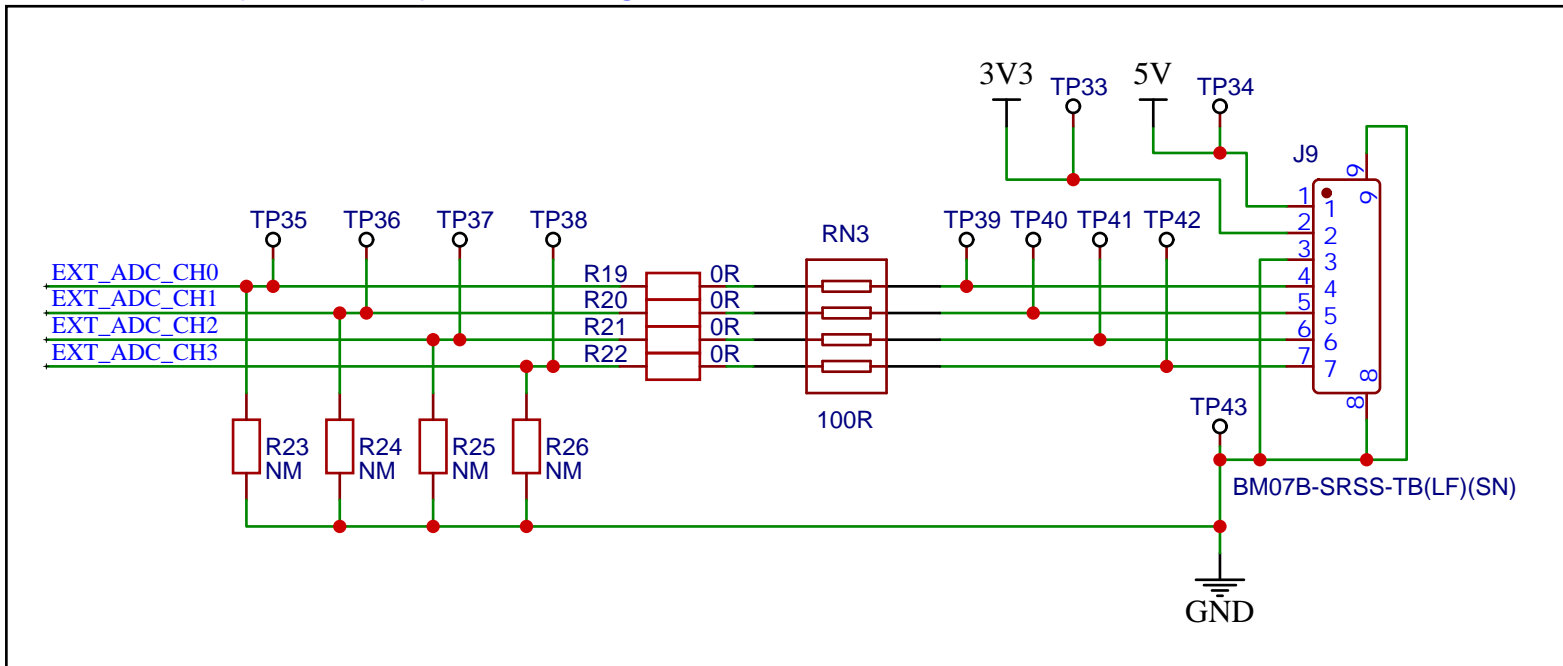
I2C1



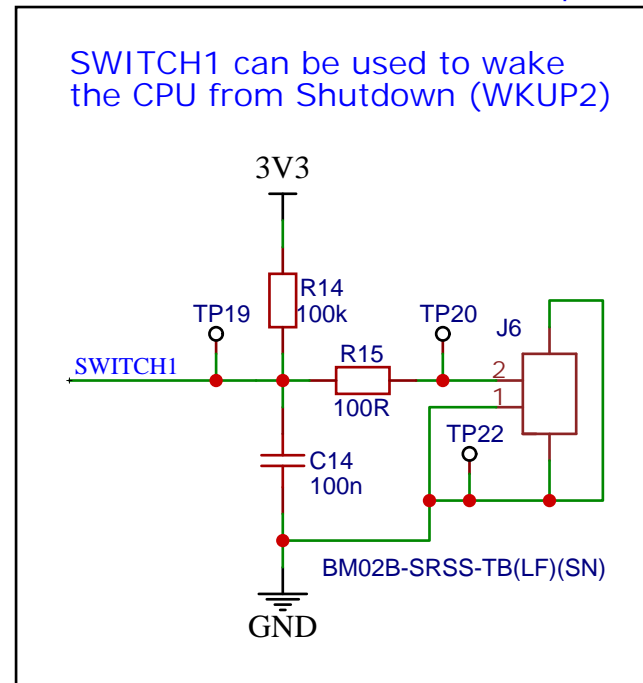
I2C2



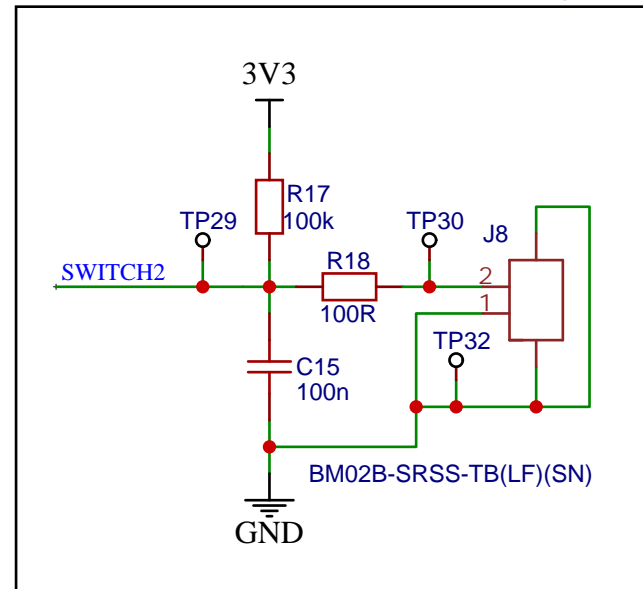
ADC - ADC Inputs with optional voltage divider



SWITCH1 - Debounced Switch Input



SWITCH2 - Debounced Switch Input

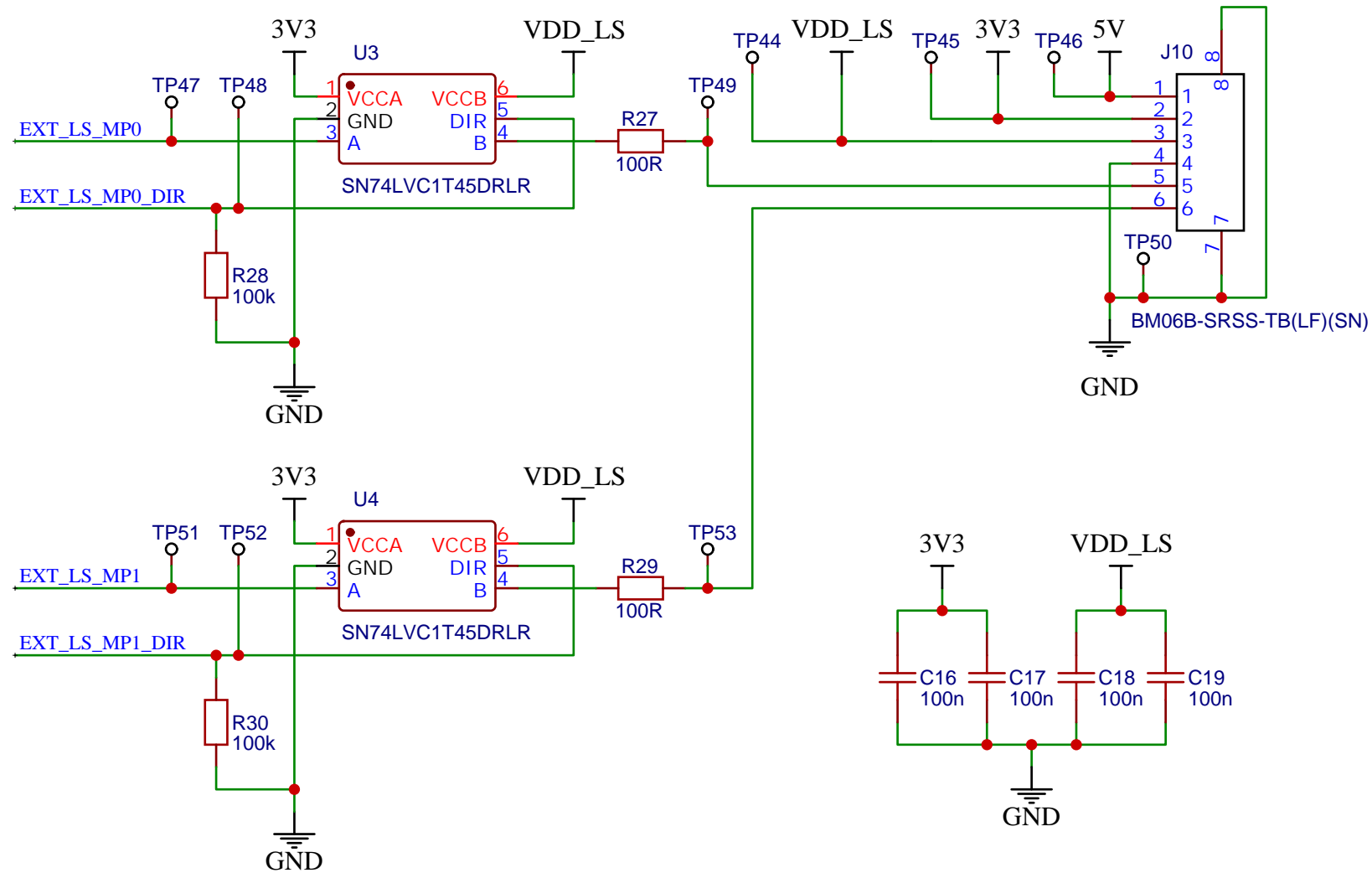


Notes:
All 7-pin extension connectors use the same supply pin layout to prevent any HW failures from connecting to the wrong header.

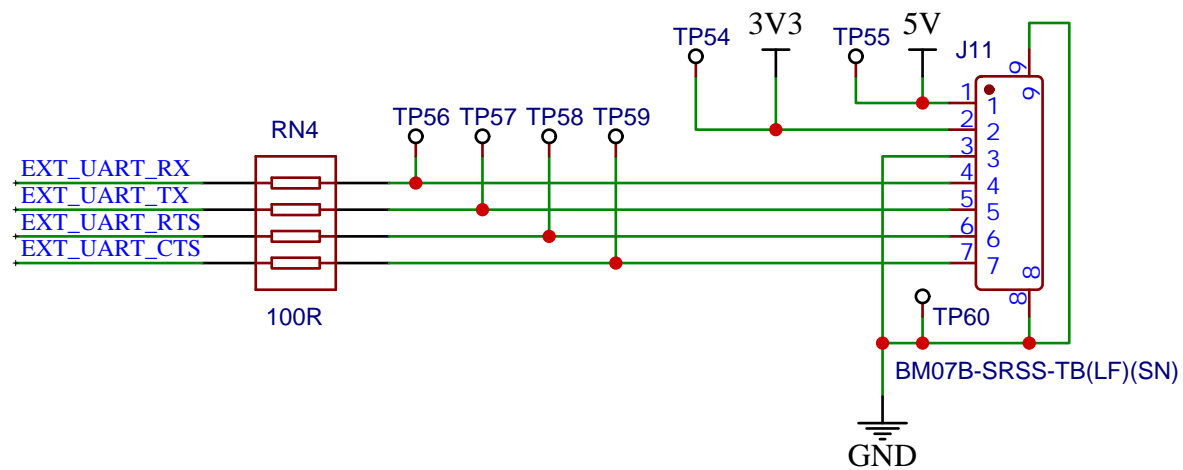
TITLE: Extension 1		REV: 1.0
Company:		Sheet: 5/8
Date:		Drawn By: raitraak

LS-MP - Level Shifted Multi Protocol IO

For flexibility the VDD_LS is provided externally. VDD_LS: 1.8-5V.
 SN74LVC1T45 has a VCC isolation feature which allows B side to be unpowered.
 Use 6-pin connector due to different supply pin layout compared to other connectors.
 Direction defaults to input.
 DIR High: Output
 DIR Low: Input



UART



TITLE: Extension 2		REV: 1.0
	Company:	Sheet: 6/8
	Date: Drawn By: raitraak	

