VLSI

Monsoon-2022 Course Project

Group Number – 12	
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A Novel XOR/XNOR Structure for Modular Design of QCA Circuits

Abstract:

In this project we try to demonstrate the functionality of XOR/XNOR gate, analyze its output and performance using graphs and manual calculation and we will also make complex circuits like Full adder circuit, 4 Parity Circuit and Comparator circuit using XOR/XNOR logic gate. Our XOR/XNOR is built using a cell level response, thus it may be thought of as a single level device.

Introduction:

To maintain the size predicted by Moore's law of the transistor nanotechnologies like Quantum cellular antenna, Carbon nanotube, Nano Magnetic logic, Resonating tunneling diodes, Spin-wave devices came into use. QCA technology dominates the CMOS technology with fast switch speed, ultra-low power consumption and high device density.

Transistors are the building blocks in the traditional circuits. In the same way QCA cells are basic units in the QCA circuits. Each cell contains two free electrons which can exchange their position within the cell. Generally, every QCA circuit uses an inverter & 3-input majority gate as its building block.

QCA Basics:

Quantum cellular automata (QCA) introduced by von Neumann refers to any one of several models of quantum computation, which have been devised in analogy to conventional models of cellular automata. It has several advantages including high device density, low power consumption and fast switch speed.

- **QCA cells** which resemble transistors in conventional circuits, are the fundamental building blocks of a QCA-based circuit. It is made up of four quantum dots that are placed one in each corner of a square structure. There are two potential grounds shown below in fig 1 states that can represent the binary states "0" and "1," respectively, with polarizations of "1" and "-1."A four stage clock method is frequently used in QCA designs to decrease signal metastability and guarantee proper signal propagation across the circuit.

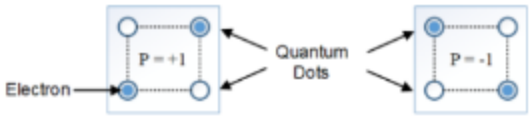


Fig-1

- **QCA wire** as shown in figure 2(b), a QCA wire is a collection of cells placed next to one another. It has four different types of clocks QCA cells.

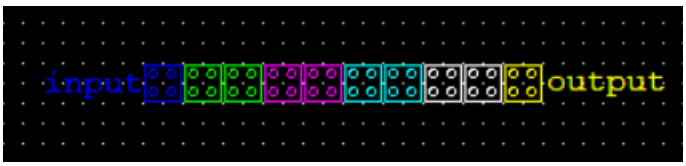


Fig-2(a)

- **Inverter and 3-input Majority -** The inverter and the majority gate are two essential components of every QCA circuit. Inverters and 3-input majority gates are the two fundamental logic gates in QCA. An inverter schematic is shown in Figure 2(b). The input signal's value can be reversed by the inverter. And Fig. 2(c) shows a schematic of the 3-input majority gate. The logic function M (P, Q, R) = PQ + PR + QR is realised by a 3-input majority gate. By setting one of the inputs to "1" or "0," respectively, it is clear from its function that it can be converted to a 2-input OR or AND gate with ease. In QCA technology, an inverter and a 3-input majority are used to accomplish all logic operations.

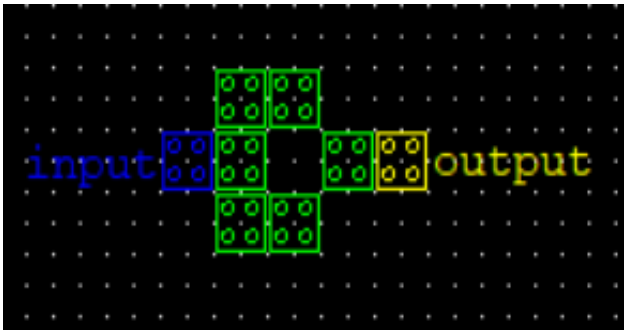


Fig-2(c)

Fig-2(d)

Software Used:

QCA Designer, QCA Designer E.

Cell level XOR/XNOR Gate:

The XOR/XNOR logic gate design presented in this project is based on a cell-level methodology (it can be regarded as a single logic device), and the intended output is achieved by the interaction of the cells.

Fig.3 shows the schematic for the proposed QCA-based XOR/XNOR gate circuit. In Fig. 3, input cells a and b, enable input cells e1 and e2, and output cell f are depicted.

The XOR/XNOR based on cell level includes 13 QCA normal cells, occupies 0.01 m2, and has a 0.25 cycle delay. The XOR operation is performed when the enable inputs (e1e2) polarization value is "-1+1."When the polarization value of the enable inputs (e1e2) is "+1-1," XNOR logic operation is carried out.

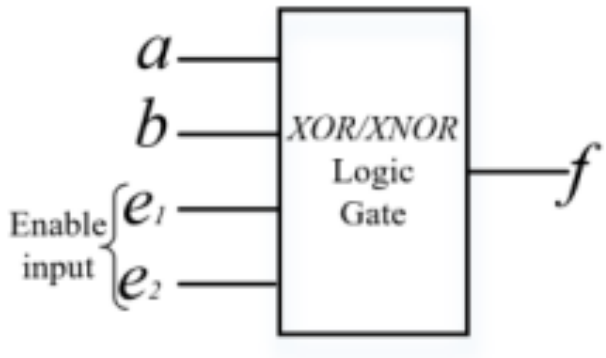
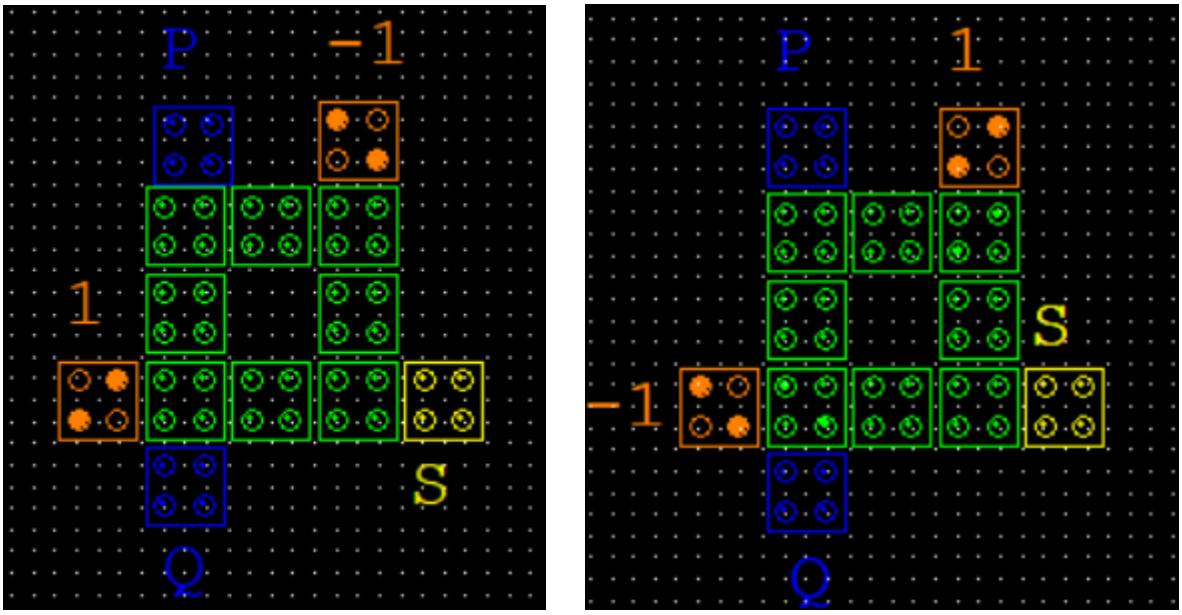


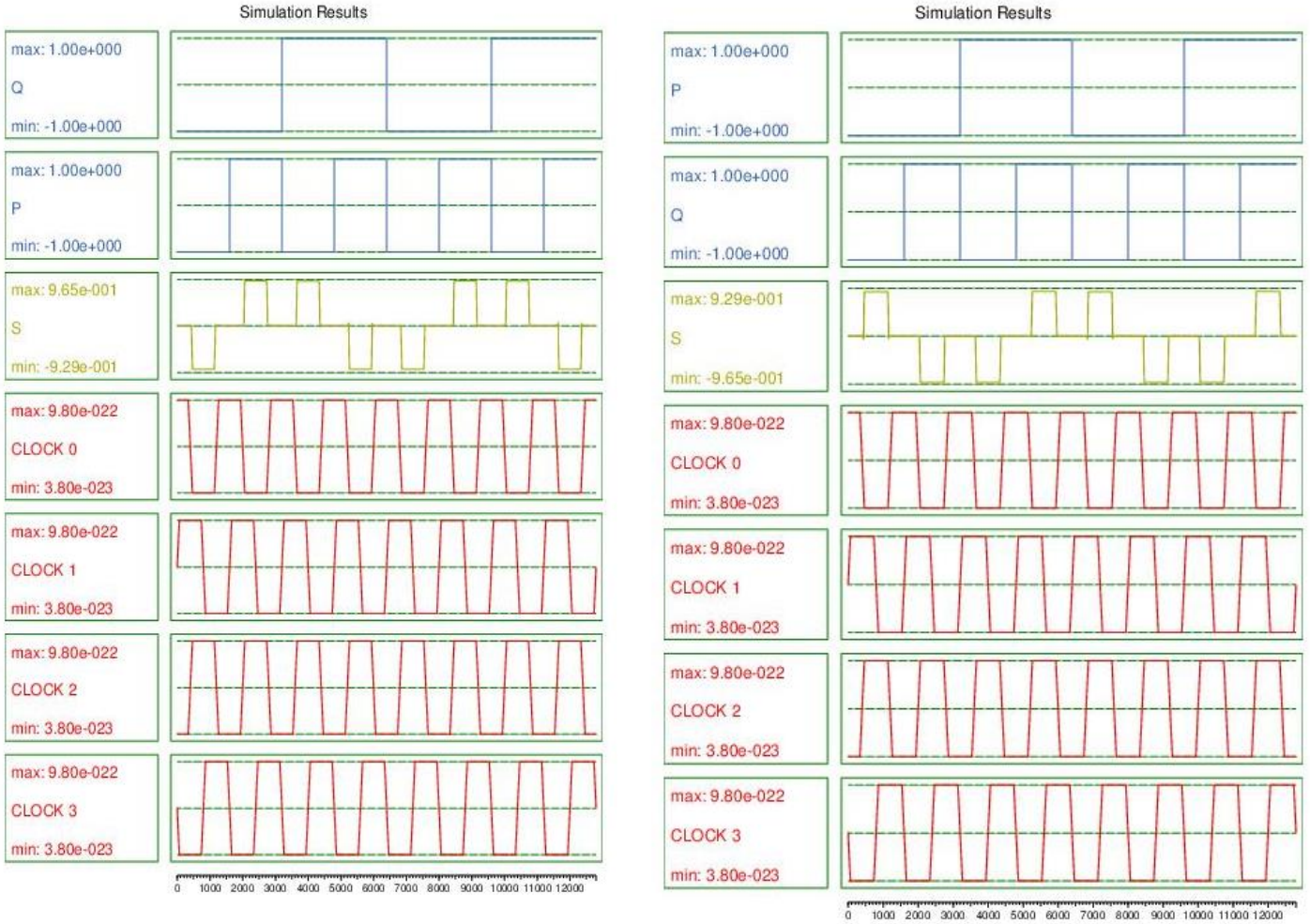
Fig-3

QCA Layout of the XOR/XNOR gate based on cell level:



Figs: Cell level XOR/XNOR gate's QCA configuration: QCA layout of XOR gate, QCA layout of XNOR gate

Simulation results of Novel XOR/XNOR gate:



Figs: Cell level XOR/XNOR gate's QCA Simulation Results.

Simulation Results:

The simulation results of the XOR/XNOR logic gate are shown in the above image. It is evident that by adjusting the values that enable inputs (i.e., e1 and e2), this structure may implement the XOR and XNOR logic functions.

The left side of the diagram displays the XOR logic function simulation results. Since the enable inputs (e1e2) are '01' in binary, it is clear from the left side of the above diagram that the output will be 0 when P= 0 and Q = 0. The result will be f = 1 when P = 0, Q = 1. As a result, all the values of output bit f are in accordance with inputs P and Q. This result confirms the theoretical XOR gate values, demonstrating the design's correctness.

The XNOR logic function simulation results are depicted in the right portion of the preceding diagram, where enable inputs (e1e2) are displayed as '10' in binary. Similarly, it can be observed that the result will be f = 1 for P = 0, Q = 0 and the result will be f = 0 for P = 0 and Q = 1. As a result, all the values of output bit f are in accordance with inputs P and Q. This result confirms the XNOR gate's theoretical values, demonstrating the design's correctness.

Physical Verification:

This part offers the physical validation of the innovative logic gate. Eight driver cells are present in the suggested design. Generous radius of effect should be considered when proving the output of the new construction using the XOR/XNOR logic gate. We assume that every other cell in this letter has an impact on the output cell in order to obtain the most accurate result. The electrostatic energies of various electrons in each cell are computed in order to determine the kink energy of any given cell while the 13th cell's state is unpolarized during the input (P, Q, e1, e2) = (1, 1, -1, 1), with only the outputs "1" and "0" being conceivable. The calculated results from the equation below are shown in Table 1. Equation below can be used to determine the electrostatic energy between two distinct electrons (first one). The equation below (second one).can be used to calculate the total electrostatic energy (UT)
The electrostatic energy (total) is given by:

$$U_{ij} = \frac{kq_i q_j}{r_{ij}}$$

$$U_T = U_{Tx} + U_{Ty} = \sum_{i=1}^{n} U_{ix} + \sum_{i=1}^{n} U_{iy}$$

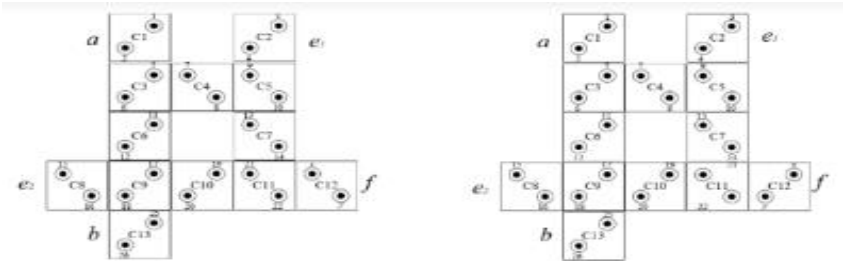


Fig-4(a) Fig-4(b)

The electrostatic energy in Fig. 4(a) is lower than that in Fig. 4(b), which means the output cell in Fig. 4(a) is more stable than the case in Fig. 4(b)

Case	Fig. 4(a) (electron x)		Fig. 4(a) (electron y)	
	r_{ix} (nm)	$U_{ix} \times 10^{-26}$ (J)	r_{iy} (nm)	$U_{iy} \times 10^{-26}$ (J)
	U_{T1x}	22.0275	U_{T1y}	10.3873
U_{T1}	32.4147 $\times 10^{-26}$ (J)			
	Fig. 4(b) (electron x)		Fig. 4(b) (electron y)	
	U_{T2x}	11.3742	U_{T2y}	23.1900
U_{T2}	34.5642 $\times 10^{-26}$ (J)			

TABLE:1

Power Analysis:

We compute the dissipation of switching and leakage energy. We test our design at 1.5 Ek at 2 K. The average switching, leakage energy dissipation, and total energy dissipation are listed in Table II as three metrics of power evaluation for the XOR and XNOR gates. The suggested XOR/XNOR uses 0.02849 and 0.03269 watts of power in total, respectively.

Tunnelling energy levels	XOR logic function	XNOR logic function
Avg. leakage energy dissipation (Ev)	0.01846	0.01783
Avg. switching energy dissipation (Ev)	0.01003	0.01485
Total energy dissipation (Ev)	0.02849	0.03269

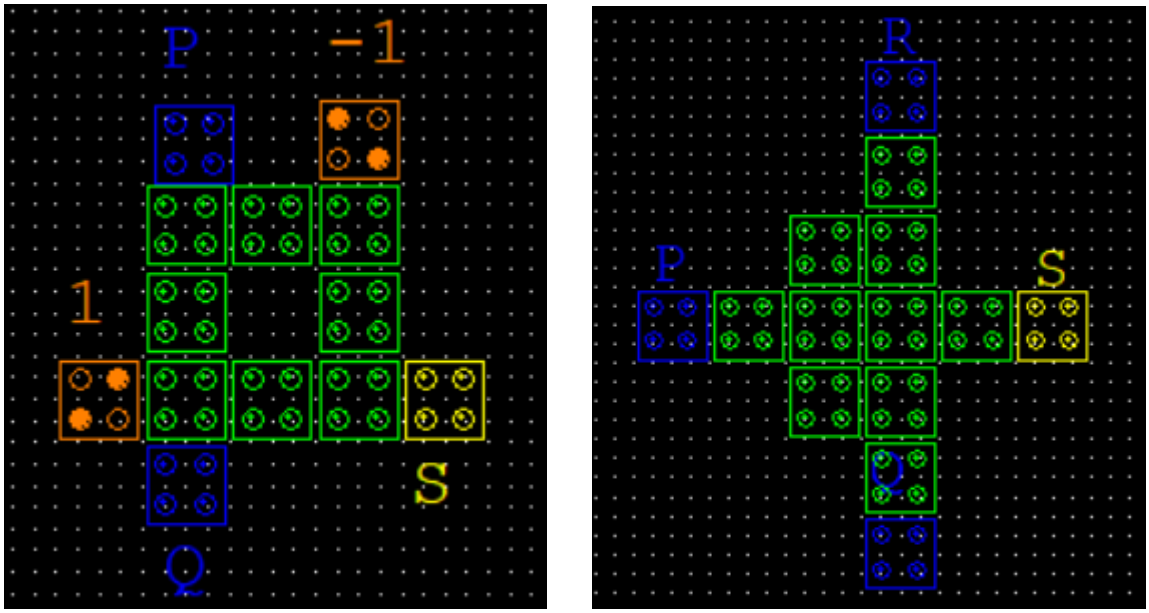
TABLE:2

Reliability Evaluation:

A key criterion for evaluating a QCA circuit's quality is reliability. A suitable analytical model in QCA technology is the probability transfer matrix (PTM) model, which is a tool for evaluating the accuracy of a single device component in order to assess the dependability of the complete circuit. Using the probabilistic transfer matrix model, we compare the dependability of several XOR structures to our suggested XOR/XNOR structures.

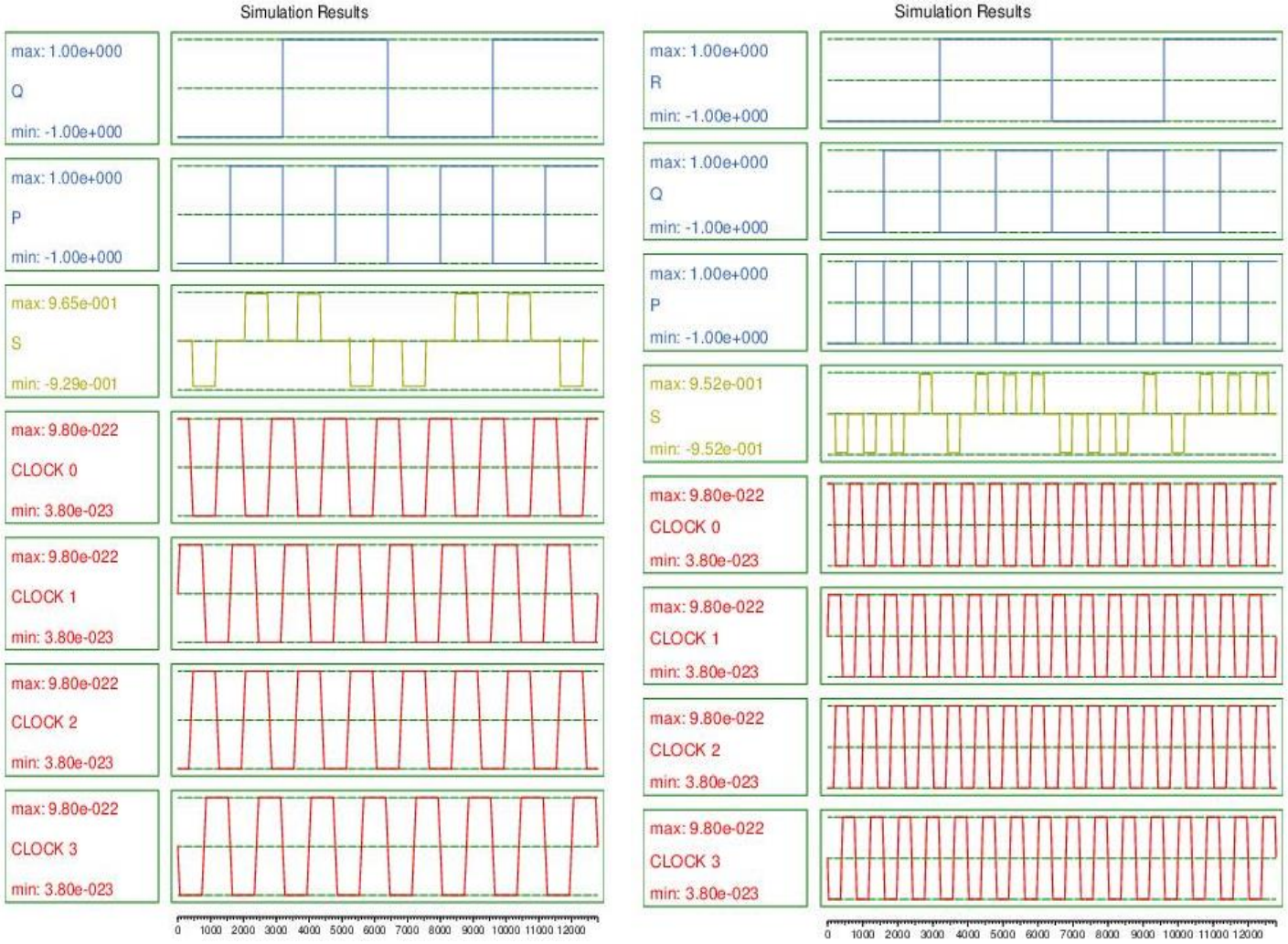
The possibility of producing incorrect outputs is indicated by the XOR experience mistake with probability. The probability that any component or gate will be flawed is referred to as error with probability. Of these structures, the proposed XOR/XNOR has the lowest error probability and is hence the most stable. In particular, the structure with more majority gates has a higher probability of error than the others when the device chance of mistake changes. Some structures have the same stability as others because they share the same basic logical building block.

QCA Layout of the XOR gate based on cell level & 3-input XOR (TIEO):



Figs: Cell level & 3-input XOR (TIEO) based XOR Gate

Simulation results of XOR gate based on cell level & 3-input XOR (TIEO):



Figs: Cell level & 3-input XOR (TIEO) based XOR gate's QCA Simulation Results.

Comparison between XOR gate based on cell level & 3-input XOR(TIEO):

	XOR/XNOR Based on cell level	XOR/XNOR using 3-input XOR (TIEO)
Cell Count	13	14
Area	0.01um^2	0.02um^2
Latency	0.25	0.5
Cost	0.00390625	0.0625

TABLE:3

- XOR/XNOR gate based on cell level has 13 cell count whereas XOR/XNOR gate using 3-input XOR (TIEO) has 14 cell count.

- XOR/XNOR gate based on cell level has area of 0.01um^2 whereas XOR/XNOR gate using 3-input XOR (TIEO) has area of 0.02um^2.

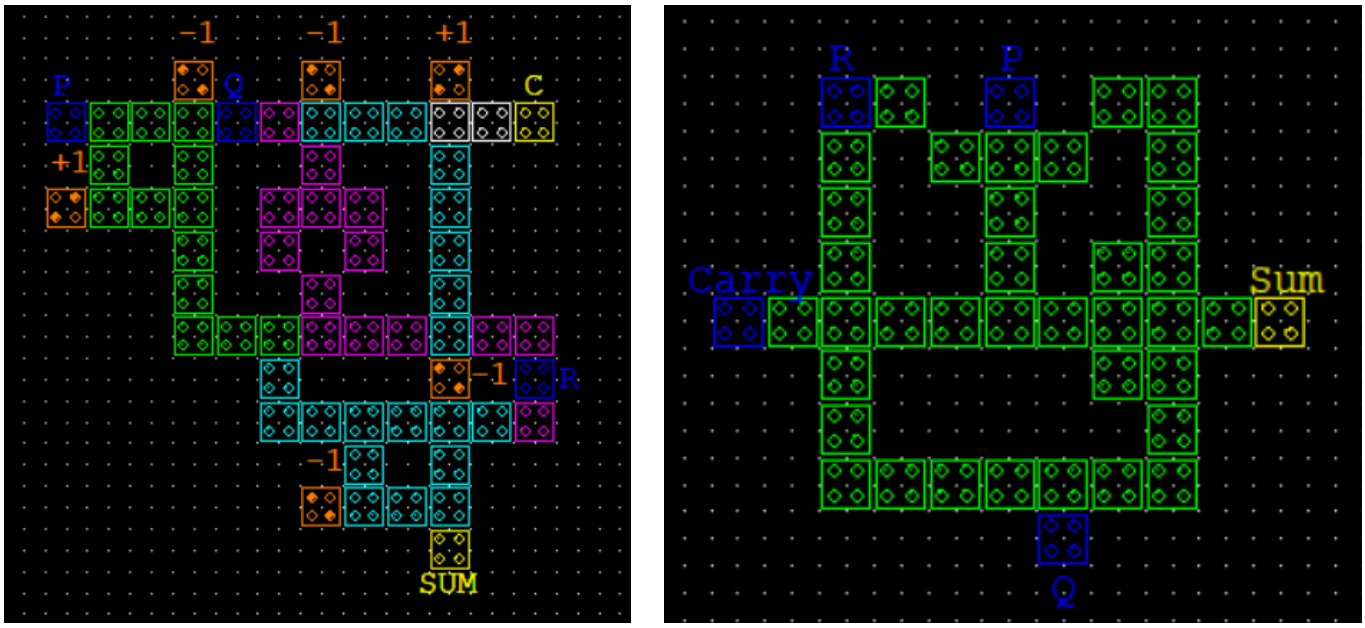
- XOR/XNOR gate based on cell level has only 1 latency (e.g., 0.25 clock cycle), whereas XOR using 3-input XOR (TIEO) has 2 latencies (e.g., 0.50 clock cycle).

- The cost of XOR/XNOR gate based on cell level is 0.00390625, while XOR/XNOR gate using 3-input XOR (TIEO) has cost of 0.0625. The costs are determined by the cost function of a QCA circuit, which is cost=(M^K+I+C^I) *T^P. Here, M denotes the quantity of majority gates, I denotes the quantity of inverters, C denotes the quantity of crossovers, T denotes the circuit's latency, and K, I, and P denote the weightings that are exponential of M, C, and T, respectively. The values for K, I, and P in this work for cell level are respectively 2, 2, and 4.

Design of complex QCA circuits:

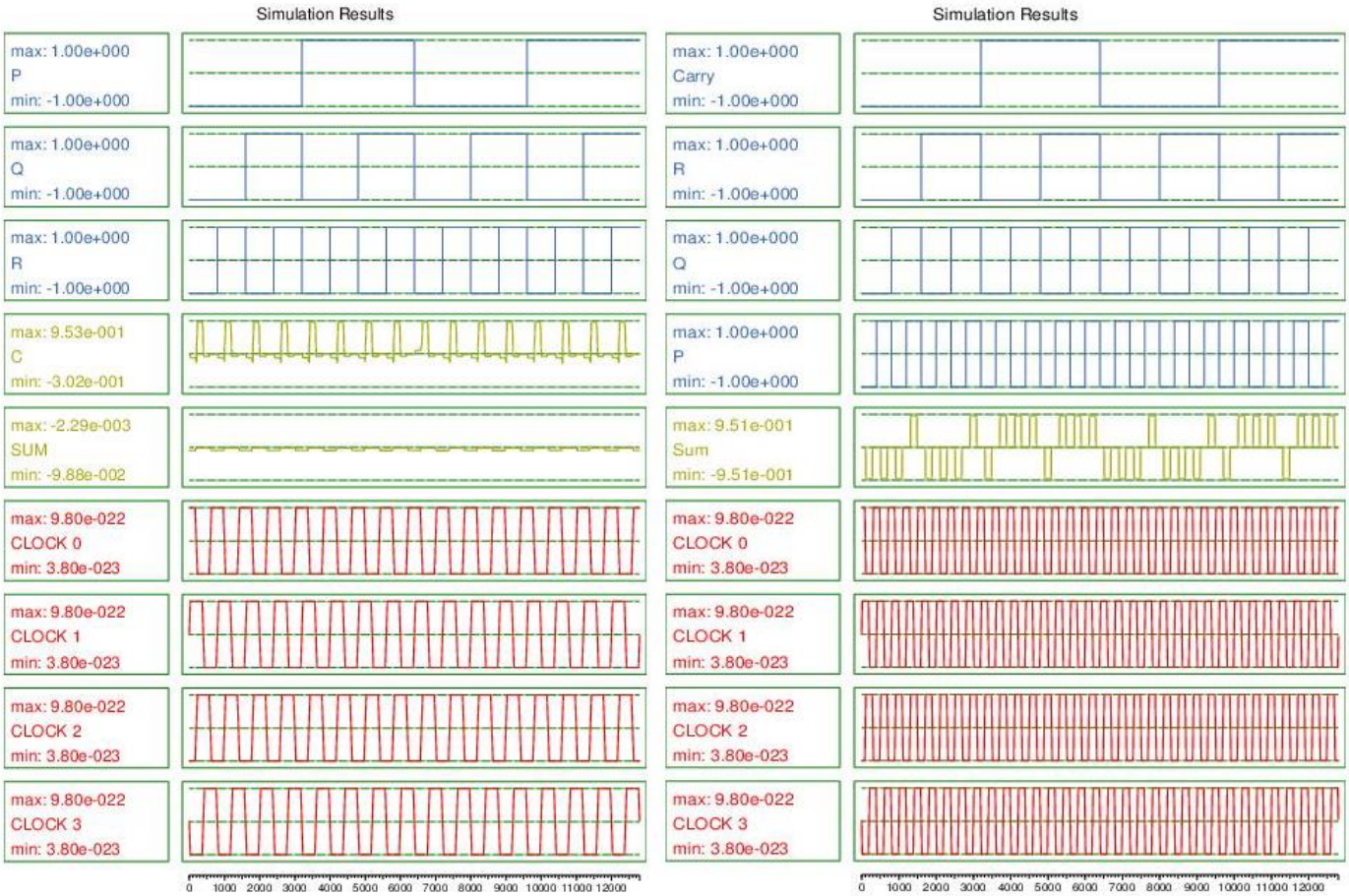
Some common circuits would be implemented in this project to show how adaptable the unique XOR/XNOR (proposed) is in huge and complex circuits. Implemented are the 4-bit parity generators, 1-bit Comparator, and 1-bit Full Adder.

QCA Layout of the Full Adder based on logic Gates & A three-input majority gate and TIEO block:



Figs: Logic Gates & A Three-input majority gate and TIEO block based Full Adder

Simulation Results of the Full Adder based on logic gates & A three-input majority gate and TIEO block: -



Figs: Logic Gates & A Three-input majority gate and TIEO block based Full Adder's QCA simulation result

Comparison between Full Adder based on logic gates & A Three-input majority gate and TIEO block: -

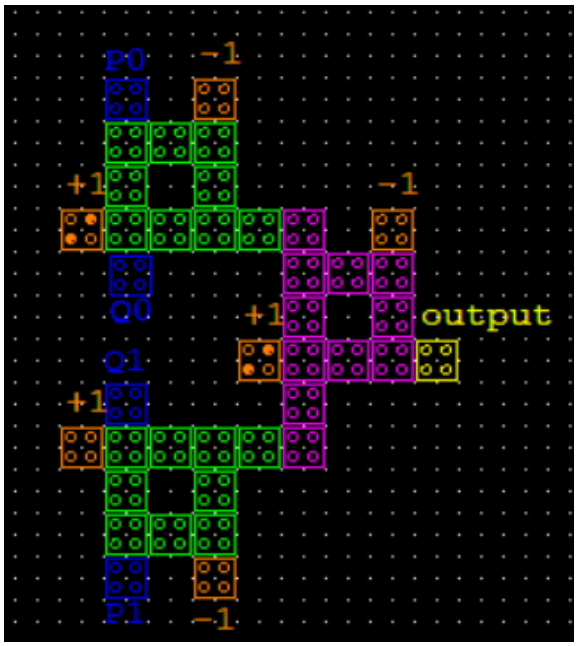
The 1-bit Full Adder shown in left side is composed of six basic logic gates including two XOR gates,2 AND gates, 2 OR gates and 1 Inverter. It does not make use of coplanar cross-wiring and only uses 60 QCA normal cells. The 1-bit full adder design has a 0.75 clock cycle delay and an appealing area of roughly 0.057 m^2. QCA Layout of the Novel 4-bit parity

The 1 Bit full adder Shown in right hand side is composed of two main components, a three-input majority gate, and a TIEO block. It makes use of coplanar cross-wiring and only uses 41 QCA normal cells. The 1-bit full adder design has a 0.5 clock cycle delay and an appealing area of roughly 0.04 m^2.

	Full adder Based on logic gates	Full adder based on Three-input majority gate and TIEO block: -
Cell Count	60	41
Area	0.057um^2	0.04um^2
Latency	0.75	0.5

TABLE:4

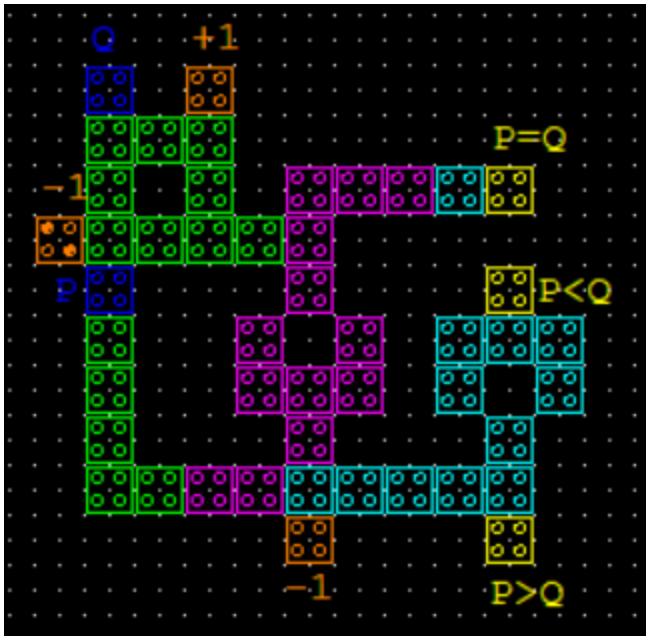
QCA Layout of the Novel 4-bit parity:



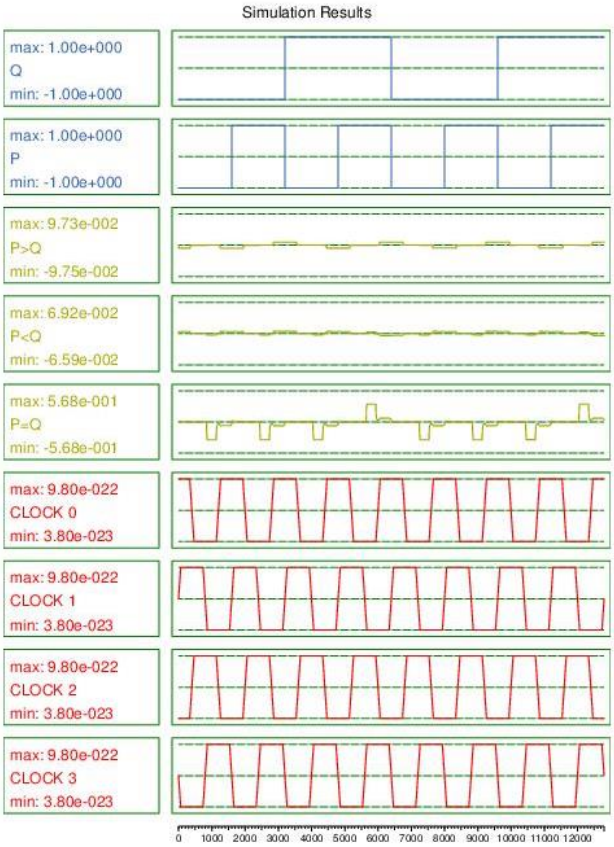
Simulation results of Novel 4-bit parity:

Three XOR logic gates are used in the 4-bit parity circuit. The design is implemented in a single layer, and the output cells are represented by P0, P1, Q0, and Q1. It does not use the coplanar cross wiring and only uses 40 QCA normal cells. The 4-bit parity circuit design has a 0.5 clock cycle delay and an attractive area of roughly 0.04 m^2.

QCA Layout of the Novel 1-bit full comparator:



Simulation results of Novel 1-bit full comparator:



The 1-bit full comparator is composed of four basic logic gates, containing one XOR gate, one 3-input majority gate, and two inverters. P and Q indicate input cells whereas P=Q, P >Q, and P<Q represent output cells in the single layer where the design is implemented. It does not make use of coplanar cross-wiring and only uses 47 QCA normal cells. The 1-bit complete comparator architecture has a 0.75 clock cycle delay and an attractive area of roughly 0.04 m2.

Conclusion:

We have developed a new XOR/NOR logic gate in this project. The work directly relates to constructing some functional circuits in the QCA field where efficiency is a goal. A revolutionary XOR/XNOR logic gate has first been introduced, and several intricate circuits have since been suggested based on it. Through physical testing and modelling, the suggested XOR/XNOR logic gate's functionality was confirmed.

It was established that the proposed XOR/XNOR logic gate uses fewer cells and covers a smaller area. There is just 1 latency in the suggested XOR gate (i.e., 0.25 clock cycle). The proposed XOR/XNOR architecture has the lowest total cost at 0.01, which is 0.00390625. In order to create big and complex circuits based on QCA (1-bit complete adder, 4-bit parity generators, and 1-bit Comparator), the proposed XOR/XNOR can be employed as a fundamental logic gate. As a result, it is very adaptable.