Synopsys Design Constraints (SDC) Basics

Full form of SDC: - Synopsys Design Constraints.

What is SDC: - SDC is a format used to specify the design intent, including the timing, power and area constraints for a design. SDC is tcl based.

Tool used this format: - DC (Design compiler, ICC (IC compiler), Prime Time (PT).

Information In the SDC: - There are mainly 4 type of the information.

1. The SDC version (optional)
2. The SDC units (optional)
3. The Design Constraints
4. Comments (Optional)

1. SDC version:

Variable name: sdc_version
E.g:- set sdc_version
Default Version: 1.9

2. SDC units:

Command name: set_units
Description: using above command you can specify the units for capacitance, resistance, time, voltage, current, and power
E.g:

```
set_units -capacitance cap_unit -resistance res_unit \
-time time_unit -voltage voltage_unit \
-current current_unit -power power_unit
```

3. Design Constraints:

You can specify design constraints using Synopsys constraints commands. (Note: If you want to know further details of each and every constraints- Please refer the Design Constraint Blog)

Type of information	Commands
Operating conditions	set_operating_conditions

Wire load models	set_wire_load_min_block_size set_wire_load_mode set_wire_load_model set_wire_load_selection_group
System interface	set_drive set_driving_cell set_fanout_load set_input_transition set_load set_port_fanout_number
Design rule constraints	set_max_capacitance set_max_fanout set_max_transition set_min_capacitance
Timing constraints	create_clock create_generated_clock group_path set_clock_gating_check set_clock_groups set_clock_latency set_clock_sense set_clock_transition set_clock_uncertainty set_data_check set_disable_timing set_ideal_latency set_ideal_network set_ideal_transition set_input_delay set_max_time_borrow set_output_delay set_propagated_clock set_resistance set_timing_derate
Timing exceptions	set_false_path set_max_delay set_min_delay set_multicycle_path
Area constraints	set_max_area
Multivoltage and power optimization constraints	create_voltage_area set_level_shifter_strategy set_level_shifter_threshold set_max_dynamic_power set_max_leakage_power
Logic assignments	set_case_analysis set_logic_dc set_logic_one set_logic_zero

Most of the constraint commands require a design object as a command argument.
Design Objects:

Design object	Access command	Description
design	current_design	A container for cells. A block.
clock1	get_clocks all_clocks	A clock in a design. All clocks in a design.
port	get_ports all_inputs all_outputs	An entry point to or exit point from a design. All entry points to a design. All exit points from a design.
cell	get_cells.	An instance of a design or library cell
pin	get_pins	An instance of a design port or library cell pin.
net	get_nets	A connection between cell pins and design ports
library	get_libs	A container for library cells
lib_cell	get_lib_cells	A primitive logic element.
lib_pin	get_lib_pins	An entry point to or exit point from a lib_cell.
register	all_registers	A sequential logic cell.

4. Comments:

You can add comments to an SDC file either as complete lines or as fragments after a command. To identify a line as a comment, start the line with a pound sign (#).
E.g : # This is an SDC comment line.
To add a comment after a command, end the command using a semicolon, then precede the comment with a pound sign (#).
E.g: create_clock -period 10 [get_ports CLK]; # comment fragment

How to generate The SDC file Automatically:

Using Synopsys Tool like DC, ICC or PrimeTime you can generate the SDC. There may be slight variation between the generated SDC across the different tool.
Command for generation: - write_sdc

Validation of manually generated SDC files:-
Command file: read_sdc -syntax_only