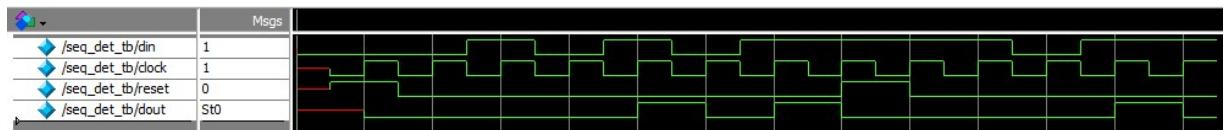


LAB 6 – Raja Aadhithan

Design – Sequence Detector:

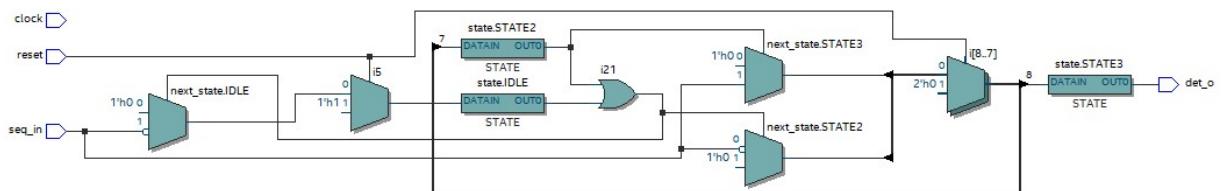
Wave:



Output:

```
VSIM 41> run -all
# Reset=x, state=xx, Din=0, Output Dout=x
# Reset=1, state=xx, Din=0, Output Dout=x
# Reset=1, state=00, Din=0, Output Dout=0
# Reset=0, state=00, Din=0, Output Dout=0
# Reset=0, state=00, Din=1, Output Dout=0
# Reset=0, state=01, Din=1, Output Dout=0
# Reset=0, state=01, Din=0, Output Dout=0
# Reset=0, state=10, Din=0, Output Dout=0
# Reset=0, state=10, Din=1, Output Dout=0
# Correct output at state 11
# Reset=0, state=11, Din=1, Output Dout=1
# Reset=0, state=11, Din=0, Output Dout=1
# Reset=0, state=10, Din=0, Output Dout=0
# Reset=0, state=10, Din=1, Output Dout=0
# Correct output at state 11
# Reset=0, state=11, Din=1, Output Dout=1
# Reset=1, state=00, Din=1, Output Dout=0
# Reset=0, state=01, Din=1, Output Dout=0
# Reset=0, state=01, Din=0, Output Dout=0
# Reset=0, state=10, Din=0, Output Dout=0
# Reset=0, state=10, Din=1, Output Dout=0
# Correct output at state 11
# Reset=0, state=11, Din=1, Output Dout=1
# Reset=0, state=01, Din=1, Output Dout=0
# ** Note: $finish : C:/Users/Aadhithan/Documents/VHDL/tb/seq_det_tb.v(117)
#   Time: 135 ps Iteration: 0 Instance: /seq_det_tb
.
```

RTL:



Design : Vending machine:

Wave:



Output:

```
VSIM 45> run -all
# @time: 0, input (ij) is x,x and output (xy) is 0,0
# @time: 15, input (ij) is 0,1 and output (xy) is 0,0
# @time: 25, input (ij) is 0,0 and output (xy) is 0,0
# @time: 35, input (ij) is 1,1 and output (xy) is 0,0
# @time: 45, input (ij) is 1,0 and output (xy) is 0,0
# @time: 50, input (ij) is 1,0 and output (xy) is 1,0
# @time: 55, input (ij) is 0,1 and output (xy) is 1,0
# @time: 60, input (ij) is 0,1 and output (xy) is 0,0
# @time: 65, input (ij) is 1,1 and output (xy) is 0,0
# @time: 80, input (ij) is 1,1 and output (xy) is 1,1
# @time: 85, input (ij) is 1,0 and output (xy) is 1,1
# @time: 90, input (ij) is 1,0 and output (xy) is 0,0
# @time: 95, input (ij) is 1,1 and output (xy) is 0,0
# @time: 105, input (ij) is 1,0 and output (xy) is 0,0
# @time: 110, input (ij) is 1,0 and output (xy) is 1,0
# @time: 115, input (ij) is 0,1 and output (xy) is 1,0
# @time: 120, input (ij) is 0,1 and output (xy) is 0,0
# @time: 125, input (ij) is 1,1 and output (xy) is 0,0
# @time: 140, input (ij) is 1,1 and output (xy) is 1,1
# @time: 145, input (ij) is 1,0 and output (xy) is 1,1
# @time: 150, input (ij) is 1,0 and output (xy) is 0,0
# ** Note: $finish      : C:/Users/Aadhithan/Documents/Ve:
#   Time: 155 ps  Iteration: 0  Instance: /coin_tb
# 1
```

RTL:

