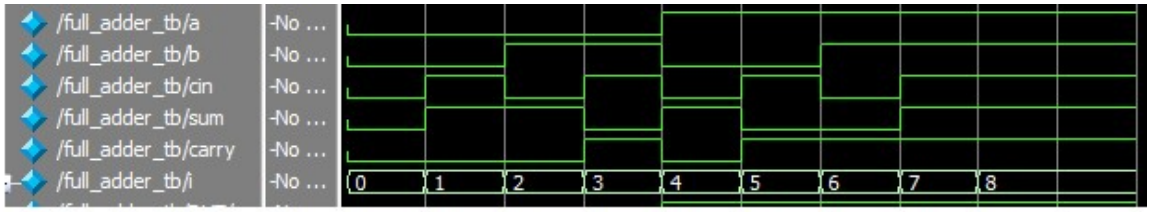
LAB 1 – Raja Aadhithan

Design - Full adder using Half adder:

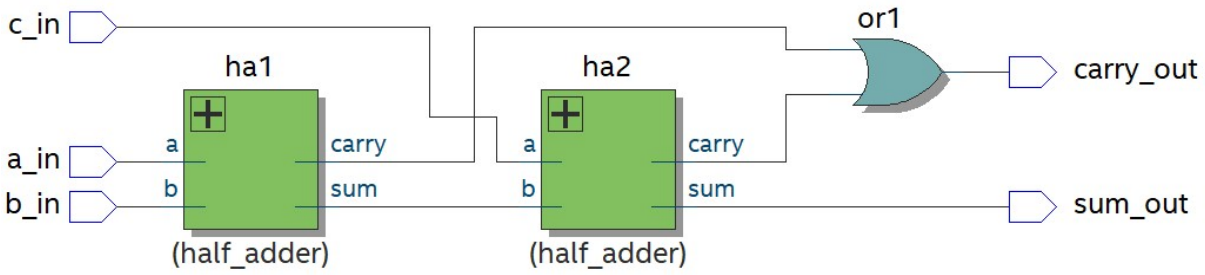
Wave:



Output:

```
# Input a=0, b=0, c=0, Output sum =0, carry=0
# Input a=0, b=0, c=1, Output sum =1, carry=0
# Input a=0, b=1, c=0, Output sum =1, carry=0
# Input a=0, b=1, c=1, Output sum =0, carry=1
# Input a=1, b=0, c=0, Output sum =1, carry=0
# Input a=1, b=0, c=1, Output sum =0, carry=1
# Input a=1, b=1, c=0, Output sum =0, carry=1
# Input a=1, b=1, c=1, Output sum =1, carry=1
```

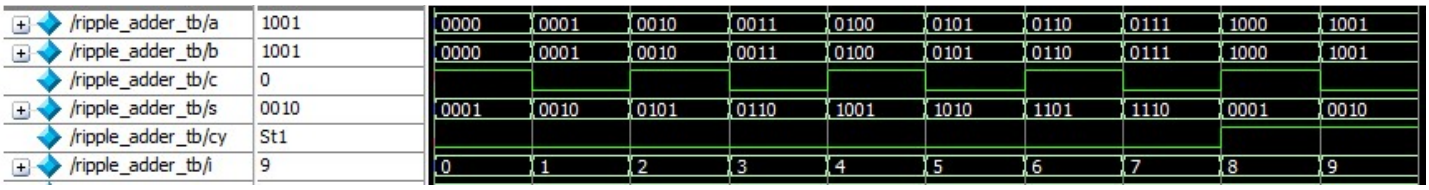
RTL:



Exercises:

Design : Ripple adder

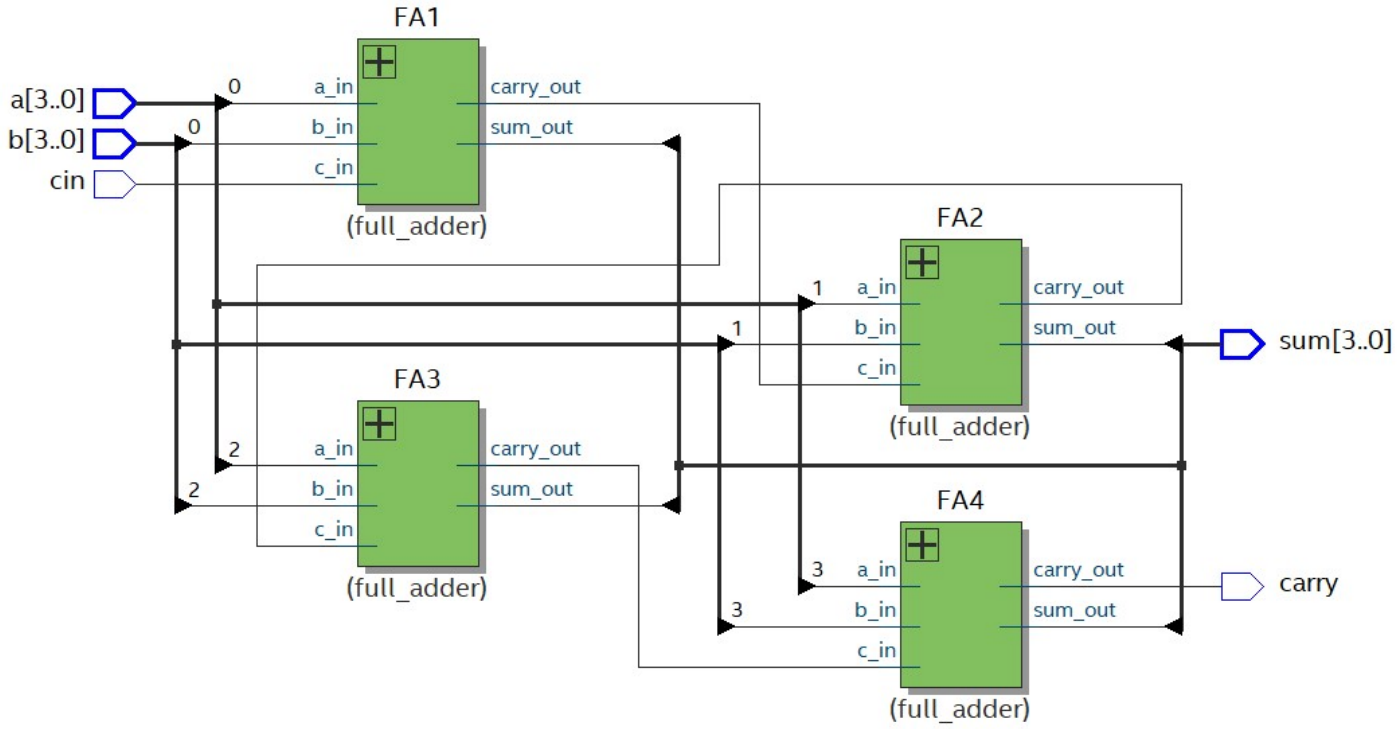
Wave:



Output:

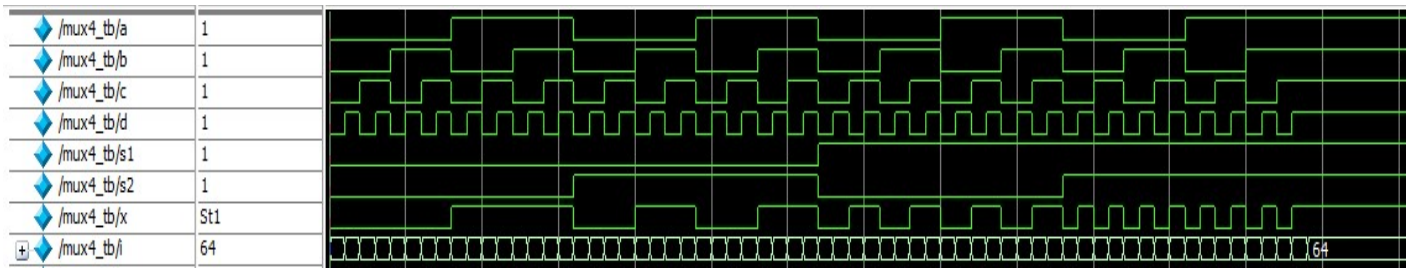
```
VSIM 28> run -all
# Input a=0000, b=0000, c=1, Output sum =0001, carry=0
# Input a=0001, b=0001, c=0, Output sum =0010, carry=0
# Input a=0010, b=0010, c=1, Output sum =0101, carry=0
# Input a=0011, b=0011, c=0, Output sum =0110, carry=0
# Input a=0100, b=0100, c=1, Output sum =1001, carry=0
# Input a=0101, b=0101, c=0, Output sum =1010, carry=0
# Input a=0110, b=0110, c=1, Output sum =1101, carry=0
# Input a=0111, b=0111, c=0, Output sum =1110, carry=0
# Input a=1000, b=1000, c=1, Output sum =0001, carry=1
# Input a=1001, b=1001, c=0, Output sum =0010, carry=1
# ** Note: $finish    : C:/Users/Aadhithan/Documents/Verilog_labs/lab1/sim/ripple_ad
der_tb.v(26)
#    Time: 100 ps  Iteration: 0  Instance: /ripple_adder_tb
```

RTL:



Design : 4:1 mux using 2:1 mux

Wave:

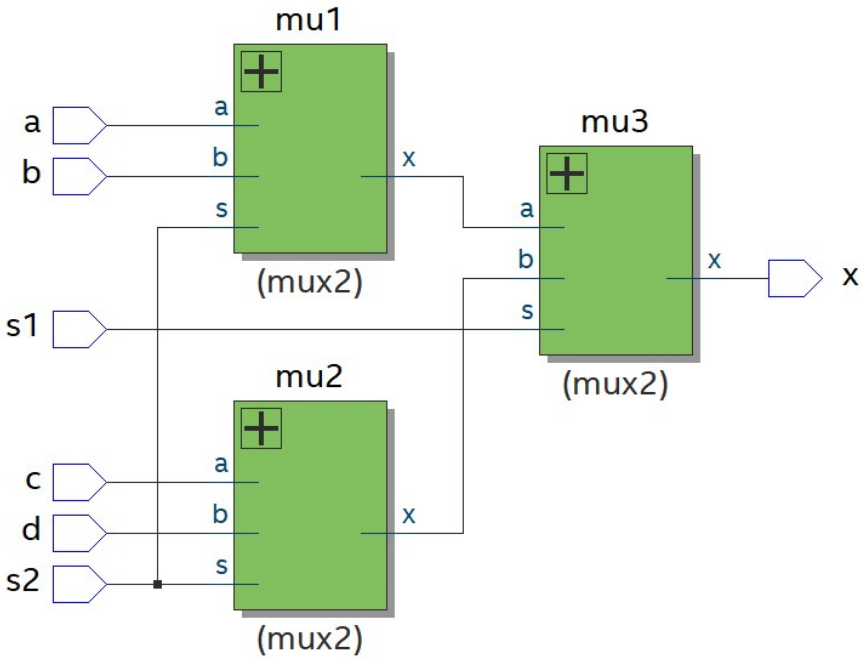


Output:

```
VSIM 34> run -all
# @time:  0- selsct is 00 nad input is 0,0,0,0 for output is 0
# @time: 10- selsct is 00 nad input is 0,0,0,1 for output is 0
# @time: 20- selsct is 00 nad input is 0,0,1,0 for output is 0
# @time: 30- selsct is 00 nad input is 0,0,1,1 for output is 0
# @time: 40- selsct is 00 nad input is 0,1,0,0 for output is 0
# @time: 50- selsct is 00 nad input is 0,1,0,1 for output is 0
# @time: 60- selsct is 00 nad input is 0,1,1,0 for output is 0
# @time: 70- selsct is 00 nad input is 0,1,1,1 for output is 0
# @time: 80- selsct is 00 nad input is 1,0,0,0 for output is 1
# @time: 90- selsct is 00 nad input is 1,0,0,1 for output is 1
# @time:100- selsct is 00 nad input is 1,0,1,0 for output is 1
# @time:110- selsct is 00 nad input is 1,0,1,1 for output is 1
# @time:120- selsct is 00 nad input is 1,1,0,0 for output is 1
# @time:130- selsct is 00 nad input is 1,1,0,1 for output is 1
# @time:140- selsct is 00 nad input is 1,1,1,0 for output is 1
# @time:150- selsct is 00 nad input is 1,1,1,1 for output is 1
# @time:160- selsct is 01 nad input is 0,0,0,0 for output is 0
# @time:170- selsct is 01 nad input is 0,0,0,1 for output is 0
# @time:180- selsct is 01 nad input is 0,0,1,0 for output is 0
# @time:190- selsct is 01 nad input is 0,0,1,1 for output is 0
# @time:200- selsct is 01 nad input is 0,1,0,0 for output is 1
# @time:210- selsct is 01 nad input is 0,1,0,1 for output is 1
# @time:220- selsct is 01 nad input is 0,1,1,0 for output is 1
# @time:230- selsct is 01 nad input is 0,1,1,1 for output is 1
# @time:240- selsct is 01 nad input is 1,0,0,0 for output is 0
# @time:250- selsct is 01 nad input is 1,0,0,1 for output is 0
# @time:260- selsct is 01 nad input is 1,0,1,0 for output is 0
# @time:270- selsct is 01 nad input is 1,0,1,1 for output is 0
# @time:280- selsct is 01 nad input is 1,1,0,0 for output is 1
# @time:290- selsct is 01 nad input is 1,1,0,1 for output is 1
# @time:300- selsct is 01 nad input is 1,1,1,0 for output is 1
# @time:310- selsct is 01 nad input is 1,1,1,1 for output is 1
# @time:320- selsct is 10 nad input is 0,0,0,0 for output is 0
# @time:330- selsct is 10 nad input is 0,0,0,1 for output is 0
```

```
# @time:330- selsct is 10 nad input is 0,0,0,1 for output is 0
# @time:340- selsct is 10 nad input is 0,0,1,0 for output is 1
# @time:350- selsct is 10 nad input is 0,0,1,1 for output is 1
# @time:360- selsct is 10 nad input is 0,1,0,0 for output is 0
# @time:370- selsct is 10 nad input is 0,1,0,1 for output is 0
# @time:380- selsct is 10 nad input is 0,1,1,0 for output is 1
# @time:390- selsct is 10 nad input is 0,1,1,1 for output is 1
# @time:400- selsct is 10 nad input is 1,0,0,0 for output is 0
# @time:410- selsct is 10 nad input is 1,0,0,1 for output is 0
# @time:420- selsct is 10 nad input is 1,0,1,0 for output is 1
# @time:430- selsct is 10 nad input is 1,0,1,1 for output is 1
# @time:440- selsct is 10 nad input is 1,1,0,0 for output is 0
# @time:450- selsct is 10 nad input is 1,1,0,1 for output is 0
# @time:460- selsct is 10 nad input is 1,1,1,0 for output is 1
# @time:470- selsct is 10 nad input is 1,1,1,1 for output is 1
# @time:480- selsct is 11 nad input is 0,0,0,0 for output is 0
# @time:490- selsct is 11 nad input is 0,0,0,1 for output is 1
# @time:500- selsct is 11 nad input is 0,0,1,0 for output is 0
# @time:510- selsct is 11 nad input is 0,0,1,1 for output is 1
# @time:520- selsct is 11 nad input is 0,1,0,0 for output is 0
# @time:530- selsct is 11 nad input is 0,1,0,1 for output is 1
# @time:540- selsct is 11 nad input is 0,1,1,0 for output is 0
# @time:550- selsct is 11 nad input is 0,1,1,1 for output is 1
# @time:560- selsct is 11 nad input is 1,0,0,0 for output is 0
# @time:570- selsct is 11 nad input is 1,0,0,1 for output is 1
# @time:580- selsct is 11 nad input is 1,0,1,0 for output is 0
# @time:590- selsct is 11 nad input is 1,0,1,1 for output is 1
# @time:600- selsct is 11 nad input is 1,1,0,0 for output is 0
# @time:610- selsct is 11 nad input is 1,1,0,1 for output is 1
# @time:620- selsct is 11 nad input is 1,1,1,0 for output is 0
# @time:630- selsct is 11 nad input is 1,1,1,1 for output is 1
# ** Note: $finish    : C:/Users/Aadhithan/Documents/Verilog_labs/lab1/4_2_mux/muv4_
tb.v(16)
#    Time: 1 ns  Iteration: 0  Instance: /mux4_tb
# 1
```

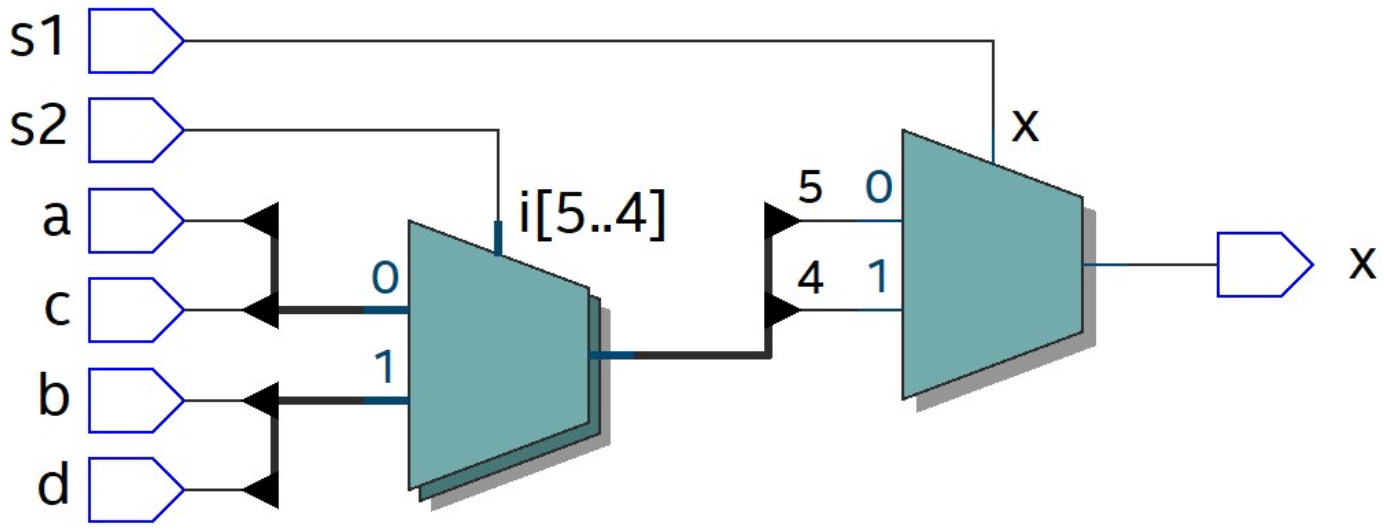
RTL:



Assignment:

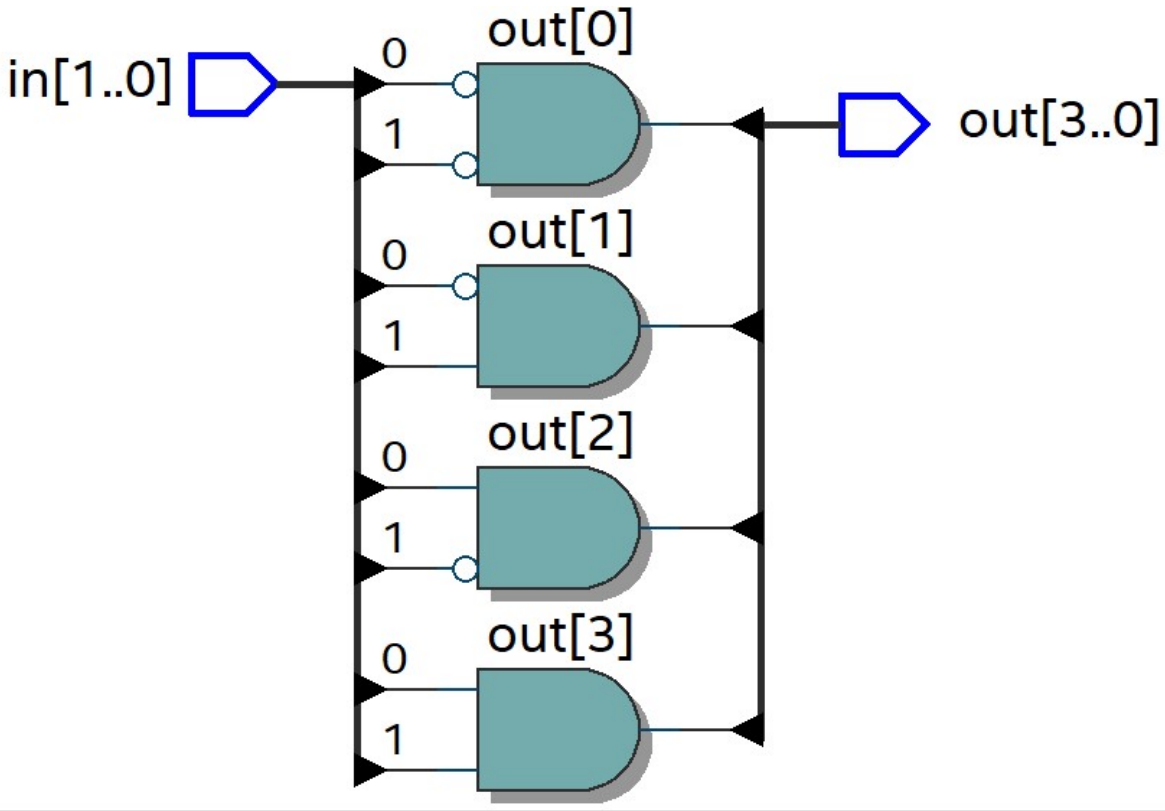
Design: RTL for full adder.

RTL:



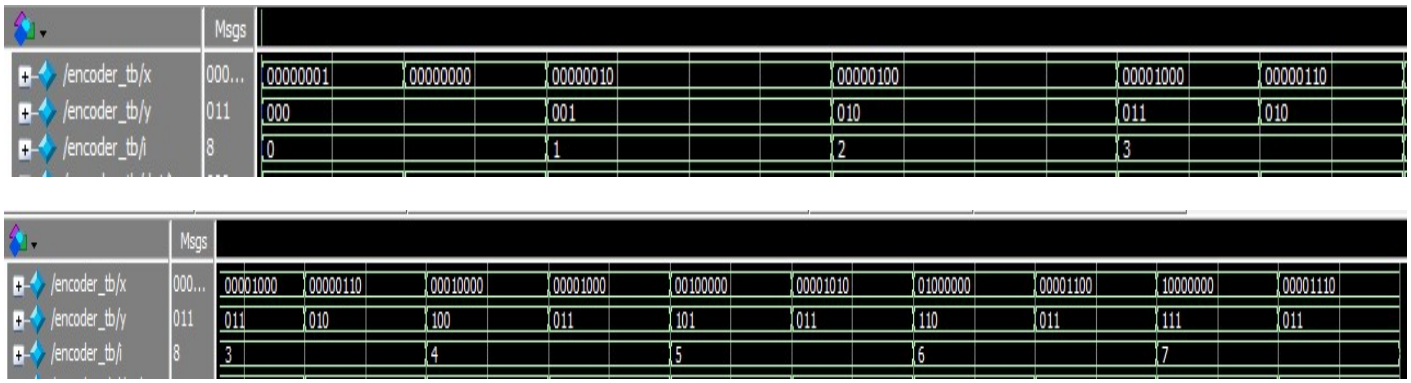
Design: 2x4 decoder.

RTL:



Design: 8x3 priority encoder.

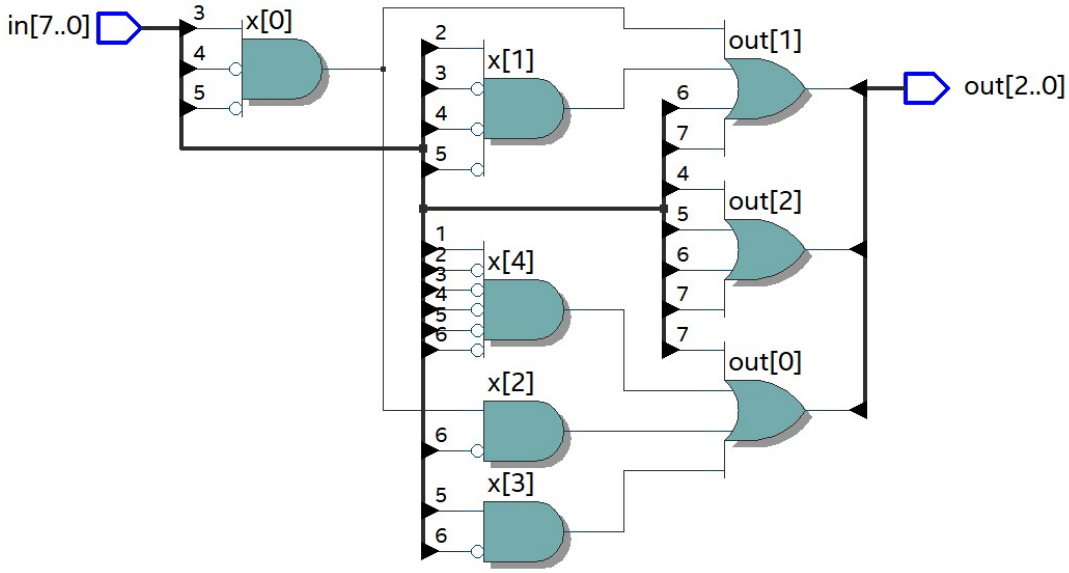
Wave:



Output:

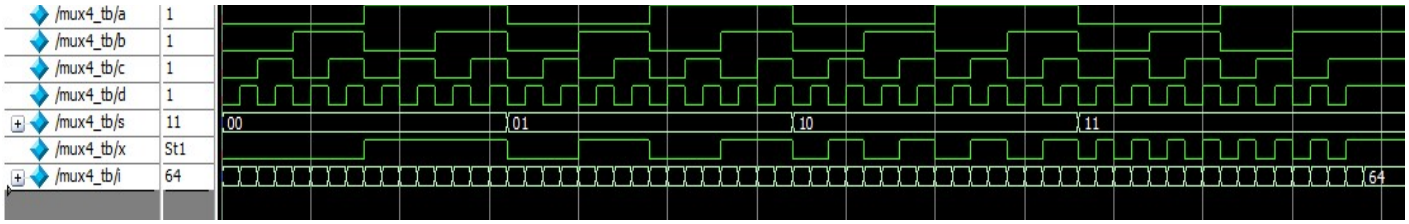
```
VSIM 38> run -all
# @ time:   0ps the input is 00000001 output is 000
# @ time:  10ps the input is 00000000 output is 000
# @ time:  20ps the input is 00000010 output is 001
# @ time:  40ps the input is 00000100 output is 010
# @ time:  60ps the input is 00001000 output is 011
# @ time:  70ps the input is 00000110 output is 010
# @ time:  80ps the input is 00010000 output is 100
# @ time:  90ps the input is 00001000 output is 011
# @ time: 100ps the input is 00100000 output is 101
# @ time: 110ps the input is 00001010 output is 011
# @ time: 120ps the input is 01000000 output is 110
# @ time: 130ps the input is 00001100 output is 011
# @ time: 140ps the input is 10000000 output is 111
# @ time: 150ps the input is 00001110 output is 011
# ** Note: $finish    : C:/Users/Aadhithan/Documents/Verilog_labs/lab1/encoder/encoder_tb.v(14)
#    Time: 160 ps  Iteration: 0  Instance: /encoder_tb
```

RTL:

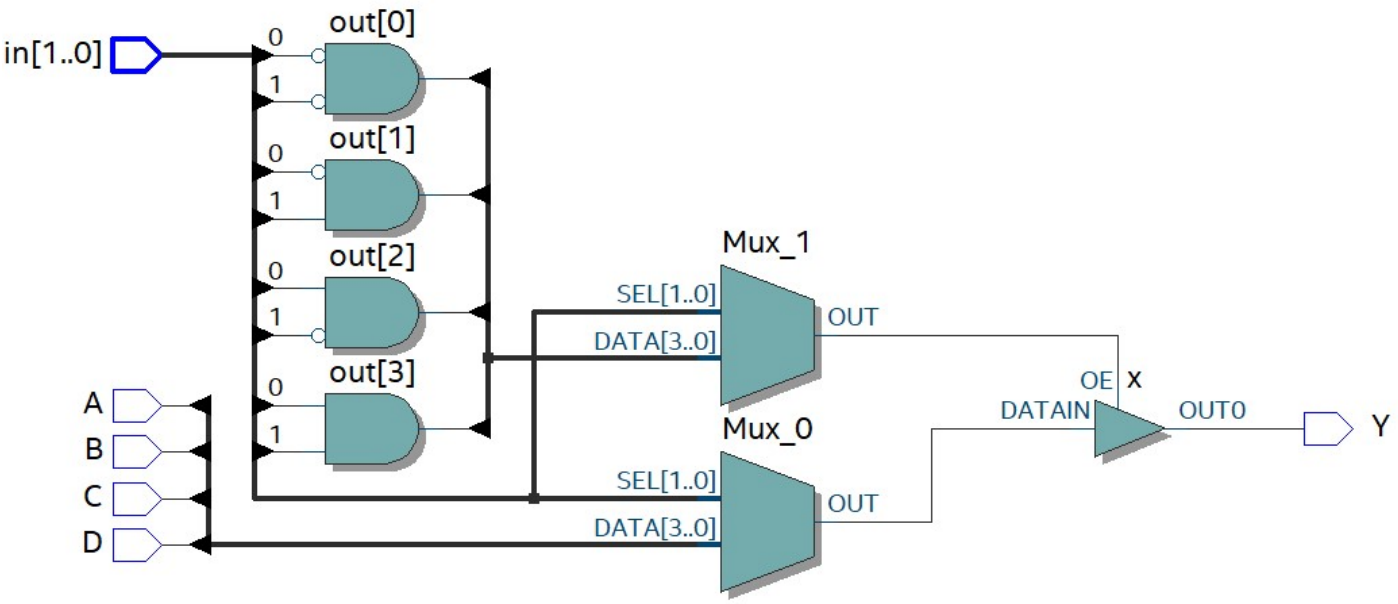


Design: 4x1 mux.

Wave:

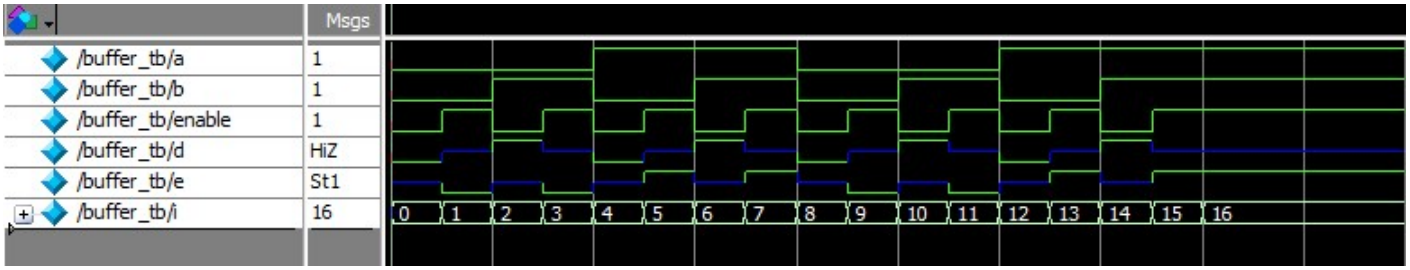


RTL:



Design: Bidirectional buffer

Wave:



Output:

```
VSIM 49> run -all
# @time =   0: The value of a is 0 and b is 0
#  enable is 0
#  output ar is 0 and br is z
# @time =  10: The value of a is 0 and b is 0
#  enable is 1
#  output ar is z and br is 0
# @time =  20: The value of a is 0 and b is 1
#  enable is 0
#  output ar is 1 and br is z
# @time =  30: The value of a is 0 and b is 1
#  enable is 1
#  output ar is z and br is 0
# @time =  40: The value of a is 1 and b is 0
#  enable is 0
#  output ar is 0 and br is z
# @time =  50: The value of a is 1 and b is 0
#  enable is 1
#  output ar is z and br is 1
# @time =  60: The value of a is 1 and b is 1
#  enable is 0
#  output ar is 1 and br is z
# @time =  70: The value of a is 1 and b is 1
#  enable is 1
#  output ar is z and br is 1
# @time =  80: The value of a is 0 and b is 0
#  enable is 0
#  output ar is 0 and br is z
# @time =  90: The value of a is 0 and b is 0
#  enable is 1
#  output ar is z and br is 0
# @time = 100: The value of a is 0 and b is 1
#  enable is 0
#  output ar is 1 and br is z
# @time = 100: The value of a is 0 and b is 1
#  enable is 0
#  output ar is 1 and br is z
# @time = 110: The value of a is 0 and b is 1
#  enable is 1
#  output ar is z and br is 0
# @time = 120: The value of a is 1 and b is 0
#  enable is 0
#  output ar is 0 and br is z
# @time = 130: The value of a is 1 and b is 0
#  enable is 1
#  output ar is z and br is 1
# @time = 140: The value of a is 1 and b is 1
#  enable is 0
#  output ar is 1 and br is z
# @time = 150: The value of a is 1 and b is 1
#  enable is 1
#  output ar is z and br is 1
```

RTL: