LAB 5 – Raja Aadhithan

Design – Single port RAM:

Output:

```
SIM 14> run -all
| @time:    0 enable is 0, Write is 0 address is xxxx, data is zzzzzzzz
| @time:   10 enable is 0, Write is 1 address is 0000, data is 00000000
| @time:   20 enable is 0, Write is 1 address is 0001, data is 00000001
| @time:   30 enable is 0, Write is 1 address is 0010, data is 00000010
| @time:   40 enable is 0, Write is 1 address is 0011, data is 00000011
| @time:   50 enable is 0, Write is 1 address is 0100, data is 00000100
| @time:   60 enable is 0, Write is 1 address is 0101, data is 00000101
| @time:   70 enable is 0, Write is 1 address is 0110, data is 00000110
| @time:   80 enable is 0, Write is 1 address is 0111, data is 00000111
| @time:   90 enable is 0, Write is 1 address is 1000, data is 00001000
| @time:  100 enable is 0, Write is 1 address is 1001, data is 00001001
| @time:  110 enable is 0, Write is 1 address is 1010, data is 00001010
| @time:  120 enable is 0, Write is 1 address is 1011, data is 00001011
| @time:  130 enable is 0, Write is 1 address is 1100, data is 00001100
| @time:  140 enable is 0, Write is 1 address is 1101, data is 00001101
| @time:  150 enable is 0, Write is 1 address is 1110, data is 00001110
| @time:  160 enable is 0, Write is 1 address is 1111, data is 00001111
| @time:  170 enable is 0, Write is 0 address is 1111, data is zzzzzzzz
| @time:  180 enable is 1, Write is 0 address is 0000, data is 00000000
| @time:  190 enable is 1, Write is 0 address is 0001, data is 00000001
| @time:  200 enable is 1, Write is 0 address is 0010, data is 00000010
| @time:  210 enable is 1, Write is 0 address is 0011, data is 00000011
| @time:  220 enable is 1, Write is 0 address is 0100, data is 00000100
| @time:  230 enable is 1, Write is 0 address is 0101, data is 00000101
| @time:  240 enable is 1, Write is 0 address is 0110, data is 00000110
| @time:  250 enable is 1, Write is 0 address is 0111, data is 00000111
| @time:  260 enable is 1, Write is 0 address is 1000, data is 00001000
| @time:  270 enable is 1, Write is 0 address is 1001, data is 00001001
| @time:  280 enable is 1, Write is 0 address is 1010, data is 00001010
| @time:  290 enable is 1, Write is 0 address is 1011, data is 00001011
| @time:  300 enable is 1, Write is 0 address is 1100, data is 00001100
| @time:  310 enable is 1, Write is 0 address is 1101, data is 00001101
| @time:  320 enable is 1, Write is 0 address is 1110, data is 00001110
| @time:  330 enable is 1, Write is 0 address is 1111, data is 00001111
| ** Note: $finish    : C:/Users/Aadhithan/Documents/Verilog_labs/lab5/t
|    Time: 350 ps  Iteration: 0  Instance: /ram_tb
```
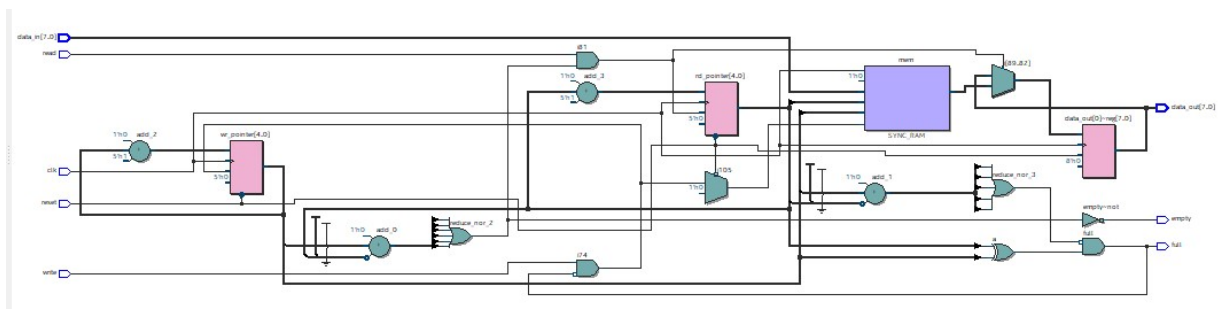
Wave:

RTL:

Too lengthy to crop.

Exercise:

Design : FIFO:

Wave: Zoomed out version

Output:

```
VSIM 21> run -all
# $@time:  0, read :x, write :x, datain = xxxxxxxx, dataout = xxxxxxxx
# $@time: 20, read :0, write :1, datain = 00000101, dataout = xxxxxxxx
# $@time: 30, read :0, write :1, datain = 00001111, dataout = xxxxxxxx
# $@time: 40, read :0, write :1, datain = 00010101, dataout = xxxxxxxx
# $@time: 50, read :0, write :1, datain = 00011111, dataout = xxxxxxxx
# $@time: 60, read :0, write :1, datain = 00101001, dataout = xxxxxxxx
# $@time: 70, read :0, write :1, datain = 00001100, dataout = xxxxxxxx
# $@time: 80, read :0, write :1, datain = 00001101, dataout = xxxxxxxx
# $@time: 90, read :0, write :1, datain = 00100001, dataout = xxxxxxxx
# $@time:100, read :0, write :1, datain = 00101010, dataout = xxxxxxxx
# $@time:110, read :0, write :1, datain = 00010000, dataout = xxxxxxxx
# $@time:120, read :1, write :1, datain = 00000010, dataout = 00000101
# $@time:130, read :1, write :1, datain = 00000001, dataout = 00001111
# $@time:140, read :1, write :1, datain = 00000010, dataout = 00010101
# $@time:150, read :1, write :1, datain = 00000011, dataout = 00011111
# $@time:160, read :1, write :1, datain = 00000100, dataout = 00101001
# $@time:170, read :1, write :1, datain = 00010101, dataout = 00001100
# $@time:180, read :1, write :1, datain = 00011111, dataout = 00001101
# $@time:190, read :1, write :1, datain = 00101001, dataout = 00100001
# $@time:200, read :1, write :1, datain = 00001100, dataout = 00101010
# $@time:210, read :1, write :1, datain = 00001101, dataout = 00010000
# $@time:220, read :1, write :1, datain = 00010101, dataout = 00000010
# $@time:230, read :1, write :1, datain = 00011111, dataout = 00000001
# $@time:240, read :1, write :1, datain = 00101001, dataout = 00000010
# $@time:250, read :1, write :1, datain = 00001100, dataout = 00000011
# $@time:260, read :1, write :1, datain = 00001101, dataout = 00000100
# $@time:270, read :1, write :0, datain = 00001101, dataout = 00010101
# $@time:280, read :1, write :0, datain = 00001101, dataout = 00011111
# $@time:290, read :1, write :1, datain = 00001101, dataout = 00101001
# $@time:300, read :0, write :1, datain = 00001010, dataout = 00101001
# $@time:310, read :0, write :1, datain = 00001011, dataout = 00101001
# $@time:320, read :0, write :1, datain = 00010101, dataout = 00101001
# $@time:330, read :0, write :1, datain = 00011111, dataout = 00101001
# $@time:340, read :0, write :1, datain = 00101001, dataout = 00101001
# $@time:350, read :0, write :1, datain = 00001100, dataout = 00101001
# $@time:360, read :0, write :1, datain = 00001101, dataout = 00101001
# $@time:370, read :0, write :1, datain = 00100001, dataout = 00101001
# $@time:380, read :0, write :1, datain = 00101010, dataout = 00101001
# $@time:390, read :0, write :1, datain = 00010000, dataout = 00101001
# $@time:390, read :0, write :1, datain = 00010000, dataout = 00101001
# $@time:400, read :0, write :1, datain = 00010110, dataout = 00101001
# $@time:410, read :0, write :1, datain = 00011110, dataout = 00101001
# $@time:420, read :0, write :1, datain = 00000110, dataout = 00101001
# $@time:430, read :1, write :0, datain = 00000110, dataout = 00001100
# $@time:440, read :1, write :0, datain = 00000110, dataout = 00001101
# $@time:450, read :1, write :0, datain = 00000110, dataout = 00010101
# $@time:460, read :1, write :0, datain = 00000110, dataout = 00011111
# $@time:465, read :1, write :1, datain = 00011110, dataout = 00011111
# $@time:470, read :1, write :1, datain = 00011110, dataout = 00101001
# $@time:475, read :1, write :0, datain = 00000110, dataout = 00101001
# $@time:480, read :1, write :0, datain = 00000110, dataout = 00001100
# $@time:490, read :1, write :0, datain = 00000110, dataout = 00001101
# $@time:500, read :1, write :0, datain = 00000110, dataout = 00001010
# $@time:510, read :1, write :0, datain = 00000110, dataout = 00001011
# $@time:520, read :1, write :0, datain = 00000110, dataout = 00010101
# $@time:530, read :1, write :0, datain = 00000110, dataout = 00011111
# $@time:540, read :1, write :0, datain = 00000110, dataout = 00101001
# $@time:550, read :1, write :0, datain = 00000110, dataout = 00001100
# $@time:560, read :1, write :0, datain = 00000110, dataout = 00001101
# $@time:570, read :1, write :0, datain = 00000110, dataout = 00100001
# $@time:580, read :1, write :0, datain = 00000110, dataout = 00101010
# $@time:590, read :1, write :0, datain = 00000110, dataout = 00011110
# ** Note: $finish    : C:/Users/Aadhithan/Documents/Verilog_labs/lab5/1
#    Time: 975 ps  Iteration: 0  Instance: /fifo_tb
```
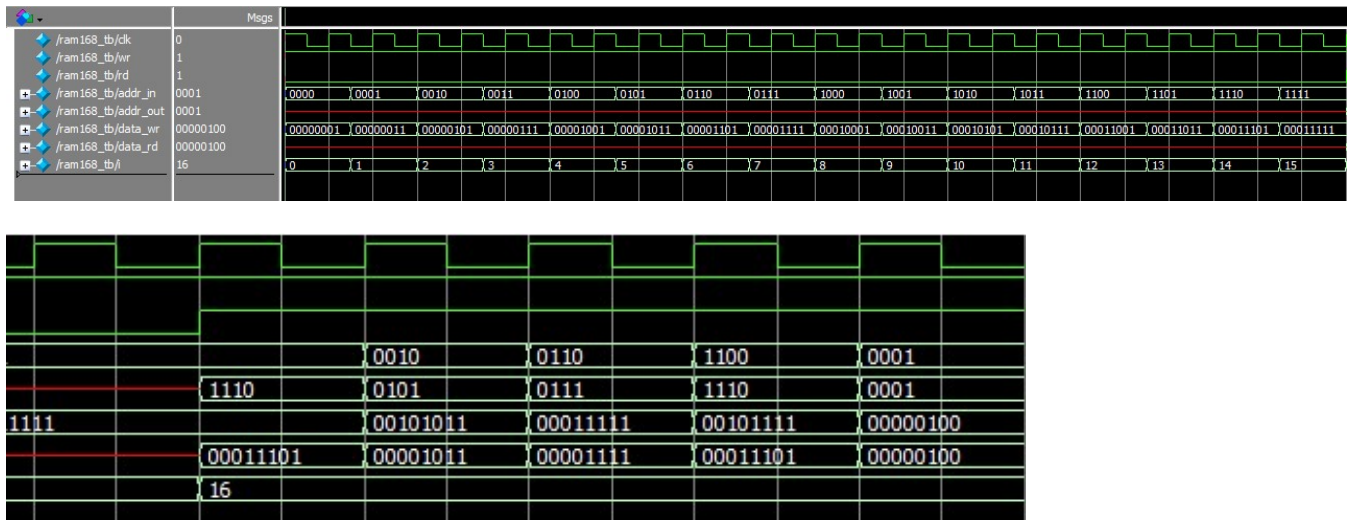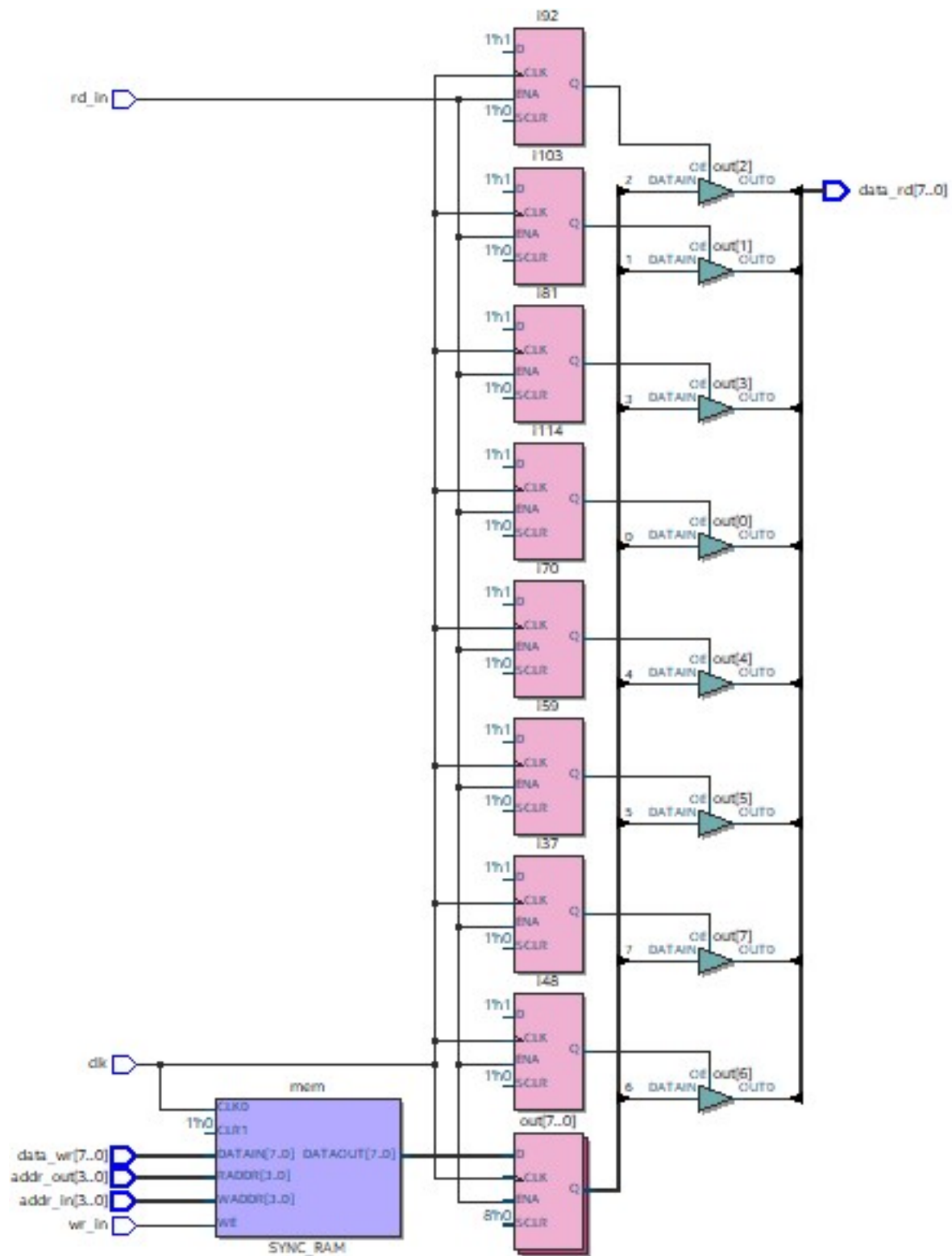
RTL:

Assignments:

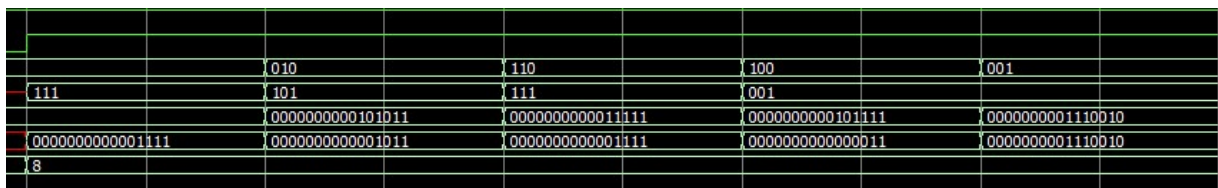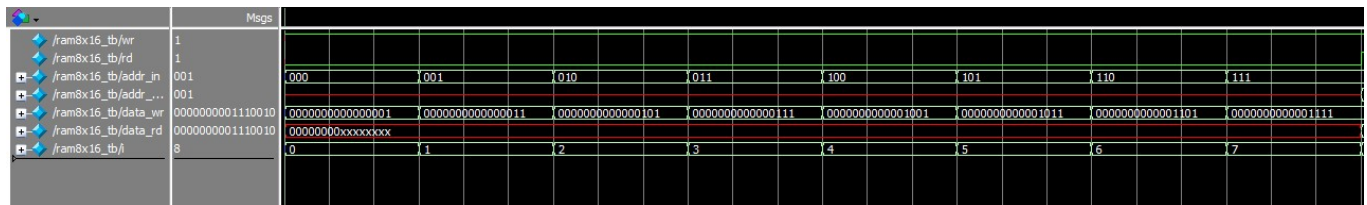Design : 16x8 dual port Ram

Wave:

Output:

```
VSIM 25> run -all
# @time:   0-wr:1,0000,00000001-rd:0,xxxx,xxxxxxxx
# @time: 15-wr:1,0001,00000011-rd:0,xxxx,xxxxxxxx
# @time: 30-wr:1,0010,00000101-rd:0,xxxx,xxxxxxxx
# @time: 45-wr:1,0011,00000111-rd:0,xxxx,xxxxxxxx
# @time: 60-wr:1,0100,00001001-rd:0,xxxx,xxxxxxxx
# @time: 75-wr:1,0101,00001011-rd:0,xxxx,xxxxxxxx
# @time: 90-wr:1,0110,00001101-rd:0,xxxx,xxxxxxxx
# @time:105-wr:1,0111,00001111-rd:0,xxxx,xxxxxxxx
# @time:120-wr:1,1000,00010001-rd:0,xxxx,xxxxxxxx
# @time:135-wr:1,1001,00010011-rd:0,xxxx,xxxxxxxx
# @time:150-wr:1,1010,00010101-rd:0,xxxx,xxxxxxxx
# @time:165-wr:1,1011,00010111-rd:0,xxxx,xxxxxxxx
# @time:180-wr:1,1100,00011001-rd:0,xxxx,xxxxxxxx
# @time:195-wr:1,1101,00011011-rd:0,xxxx,xxxxxxxx
# @time:210-wr:1,1110,00011101-rd:0,xxxx,xxxxxxxx
# @time:225-wr:1,1111,00011111-rd:0,xxxx,xxxxxxxx
# @time:240-wr:1,1111,00011111-rd:1,1110,00011101
# @time:250-wr:1,0010,00101011-rd:1,0101,00001011
# @time:260-wr:1,0110,00011111-rd:1,0111,00001111
# @time:270-wr:1,1100,00101111-rd:1,1110,00011101
# @time:280-wr:1,0001,00000100-rd:1,0001,00000100
# ** Note: $finish    : C:/Users/Aadhithan/Documents/V
#    Time: 290 ps  Iteration: 0  Instance: /ram168_tb
```
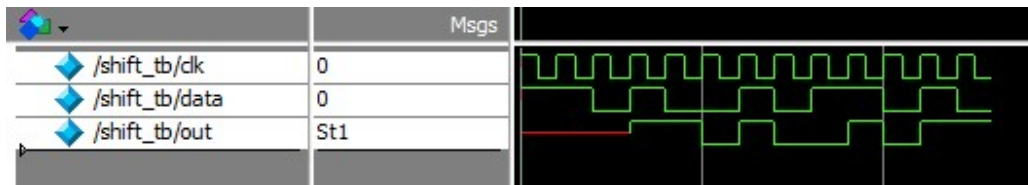
RTL:

Design : 8x16 Ram:

Wave:

Output:


```
VSIM 29> run -all
# @time:   0-wr:1,000,0000000000000001-rd:0,xxx,00000000xxxxxxxx
# @time:  15-wr:1,001,0000000000000011-rd:0,xxx,00000000xxxxxxxx
# @time:  30-wr:1,010,0000000000000101-rd:0,xxx,00000000xxxxxxxx
# @time:  45-wr:1,011,0000000000000111-rd:0,xxx,00000000xxxxxxxx
# @time:  60-wr:1,100,0000000000001001-rd:0,xxx,00000000xxxxxxxx
# @time:  75-wr:1,101,0000000000001011-rd:0,xxx,00000000xxxxxxxx
# @time:  90-wr:1,110,0000000000001101-rd:0,xxx,00000000xxxxxxxx
# @time:105-wr:1,111,0000000000001111-rd:0,xxx,00000000xxxxxxxx
# @time:120-wr:1,111,0000000000001111-rd:1,111,0000000000001111
# @time:130-wr:1,010,0000000000101011-rd:1,101,0000000000001011
# @time:140-wr:1,110,0000000000011111-rd:1,111,0000000000001111
# @time:150-wr:1,100,0000000000101111-rd:1,001,0000000000000011
# @time:160-wr:1,001,0000000001110010-rd:1,001,0000000001110010
# ** Note: $finish    : C:/Users/Aadhithan/Documents/Verilog_labs/1a
#    Time: 170 ps  Iteration: 0  Instance: /ram8x16_tb
```

RTL:

Too length to attach.
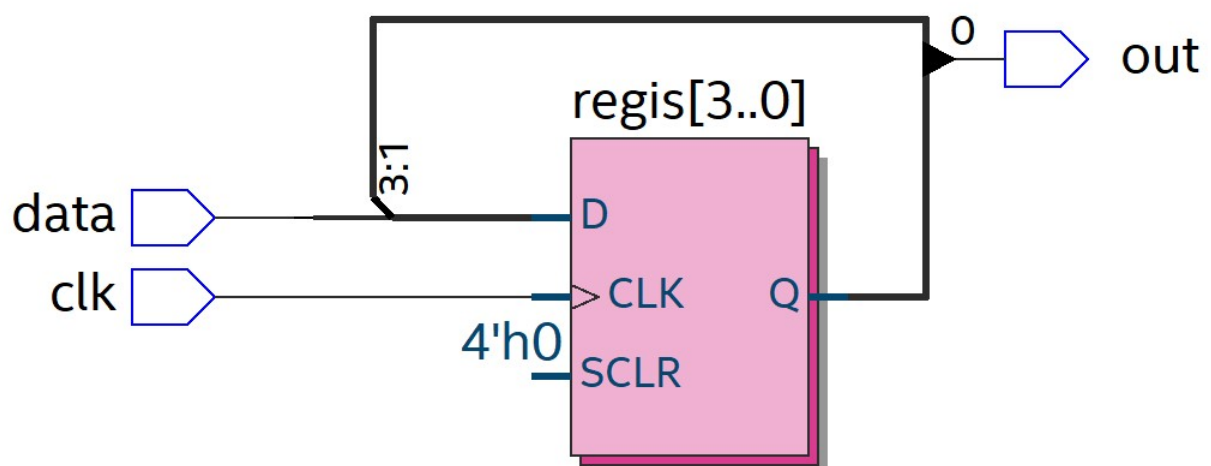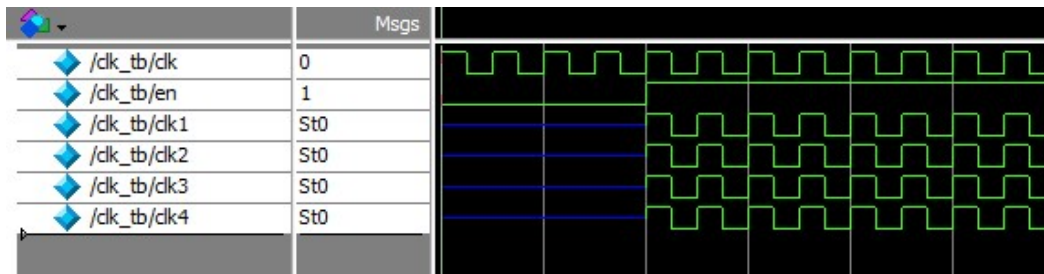
Design : 4 bit SISO

Wave:

Output:

```
VSIM 33> run -all
# @time:   0, in data is 1, out data is x
# @time:  20, in data is 0, out data is x
# @time:  30, in data is 1, out data is 1
# @time:  40, in data is 0, out data is 1
# @time:  50, in data is 0, out data is 0
# @time:  60, in data is 1, out data is 1
# @time:  70, in data is 0, out data is 0
# @time:  80, in data is 1, out data is 0
# @time:  90, in data is 1, out data is 1
# @time: 100, in data is 0, out data is 0
# @time: 110, in data is 1, out data is 1
# @time: 120, in data is 0, out data is 1
# ** Note: $finish    : C:/Users/Aadhithan/Documents/
#     Time: 130 ps  Iteration: 0  Instance: /shift_tb
```

RTL:

Design : Clock buffer:

Wave:

	Msgs
/clk_tb/clk	0
/clk_tb/en	1
/clk_tb/clk1	St0
/clk_tb/clk2	St0
/clk_tb/clk3	St0
/clk_tb/clk4	St0

Output:

```
VSIM 37> run -all
# @time:   0,in-clk:1,out-clk:z,z,z,z
# @time:   5,in-clk:0,out-clk:z,z,z,z
# @time:  10,in-clk:1,out-clk:z,z,z,z
# @time:  15,in-clk:0,out-clk:z,z,z,z
# @time:  20,in-clk:1,out-clk:z,z,z,z
# @time:  25,in-clk:0,out-clk:z,z,z,z
# @time:  30,in-clk:1,out-clk:z,z,z,z
# @time:  35,in-clk:0,out-clk:z,z,z,z
# @time:  40,in-clk:1,out-clk:1,1,1,1
# @time:  45,in-clk:0,out-clk:0,0,0,0
# @time:  50,in-clk:1,out-clk:1,1,1,1
# @time:  55,in-clk:0,out-clk:0,0,0,0
# @time:  60,in-clk:1,out-clk:1,1,1,1
# @time:  65,in-clk:0,out-clk:0,0,0,0
# @time:  70,in-clk:1,out-clk:1,1,1,1
# @time:  75,in-clk:0,out-clk:0,0,0,0
# @time:  80,in-clk:1,out-clk:1,1,1,1
# @time:  85,in-clk:0,out-clk:0,0,0,0
# @time:  90,in-clk:1,out-clk:1,1,1,1
# @time:  95,in-clk:0,out-clk:0,0,0,0
# @time:100,in-clk:1,out-clk:1,1,1,1
# @time:105,in-clk:0,out-clk:0,0,0,0
# @time:110,in-clk:1,out-clk:1,1,1,1
# @time:115,in-clk:0,out-clk:0,0,0,0
# ** Note: $finish    : C:/Users/Aadhithan/Document
5/clock/clk_tb.v(15)
#    Time: 120 ps  Iteration: 0  Instance: /clk_tb
```

RTL: