**Experiment 2**

**Aim:**

To write an ARM Assembly Language to load any register with 32 bit data and perform the following.

1. Shift left by 2 bit.
2. Shift right by number of bits stored in register.
3. Shift left 5 bits conditionally when ‘0’ flag is set.
4. Arithmetic Shift right by number of bits stored in register.

**Tool Used:**

Keil uVision4

**Theory:**

LSL shift the bits left and concatenate a 0 at the LSB. LSR shift the bits right and concatenate a 0 at the MSB. ASR shifts the bits right and concatenate the value of MSB at the new MSB.

**a) Shift left by 2 bit.**

**Code:**

AREA PROGRAM, CODE, READONLY

ENTRY

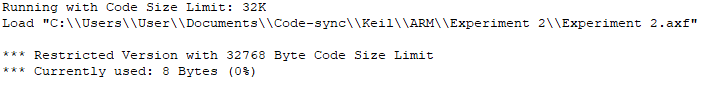
MAIN

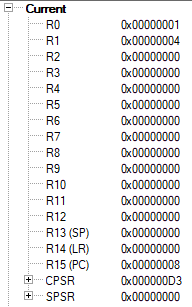
LDR R0,=0x00000001 ;LOAD R0 WITH VALUE 1

  MOV R1,R0,LSL#0x02 ;SHIFT 1 TWO TIMES AN STORE IN R1

  END

**Output:**

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****

The Value at R0 is 1 and it is shifted 2 times resulting in R1 to be 4.

The program Counter has the value 0x00000008 indicating that 2 32-bit instructions have been executed.

**b) Shift right by number of bits stored in register.**

**Code:**

AREA PROGRAM, CODE, READONLY

 ENTRY

MAIN

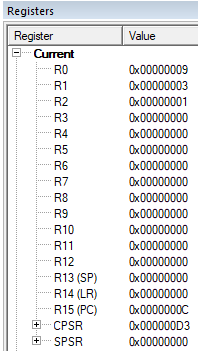
 LDR R0, =0x00000009 ;LOAD VALUE 9 TO R0 REGISTER

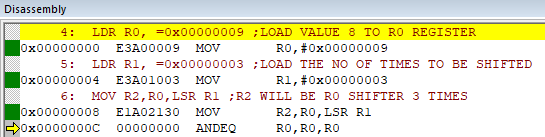
 LDR R1, =0x00000003 ;LOAD THE NO OF TIMES TO BE SHIFTED

 MOV R2,R0,LSR R1 ;R2 WILL BE R0 SHIFTER 3 TIMES

 END

**Output:**

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The value stored in R0 is 9 and it is shifted right 3 times resulting in a value of 1 at R2 where the lower bits are truncated.

**c) Shift left 5 bits conditionally when ‘0’ flag is set.**

**Code:**

AREA PROGRAM, CODE, READONLY

  ENTRY

MAIN

 LDR R0, =0x00000000 ;LOAD VALUE 0 TO R0 REGISTER

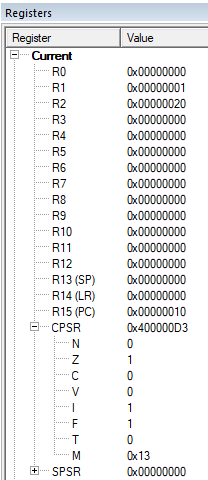
 LDR R1, =0x00000001 ;LOAD VALUE 3 TO R1 REGISTER

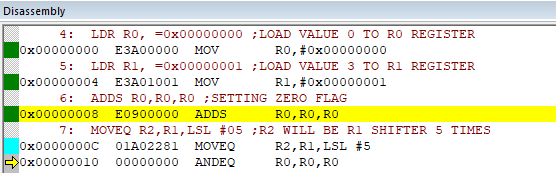
 ADDS R0,R0,R0 ;SETTING ZERO FLAG

 MOVEQ R2,R1,LSL #05 ;R2 WILL BE R1 SHIFTER 5 TIMES

 END

**Output:**

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The value stored in R1 is 1 and it is shifted 5 times resulting in a value of 20 at R2 as the Zero flag in CPSR is set to zero.

**d) Arithmetic Shift right by number of bits stored in register.**

**Code:**

AREA PROGRAM, CODE, READONLY

ENTRY

MAIN

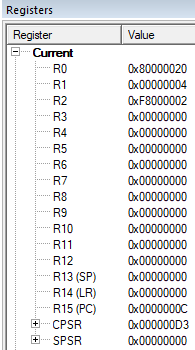
  LDR R0, =0x80000020 ;LOAD VALUE WITH MSB 1 TO R0 REGISTER

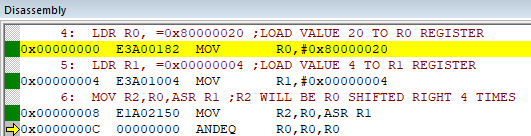
  LDR R1, =0x00000004 ;LOAD VALUE 4 TO R1 REGISTER

  MOV R2,R0,ASR R1 ;R2 WILL BE R0 SHIFTED RIGHT 4 TIMES

  END

**Output:**

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R0 has MSB as 1000\_0000 which is shifted right

4 times resulting in 1111\_1000(F8) in R2.

**Result:**

The experiments on shift operations have been performed and verified to be correct.