Experiment: CMOS and Resistive load Inverter Characteristics

PART-A

Aim:

To implement a CMOS inverter of level (1, 3 and 54) and analyze its transient and dc characteristics.

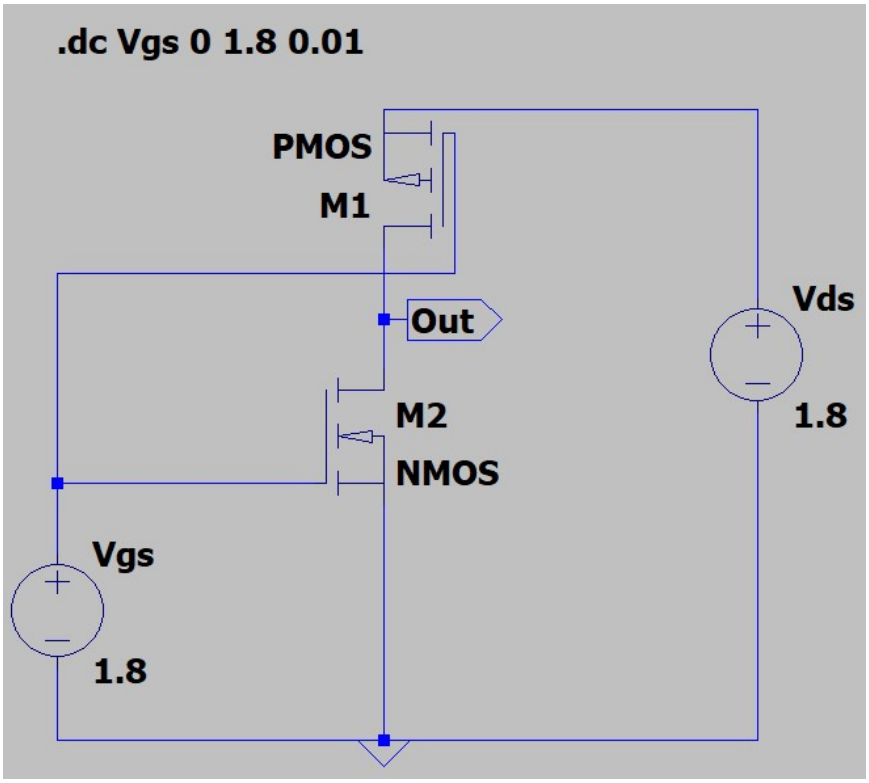
Tool Used:

LTspice

Theory:

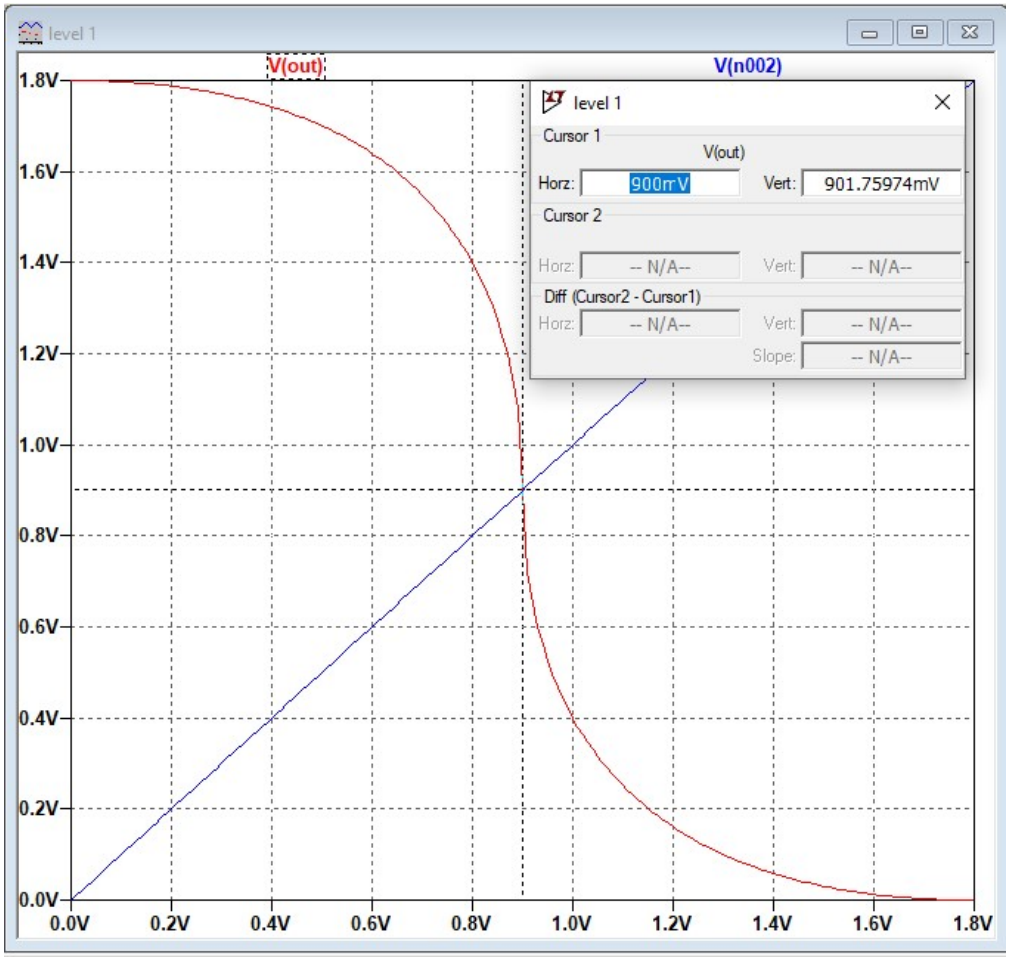
In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor. In CMOS inverter an n-type MOSFET acts as a pull-down transistor between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of Resistive Inverter, CMOS inverter has a p-type MOSFET in a pull-up transistor between the output and the higher-voltage rail (often named Vdd).

Circuit Schematic: [Level 1]

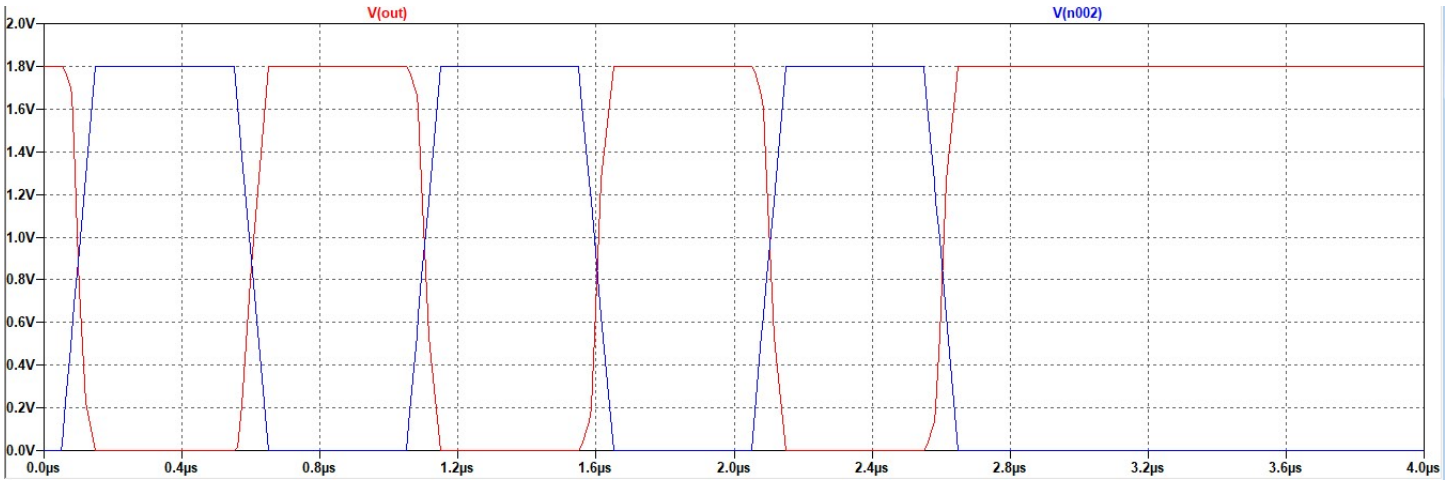


Output Waveforms:

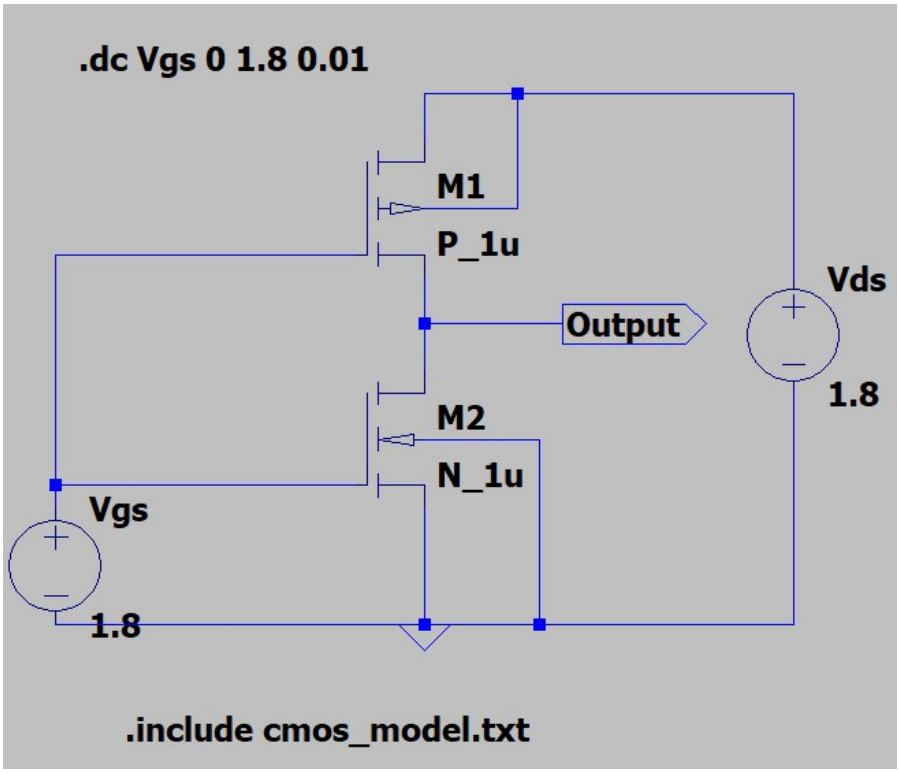
Dc Transfer characteristics (Vgs vs. Vout)



Transient characteristics

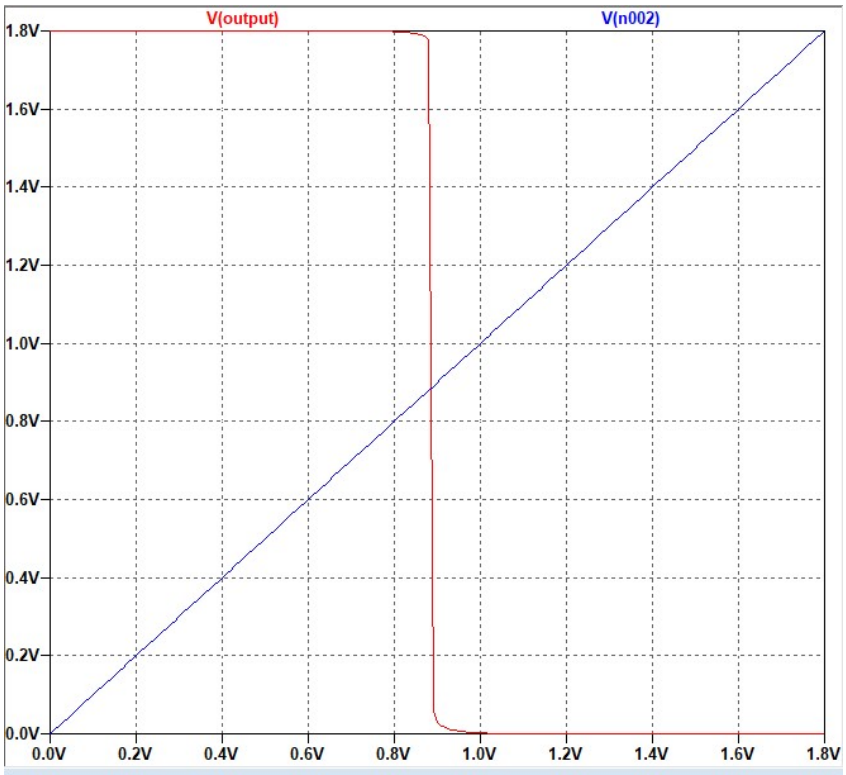


Circuit Schematic: [Level 3]

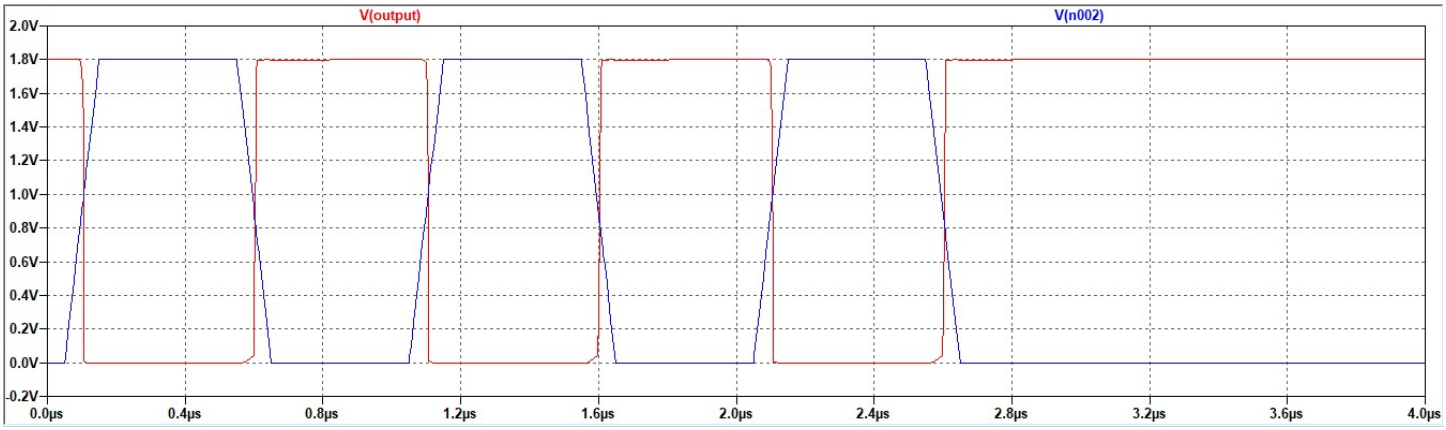


Output Waveforms:

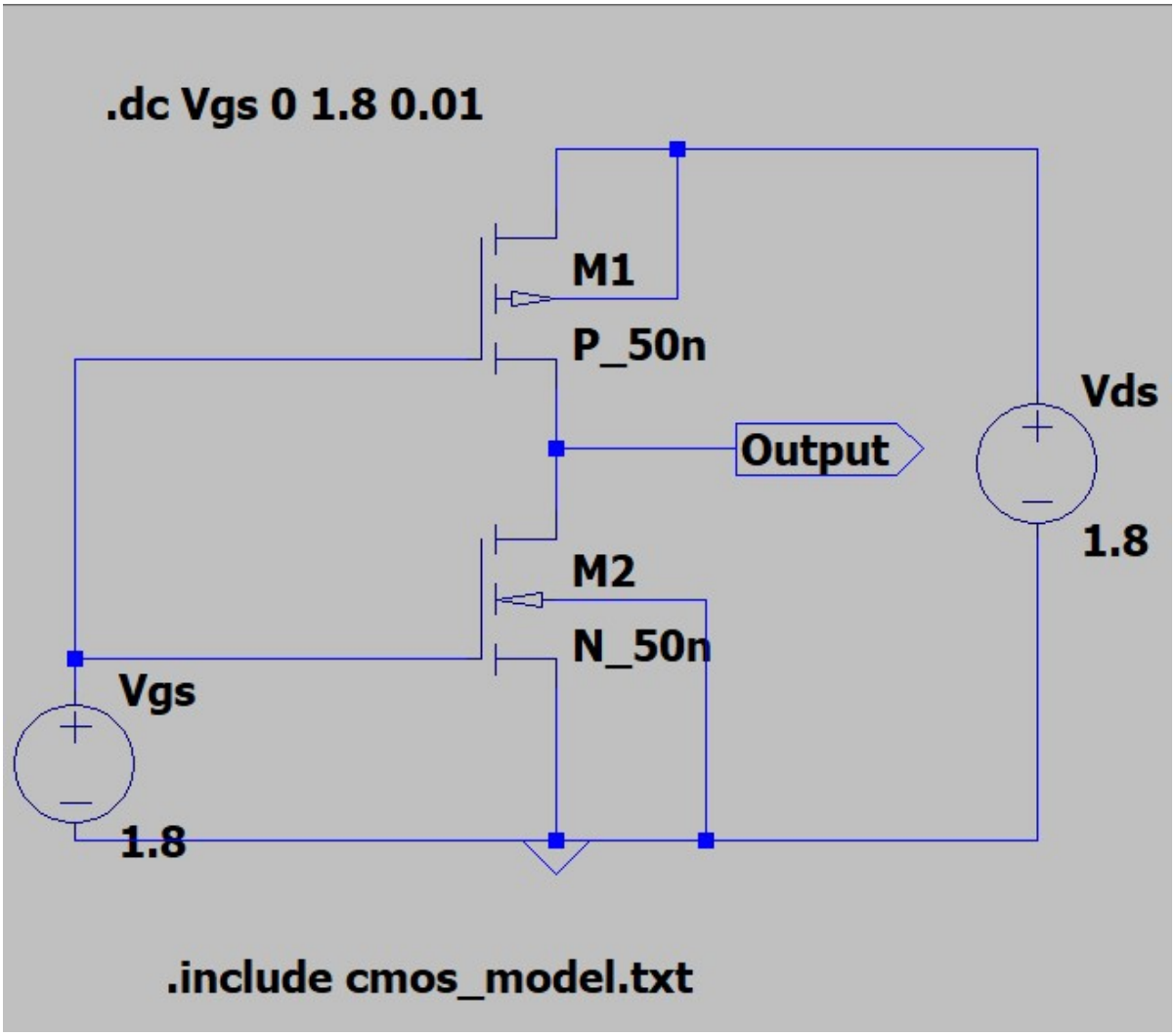
Dc Transfer characteristics (Vgs vs. Vout) for $(W/L)_p / (W/L)_n = 5$



Transient characteristics

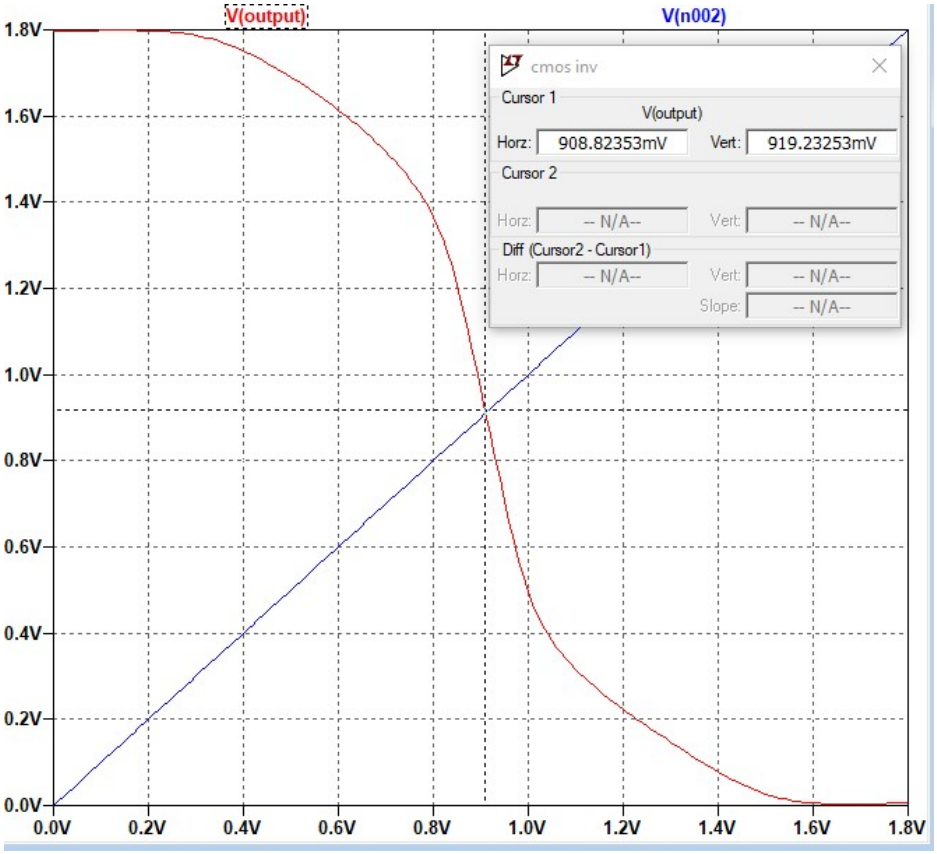


Circuit Schematic: [Level 54]

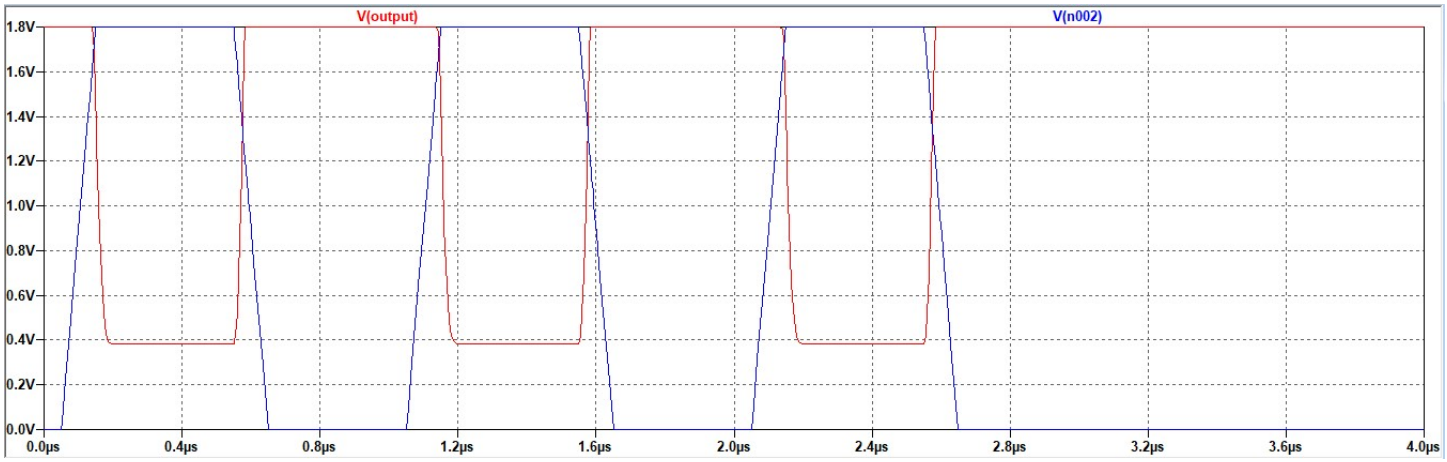


Output Waveforms:

Dc Transfer characteristics (Vgs vs. Vout) for $(W/L)_p / (W/L)_n = 2.2$



Transient characteristics



Result:

The circuit is stimulated for 3 levels of CMOS inverter and the transient and dc characteristics are visualized.

PART-B

Aim:

To implement a Resistive Load inverter and analyze its transient and dc characteristics.

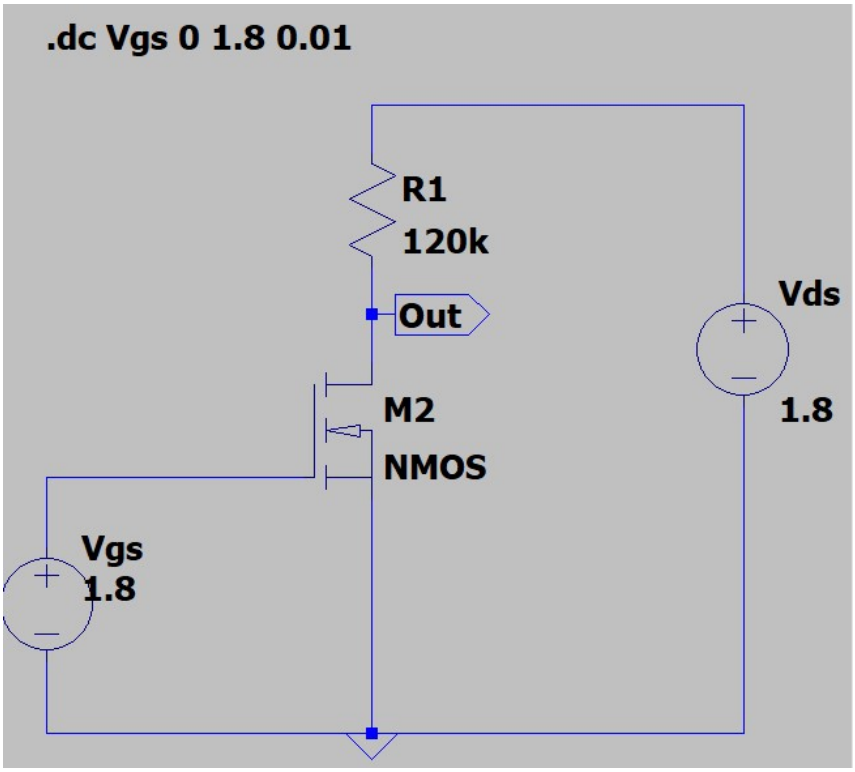
Tool Used:

LTspice

Theory:

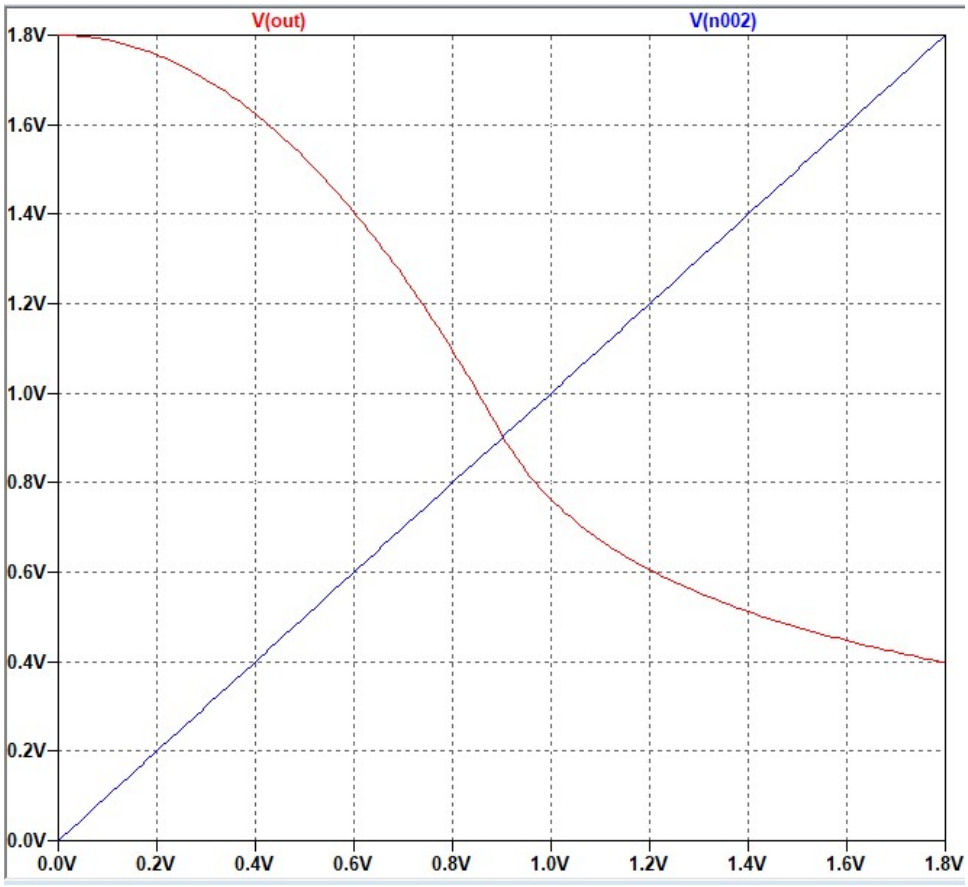
The basic structure of a resistive load inverter is shown in the figure given below. Here, enhancement type nMOS acts as the driver transistor. The load consists of a simple linear resistor RL. The power supply of the circuit is VDD and the drain current ID is equal to the load current IR. When the input of the driver transistor is less than threshold voltage VTH (Vin < VTH), driver transistor is in the cut – off region and does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to the VDD. Now, when the input voltage increases further, driver transistor will start conducting the non-zero current and nMOS goes in saturation region.

Circuit Schematic:

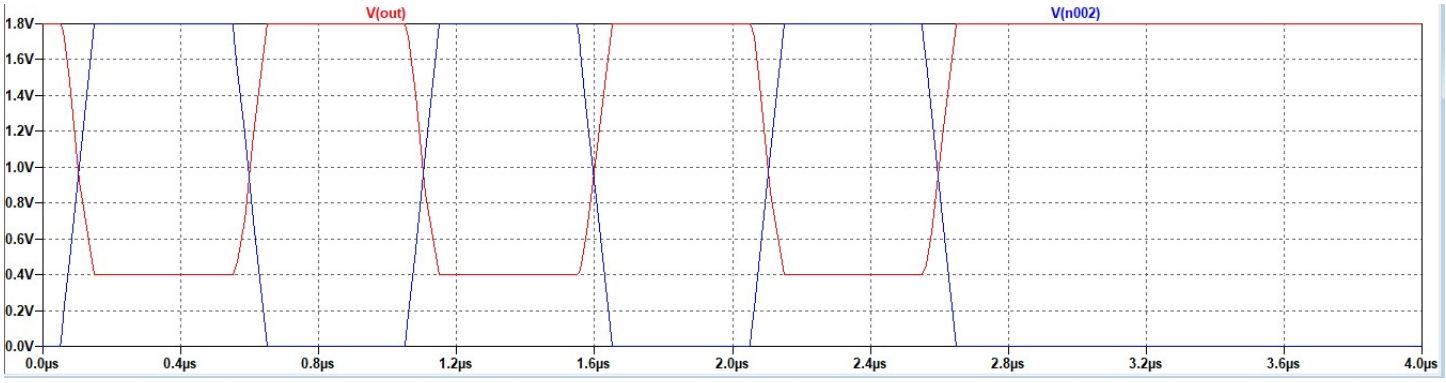


Output Waveforms:

Dc Transfer characteristics (Vgs vs. Vout)



Transient characteristics



Result:

The circuit is stimulated with 120k resistor and the transient and dc characteristics are visualized.