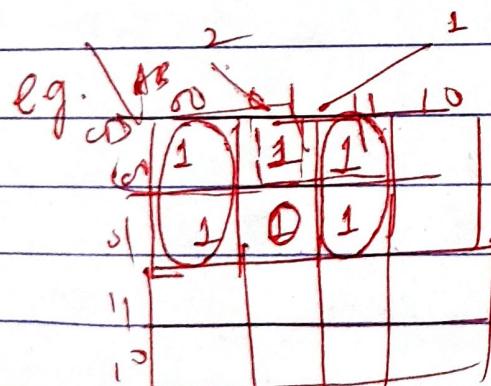
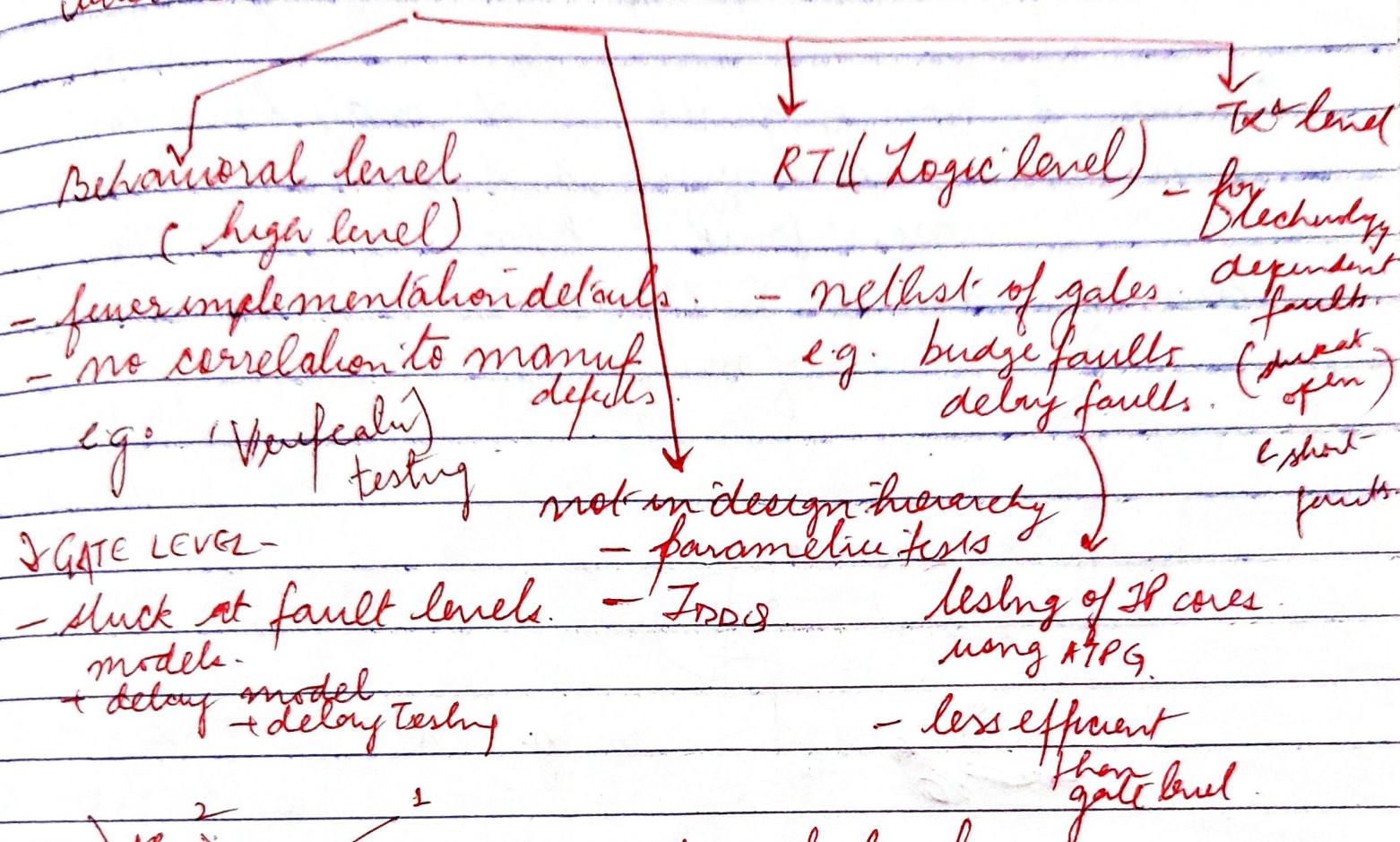


Fault modeling: models used to bridge gap b/w physical reality & mathematical abstraction

Fault models can be at diff. levels of abstr. abstraction:



physical level
→ interconnects
→ R.C., R.L.C. models
used to analyze Crosstalk problems

$$\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{C}\bar{D}(1)$$

or

$$\bar{A}\bar{B}\bar{C} + AB\bar{C} + \bar{A}\bar{C}\bar{D}(0)$$

Fault Models → stuck at faults
Bridging
pattern inscribe

A good fault model should satisfy 2 criteria

- reflect the behavior of defects.
- computationally efficient

Assume k types of faults. & ckt may have 'n' possible sites assuming a single fault model

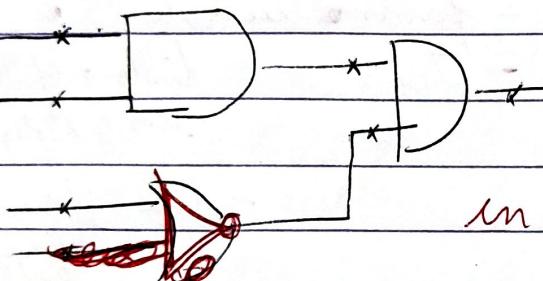
No. of faults = $k \times n$. assumes only one fault at a time (SIMPLE)

but for multiple faults.

$$\text{No. of multiple faults} = (k+1)^n - 1$$

takes into account fault free set

(DIFFICULT TO SIMPLY COMPLEX)



in general 100% single FC
 $\Rightarrow 98\%$ multiple F.C.

$$2 \times 6 = 12$$

$$(3)^6 - 1$$

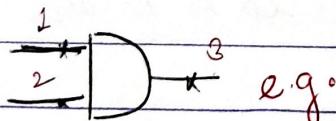
F.C.

single faults.

$$= 9 \times 9 \times 9 - 1$$

$$= 81 \times 9 - 1$$

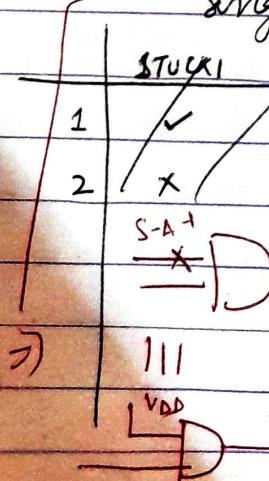
$$= 729 - 1 = 728$$



$$\text{Single} = 2 \times 3 = 6$$

$$\text{multiple} : (2+1)^3 - 1 \rightarrow$$

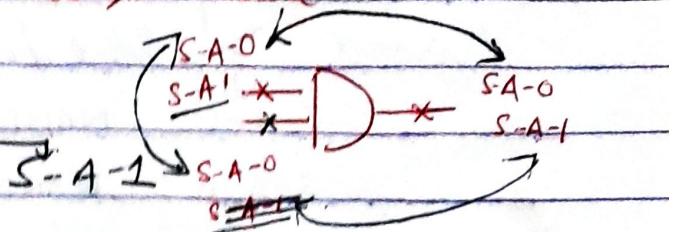
$$= 87 - 1 = 86$$



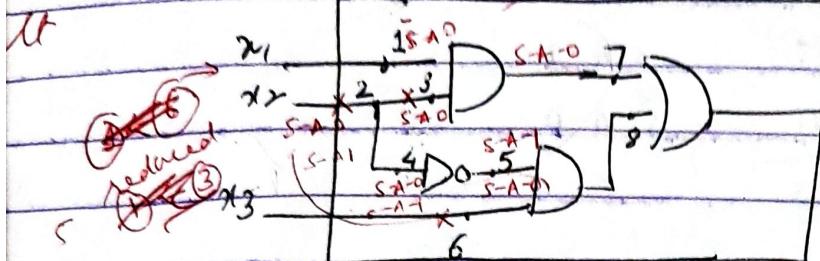
	1	2	3		1	2	3
STUCK-1	✓			S-1	x	x	
STUCK-0	x			S-0	x	x	
S-A ¹	x			x	s-1	x	
				x	s-0	x	
				x	s-1	x	
				x	s-0	x	
				x	s-1	x	
SIMPLE	x			x	s-1	x	
				x	s-0	x	
				x	s-1	x	

Equivalent faults: faults which result in identical behavior
fault collapsing: process of removing eqt faults.
reduce the no. of faults to simulate.

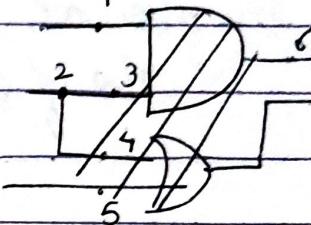
STUCK AT FAULTS



∴ no of collapsed
faults = 1

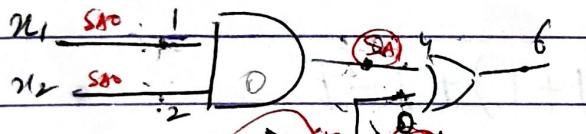


$$\frac{q}{\text{reduced}} = 2$$

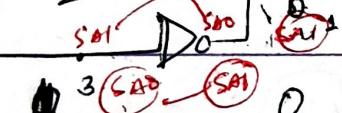


$$\begin{aligned}\text{collapsed faults} &= 2(1+0) + 5 - 1 \\ &= 7 - 1 = \textcircled{6}\end{aligned}$$

1) 001, 010, 011, 101, 111



needed



1

Identify test vectors — which give 100% coverage

$$2 \times (1+3) + \frac{12}{2} = 8 + 12 = 20$$

Find fault equivalence.

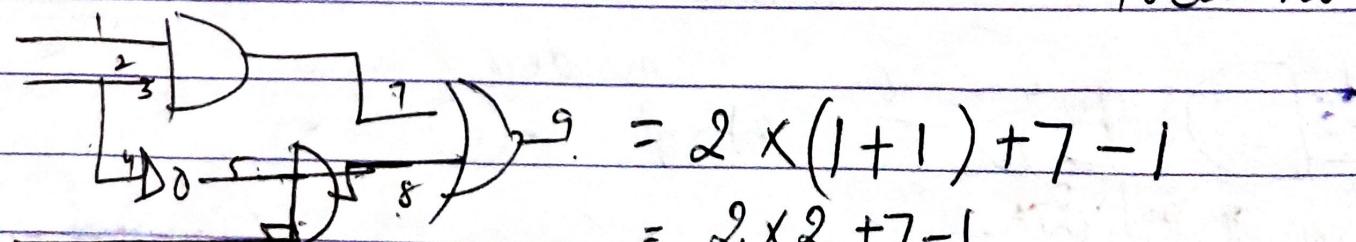
Based on the fact that

S-A-0	NAND	S-A-1
S-A-0	AND	S-A-0
S-A-1	OR	S-A-1
S-A-1	NOR	S-A-0
S-A-0	NOT	S-A-1
S-A-1	NOT	S-A-0

In general

No of collapsed faults

$$\begin{aligned} &= 2 \times (\text{No. of P0s} + \text{No. of fanouts}) \\ &\quad + \text{total no of gates } \text{APs} \\ &\quad - \text{total no of inverters} \end{aligned}$$



$$= 2 \times (1+1) + 7 - 1$$

$$= 2 \times 2 + 7 - 1$$

$$= 4 + 7 - 1 = 10$$

(min faults to be detected)

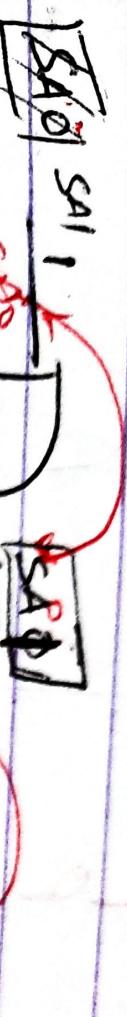
fault collapsing ratio

$$= \frac{\text{Set of collapsed faults}}{\text{Set of all faults}}$$

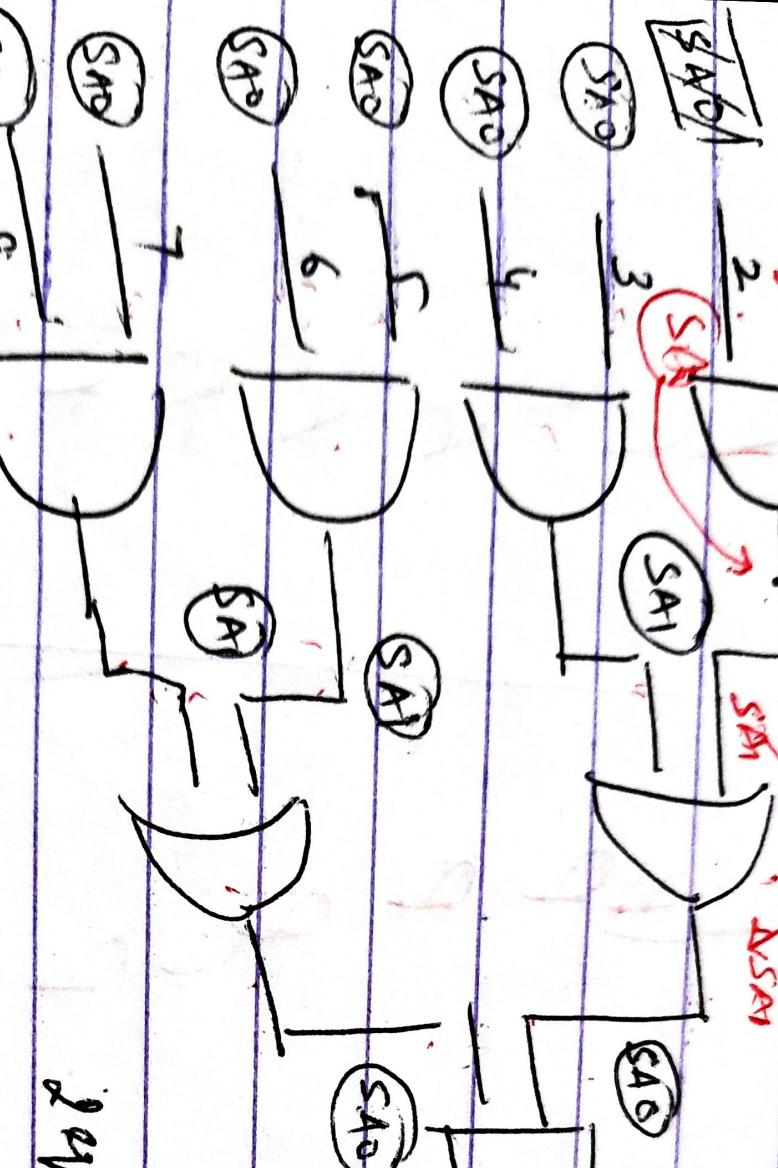
$$\frac{16}{30}$$

$$2(1 +$$

= 2(1+2) + 1 = 7



= 2(1+2) + 1 = 7



2nd. Inspection:

15x2230

6x1

4x1

2x1

3rd. 3x1

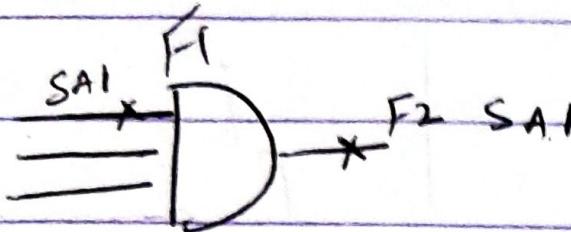
8x1

1x1

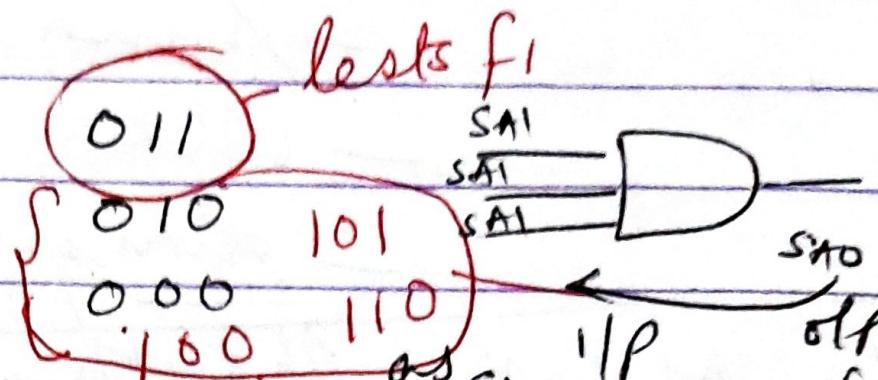
$$\text{fault dominance} = 2(1+0) + 14 = 16$$

$$\text{Form} = 2(1+0) + 12 - 0$$

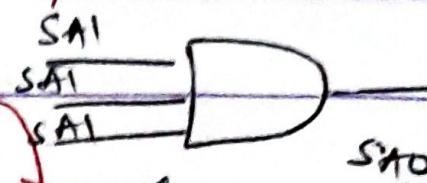
when test vector containing Fault F1 is subset of test vector for fault F2 \Rightarrow F2 is said to dominate F1 if 2 faults dominate each other i.e. all tests detecting F1 detect F2 also & vice-versa \Rightarrow F1 & F2 are equivalent.



Dominance fault



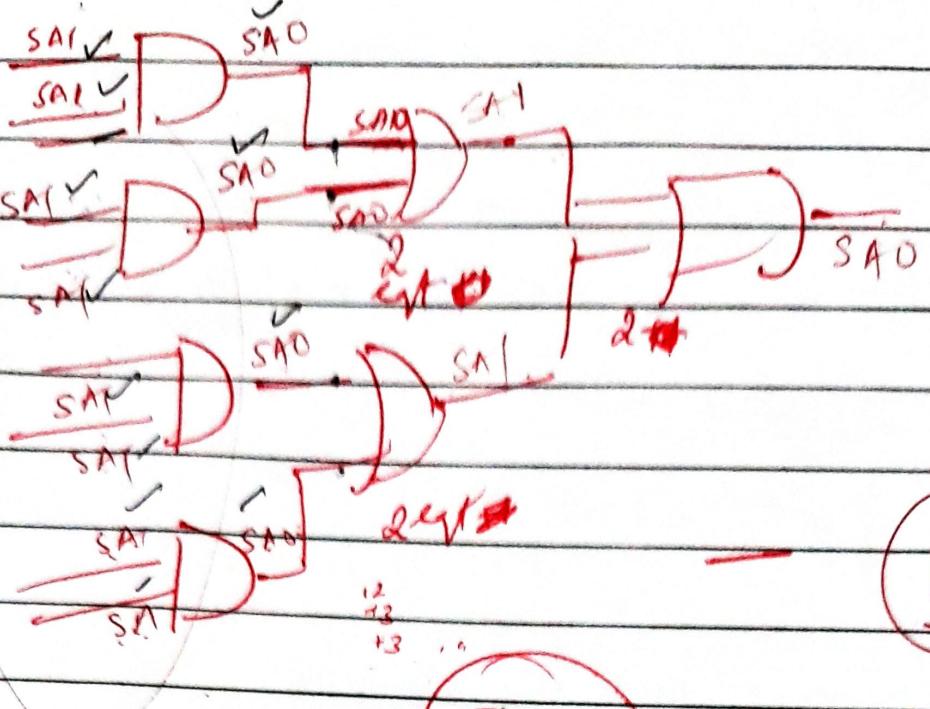
tests f1



as SAO is same for all 1/f's.

n/l gate req n/l fault model

all test F2



91412

13

$$12 + 4 + 2$$

salvo

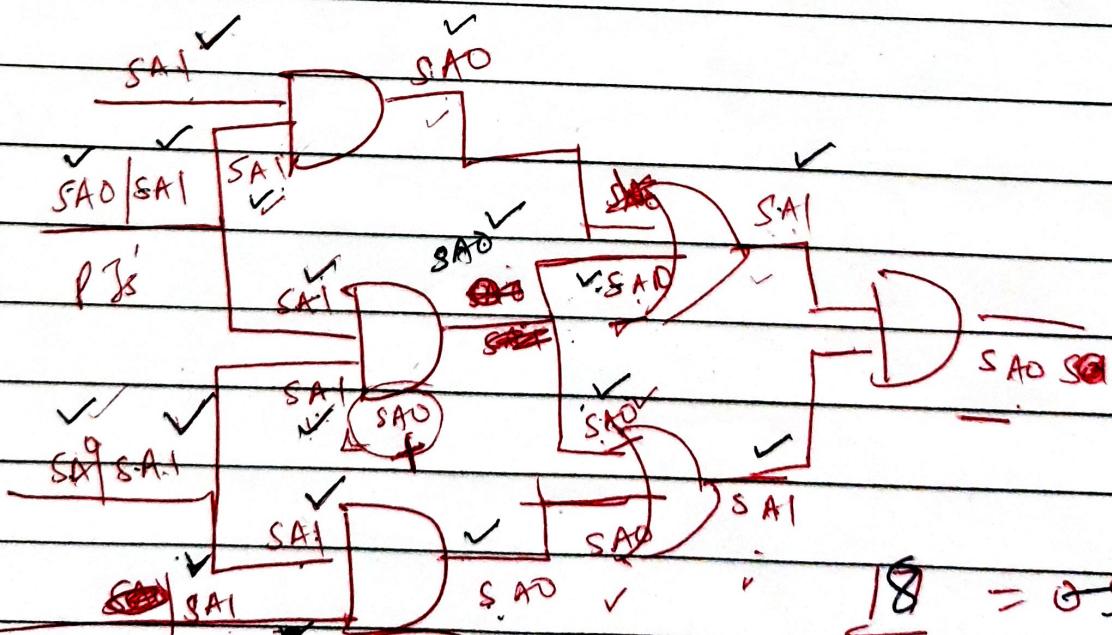
~~12~~
~~30~~

reduced

12
30

huswif 0-5

and except there



$$\underline{18} = \underline{0}\underline{5}3$$

~~check pt~~

$$\cancel{6+4+3}$$

~~17~~
~~32~~

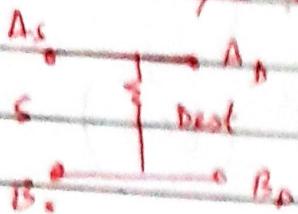
Checkit theorem

PI & fanout branches



BRIDGING FAULTS

→ short b/w 2 elements - BRIDGING FAULT



interconnecting wires to Xistor if open will be same as stuck-open Xistor fault.

& if open occurs b/w gates it becomes as stuck a fault.

But a resistive open cannot be modeled as stuck open / stuck at fault & rather effects the delay of path.

Q - When 2 signal wires are shorted

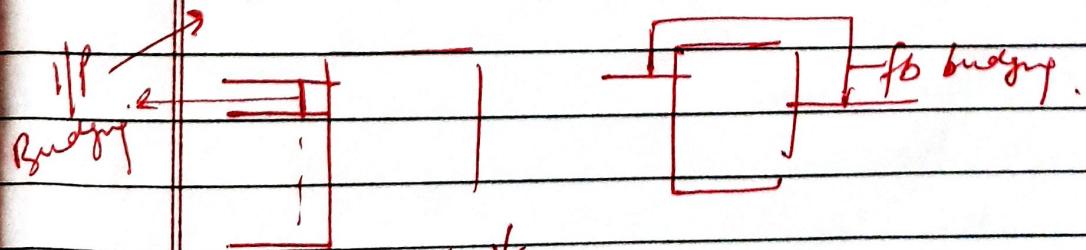
- depends on :
1) Technology
2) location of faults.
3) Extensiveness of fault.

Theoretically, if circuit has n lines

→ $\frac{n(n-1)}{2}$ BRIDGING FAULTS assuming
it to be b/w any 2 pairs -

though actually it is always less bcz
bridging fault occurs b/w adjacent lines.

INPUT BRIDGING



- resolution needs use of wired-AND, wired-OR model.

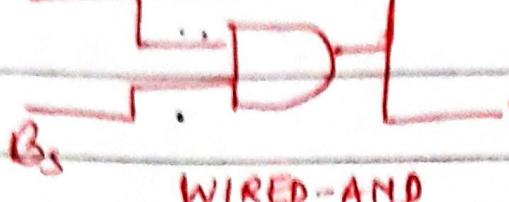
WOR
Reflection of Bridging fault -

1/P	Q/P	Q/P
00	00	00
01	00	01
10	00	10
11	11	11

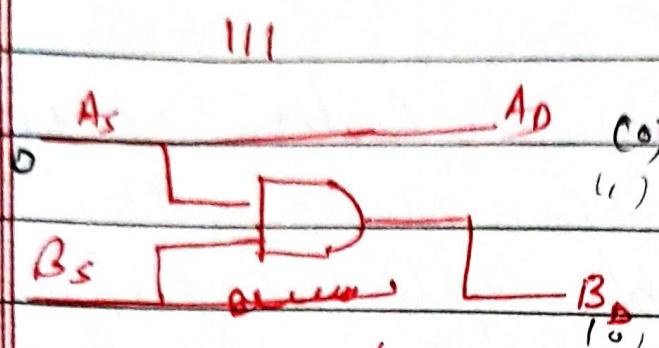
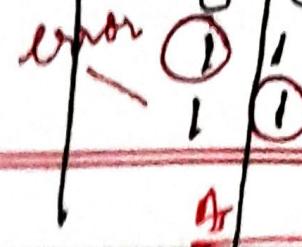
Error.

expected

WAND

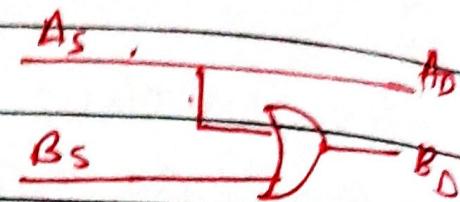


WIRED-AND



DOMINANT 'A' WIRED AND

(TTL)



DOMINANT 'A' OR
may
(ECL)

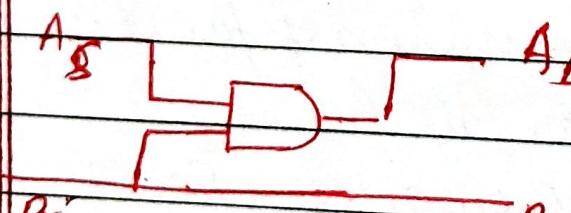
but for CMOS (inverter based)

any I/P stuck at '1', makes diff.

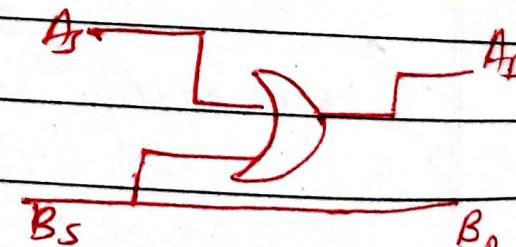
- DOMINANT AND or DOMINANT OR

or

~~Show~~



B DOMINANT AND

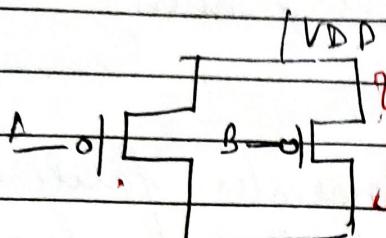


TRANSISTOR FAULTS: -

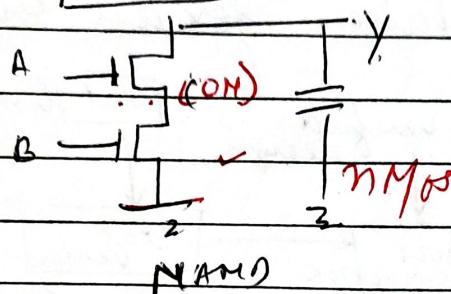
Date _____
Page _____

a Txr can be stuck open ($I_{DDQ} \neq 0$) or (ON)

stuck short - lead
(OFF) (building of a
memory cell)



PMOS $A=1$, so logic not
depends on B.



$A=0$, $Y=1$

Further for series Txrs. stuck off is eqt.
/ / / el stuck on faults are eqt.

∴ Collapsed faults

$$= 2T - \underline{N_{A\text{st}} + G_{A\text{st}}} - \underline{N_{B\text{st}} + G_{B\text{st}}}$$

e.g.

$$= 2 \times 4 - 2 + 1 - 2 + 1 \\ - 8 - 4 + 2 = 6$$

These faults are.

PMOS A - ON \equiv PMOS B on.

PMOS A - OFF

PMOS - B - off.

NMOS A - OFF \equiv NMOS B off

NMOS A - ON =

NMOS - B ON

stuck ON faults - I_{DDQ} testing.

stuck off, wrong off logic & needs
J/P vectors for tests