**EDCHC: Error Detection and Correction based on Hamming Code**

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**Introduction on Hamming code:**

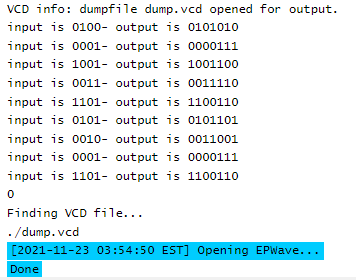
Hamming code makes use of the concept of [parity](https://searchstorage.techtarget.com/definition/parity) and [parity bit](https://searchstorage.techtarget.com/definition/parity)s, which are bits that are added to data so that the validity of the data can be checked when it is read or after it has been received in a data transmission. Using more than one parity bit, an error-correction code can not only identify a single bit error in the data unit, but also its location in the data unit.

In this paper we will be first designing a circuit to generate hamming code, then one more design to detect and correct a single bit error.

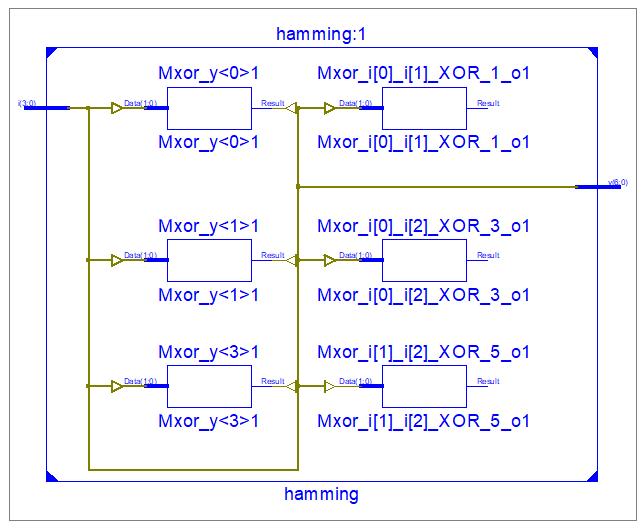
**Code Generator:**

First we implement a module which can generate a 7 bit hamming code output for a 4 bit hamming code input. The source codes of the DUTs and Test benches could be found in <https://github.com/raja-aadhithan/M.Tech_Verilog/tree/main/Hamming>

**The output of the generator is:**



**RTL of the DUT:**

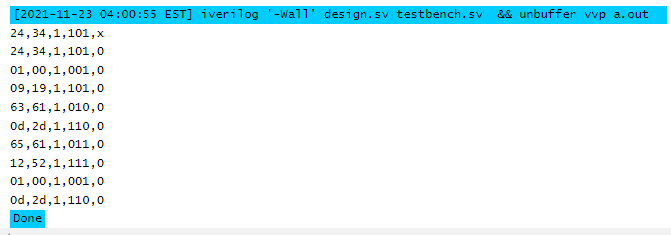


**Error Detection and Correction:**

The error detection DUT could detect if one bit is manipulated and can restore its value, but if more than 1 value are changed, the output will still show a valid hamming code but not the original one.

The output also shows the position at which the bit was wrong.

**Simulation output:**



**RTL of the error corrector:**

