**Verilog code to implement Sequence detector(1001) using Moore style**

**Design Code:**

module moore(input i,clk,rst, output reg y);

    reg [2:0] state,next\_state;

    parameter idle=3'b000, s1=3'b001, s10=3'b010, s100=3'b011, s1001=3'b100;

    always@(\*)begin

        case(state)

            idle    : next\_state = i ? s1   : idle;

            s1      : next\_state = i ? s1   : s10;

            s10 : next\_state = i ? s1   : s100;

            s100    : next\_state = i ? s1001: idle;

            s1001   : next\_state = i ? s1   : s10;

        endcase

    end

    always@(posedge clk) begin

        if (rst == 1) begin

            state = idle;

            y <= 1'b0;

        end

        else begin

            state = next\_state;

            y <= (state==s1001);

        end

    end

endmodule

**Test Bench:**

module tb();

    reg i,clk,rst;

    wire y;

    moore dut(i,clk,rst,y);

    initial begin

        clk = 1'b1;

        forever #5 clk = !clk;

    end

    initial begin

        rst = 1'b1;

        #10;

        @(negedge clk)

        rst = 1'b0;

        i = 1;

        @(negedge clk) i = 0;

        @(negedge clk) i = 0;

        @(negedge clk) i = 1;

        @(negedge clk) i = 1;

        @(negedge clk) i = 0;

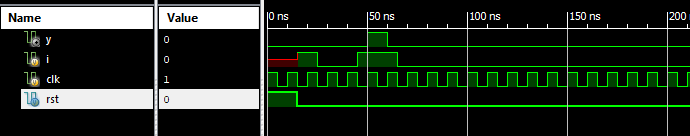
        @(negedge clk) i = 0;

        @(negedge clk) i = 0;

    end

endmodule

**Simulation Result:**

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**RTL Diagram:**

