RTL Design of a MATLAB Model

A PROJECT REPORT

Submitted by

T RAJA AADHITHAN

in partial fulfillment for the award of the degree

of

Master of Science

in

ELECTRONIC SCIENCE

DEPARTMENT OF ELECTRONIC SCIENCE

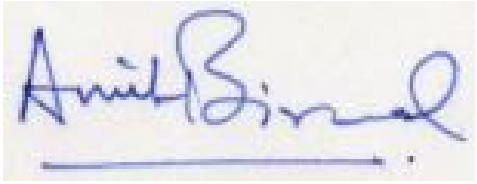
UNIVERSITY OF DELHI

MAY 2021

DEPARTMENT OF ELECTRONIC SCIENCE
University of Delhi, South Campus
Benito Juarez road, New Delhi 110021, India

CERTIFICATE

This is to certify that **Mr. T Raja Aadhithan,** student of University of Delhi has successfully completed his project work entitled **"RTL Design of a MATLAB Model"** under the partial fulfillment of his Master's degree (M.Sc) in Electronics from the Department of Electronic Science, **University of Delhi, South Campus, New Delhi**. This report embodies original work of the candidate. It has been carried out under our guidance and supervision and is to the satisfaction of the department.



Mr. Amit Birwal
Assistant Professor
(Project Guide)
Department of Electronic Science,
University of Delhi South Campus.

Prof. Mridula Gupta
(Project Coordinator)
Department of Electronic Science,
University of Delhi South Campus.

Prof. Mridula Gupta
(Head of the Department)
Department of Electronic Science,
University of Delhi South Campus.

Candidate's Declaration

I hereby declare that the project entitled "**RTL Design of a MATLAB Model*"***, is carried out by me during the month January 2021 to June 2021 in partial fulfillment of the award of ***Master of Science*** with specialization in ***Electronics Science*** from ***Department of Electronic Science, University of Delhi, South Campus***, New Delhi, India. I have not submitted the same to any other University or organization for the award of any other degree.

Place: Dindigul
Date: 31-May-2021

Name: T Raja Aadhithan
Roll No: 3977

ACKNOWLEDGEMENT

I would like to express my special thanks of gratitude to my project guide Mr. Amit Birwal as well as our head of Department Prof. Mridula Gupta who gave me the golden opportunity to do this wonderful project on the topic RTL design of MATLAB Model, which also helped me in doing a lot of research and I came to know about so many new things I am really thankful to them.

Secondly I would also like to thank my parents and friends who helped me a lot in finalizing this project within the limited time frame.

Date : 29 May 2021

Name : T Raja Aadhithan

Place : Dindigul

Roll No : 3977

TABLE OF CONTENTS

ABSTRACT

In this Project a production proven path is taken on a MATLAB digital signal processing algorithm through Simulink fixed point designer and HDL coder to target an FPGA.

Verilog from MATLAB functions, Simulink models and state flowcharts that can be used to target FPGA or ASIC hardware MATLAB is a high-level language an interactive environment a complex mathematical operations can be easily performed on large sets of data. This ability of MATLAB makes it an ideal tool to develop digital signal processing algorithms to target such a powerful language onto Hardware.

We need to understand that the FPGA hardware is a fixed set of resources. The FPGA hardware has limited bandwidth of resources consisting of input/output blocks memory and DSP slices which must be effectively used to achieve an optimized design architecture while achieving the desired outcome. As resources are fixed in Hardware to perform operations on large datasets we will work on stream of bits while coordinating the timing to obtain the right answer.

Simulink provides an environment where you can describe how the algorithm design will work with a stream of data and simulate before moving to Hardware implementation. Simulink has a built-in sense of time and aids in visualizing the data types and sizes propagation through operations which are key to creating a good hardware architecture, It also has a HDL optimized library with more than 250 blocks and compatible with HDL code generation thus to deploy the MATLAB algorithm on an FPGA. The performed workflow is to use MATLAB and Simulink together to combine textual and graphical programming in a simulation environment.

1. INTRODUCTION

A MATLAB algorithm is used as a golden reference which describes the hardware architecture in Simulink. Simulink then converts to fixed point and utilize Simulink visualization to optimize the generated HDL code. Thus each step in Simulink can be verified in MATLAB and utilizes MATLAB as a test and visualization environment.

In the MATLAB reference script the pulse to detect is created and is inserted. In a transmitted signal noise is added to represent a real-world receive signal to detect the pulse in MATLAB we will utilize the entire frame of the receive signal and pass it through a match filter with decided coefficients. This algorithm will be our MATLAB golden reference which will detect the peak value and its location.

Hardware works on a continuous stream of bits and peak detection is obtained by sliding a window over a sample of the bit stream to ensure this method gives us the desired result. We create a MATLAB algorithm which represents the hardware implementation and we will call as the hardware friendly algorithm. The hardware implementation algorithm detects the peak within a sliding window of the last 11 samples under the criteria the middle sample is the largest and the middle sample is greater than a predetermined threshold this algorithm will be utilized to verify and compare the output of the Simulink model.

BLOCK DIAGRAM OF PROJECT FLOW: