Experiment #4

Aim: Write the SystemVerilog testbench code for 256 word memory. Use the concept of StemVerilog "interface".

Memory has following ports:

Input ports: clk, rst, ce

Input ports: datai, addr of 8bits

Output port: datao of 8-bit size.

1. Write the SV code for interface.
2. Write the SV code for Memory with interface i.e. DUT with interface.
3. Write the SV testbench to perform the write operation (store 10 random values in the locations with address 0, 1,2….9. Also perform the read operations to display the content written in the memory during write operation.