Experiment #1

Aim: Familiarization with SystemVerilog *data types and arrays.*

1. Write the SystemVerilog code to:
   - **i.** Declare a 2-state array, my_array, that holds four 12-bit values
   - **ii.** Initialize my_array so that:
     my_array[0] = 12'h012
     my_array[1] = 12’h345
     my_array[2] = 12'h678
     my_array[3] = 12’h9AB
   - **iii.** Traverse my_array and print out bits [5:4] of each 12-bit element
     - **a.** With a for loop
     - **b.** With a foreach loop
2. Write the SystemVerilog code to:
   - **i.** Declare a 2-state two dimensional array, array_2d (4 rows and 3 columns), that holds 12 integer values.
   - **ii.** Initialize my_array so that:
     array_2d[0][0] = 0
     array_2d[0][1] = 1
     array_2d[0][2] = 2
     array_2d[1][0] = 3
     array_2d[1][1] = 4
     array_2d[1][2] = 5
     array_2d[2][0] = 6
     array_2d[2][1] = 7
     array_2d[2][2] = 8
     array_2d[3][0] = 19
     array_2d[3][1] = 20
     array_2d[3][2] = 21

   - **iii.** Print out the values stored in array_2d and verify them with initialized values. Hint: use foreach loop.