Experiment #7

Aim: Write the System Verilog testbench for the 8-bit adder with monitor and scoreboard.

Follow the following steps for the development of SV testbench for the adder design.

1. Write SV code for the adder

2. Write SV interface for DUT.

3. Write the SV class for packet-class (also called transaction class)

4. Write the SV class for generator block.

5. Write the SV class for driver block.

6. Write the SV class for monitor block.

7. Write the SV class for scoreboard block.

8. Write the SV class for environment block.

9. Write SV testbench with program block

10. Write SV code for testbench top to connect the interface, testbench and DUT. Run it and check the output.