Experiment #5

Aim: Familiarization with SystemVerilog task, function and void function.

1. Write the SV "task" code for the addition of two integer numbers and check it correctness.

2. Observe the difference between simple and automatic tasks:
   a. Write a simple task which increments the value of a local variable by a specified amount.
   b. Write an automatic task which increments the value of a local variable by a specified amount.

      Hint: You can write a simple task which increments the value of a local variable by a specified amount.

3. Demonstrate the difference between static and automatic variables used in SV task.
   →Write the following SV code and simulate it. Study the output and comment on it.

```
module auto_variable_task;

  task auto_example (input time delay);
    // Initialize the variables
    logic static_var = 1'b0;
    automatic logic auto_var = 1'b0;

    // Display the values at start of task
    $display("Entering task at %0tns", $time);
    $display("Automatic variable = %0d", auto_var);
    $display("Static variable = %0d", static_var);

    // Wait the given time and invert the signals
    #delay
    static_var = ~static_var;
    auto_var = ~auto_var;

    // Display the values at end of task
    $display("Task completed at %0tns", $time);
    $display("Automatic variable = %0d", auto_var);
    $display("Static variable = %0d", static_var);
  endtask : auto_example

  // Call the task 3 times to see how it behaves
  initial begin
    repeat (3) begin
      auto_example(10ns);
    end
  end

endmodule : auto_variable_task
```

4. Write the code using SV "**function"** for the addition of two integer numbers.

5. Write the SV **void function** to print the current simulation time. Check its corrections.