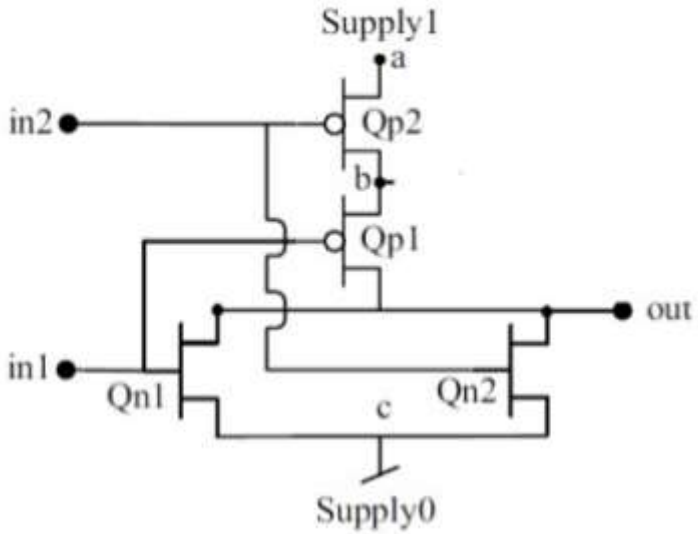
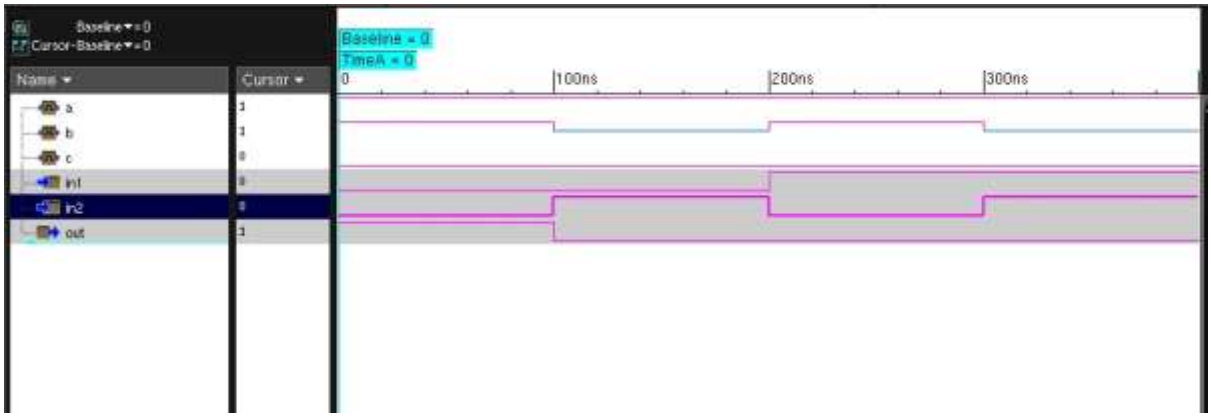
CMOS NOR GATE



RTL SCHEMATIC VIEW

SIMULATION RESULT:



Expt.No.: 8a.	**Design and Simulation of a CMOS Basic Gates & Generate Manual/Automatic Layout Using Cadence Virtuoso**
Date:	

AIM:

To write a Verilog code for CMOS basic gates and to perform simulation, synthesis, analyze the power, area and timing report by performing pre layout and post layout simulations in Cadence Virtuoso Tool.

OBJECTIVES:

On completing this experiment, the students will be able to

1. Design CMOS basic gates using Verilog code Hardware description language.
2. Simulate, synthesis, analyze the power, area and timing report by performing pre layout and post layout simulations in Cadence Virtuoso Tool.

APPARATUS REQUIRED:

Sl.No.	Name of the Apparatus	Quantity
1	PC	1
2	Cadence Virtuoso Software	-

THEORY:

Combinational Logic circuits that change state depending upon the actual signals being applied to their inputs at that time, Sequential Logic circuits have some form of inherent "Memory" built in.

This means that sequential logic circuits are able to take into account their previous input state as well as those actually present, a sort of "before" and "after" effect is involved with sequential circuits.

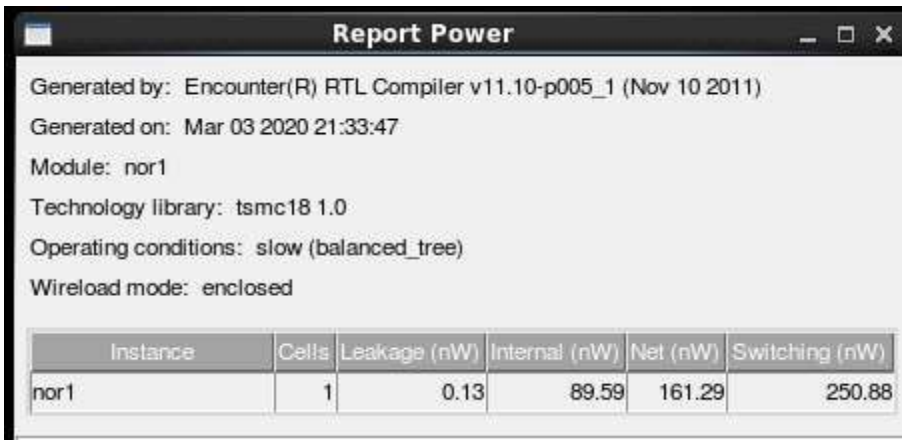
The AND Gate:

The AND gate outputs a logical 1 if and only if all inputs are a logical 1 and outputs 0 otherwise.

The NAND Gate:

The NAND gate is an AND gate followed by a NOT gate. Therefore, it outputs a logical 0 if and only if all inputs are a logical 1 and outputs 0 otherwise. The symbol is a regular AND gate with a circle at the output.

POWER REPORT:



Report Power

Generated by: Encounter(R) RTL Compiler v11.10-p005_1 (Nov 10 2011)

Generated on: Mar 03 2020 21:33:47

Module: nor1

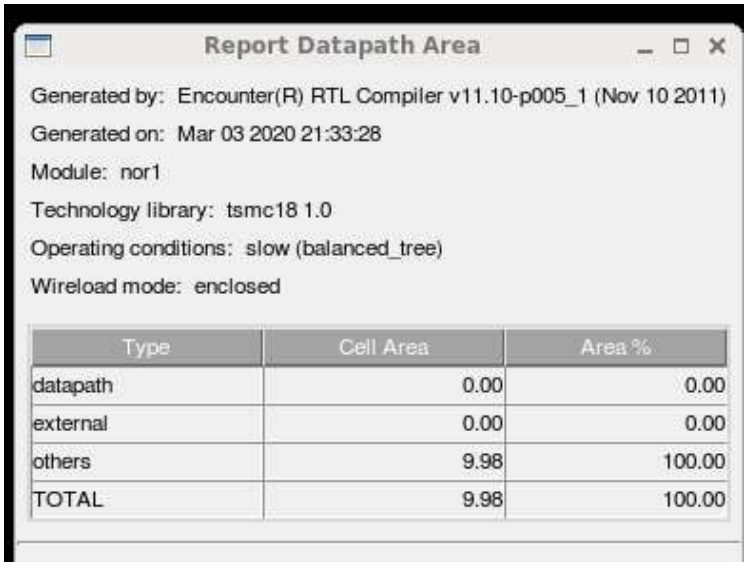
Technology library: tsmc18 1.0

Operating conditions: slow (balanced_tree)

Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
nor1	1	0.13	89.59	161.29	250.88

AREA REPORT:



Report Datapath Area

Generated by: Encounter(R) RTL Compiler v11.10-p005_1 (Nov 10 2011)

Generated on: Mar 03 2020 21:33:28

Module: nor1

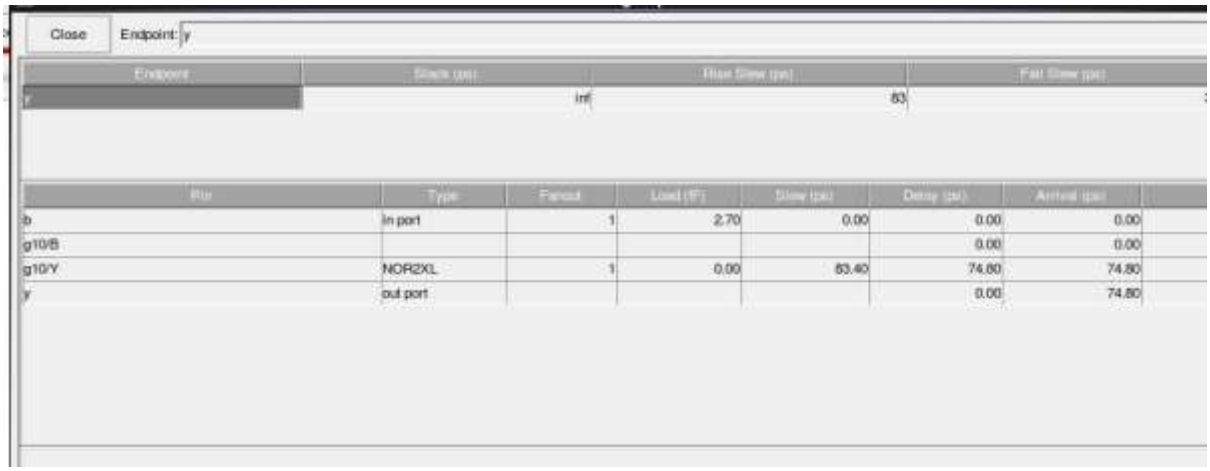
Technology library: tsmc18 1.0

Operating conditions: slow (balanced_tree)

Wireload mode: enclosed

Type	Cell Area	Area %
datapath	0.00	0.00
external	0.00	0.00
others	9.98	100.00
TOTAL	9.98	100.00

TIMING REPORT:



Close Endpoint: y

Endpoint	Slack (ps)	Rise Slew (ps)	Fall Slew (ps)
y	inf	83	

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)
b	in port	1	2.70	0.00	0.00	0.00
g10/B					0.00	0.00
g10/Y	NOR2XL	1	0.00	83.40	74.80	74.80
y	out port				0.00	74.80

PROCEDURE:

Simulation-procedure:

- Create a new folder in desktop and give File name for your experiment.
- Copy **default.global, default.view and synthesize.tcl** files from Cadence folder and past in your folder.
- Right click and open default.global file – Change the line as => **set init_verilog{./Filename_netlist.v}** – Save & Close.
- Right click and open default.view file – Change the line as => **create_constraint_mode –name constraints –sdc_files {Filename_sdc.sdc} -** Save & Close.
- Right click and open synthesize.tcl file – Change the lines as =>

  read_hdl Filename.v

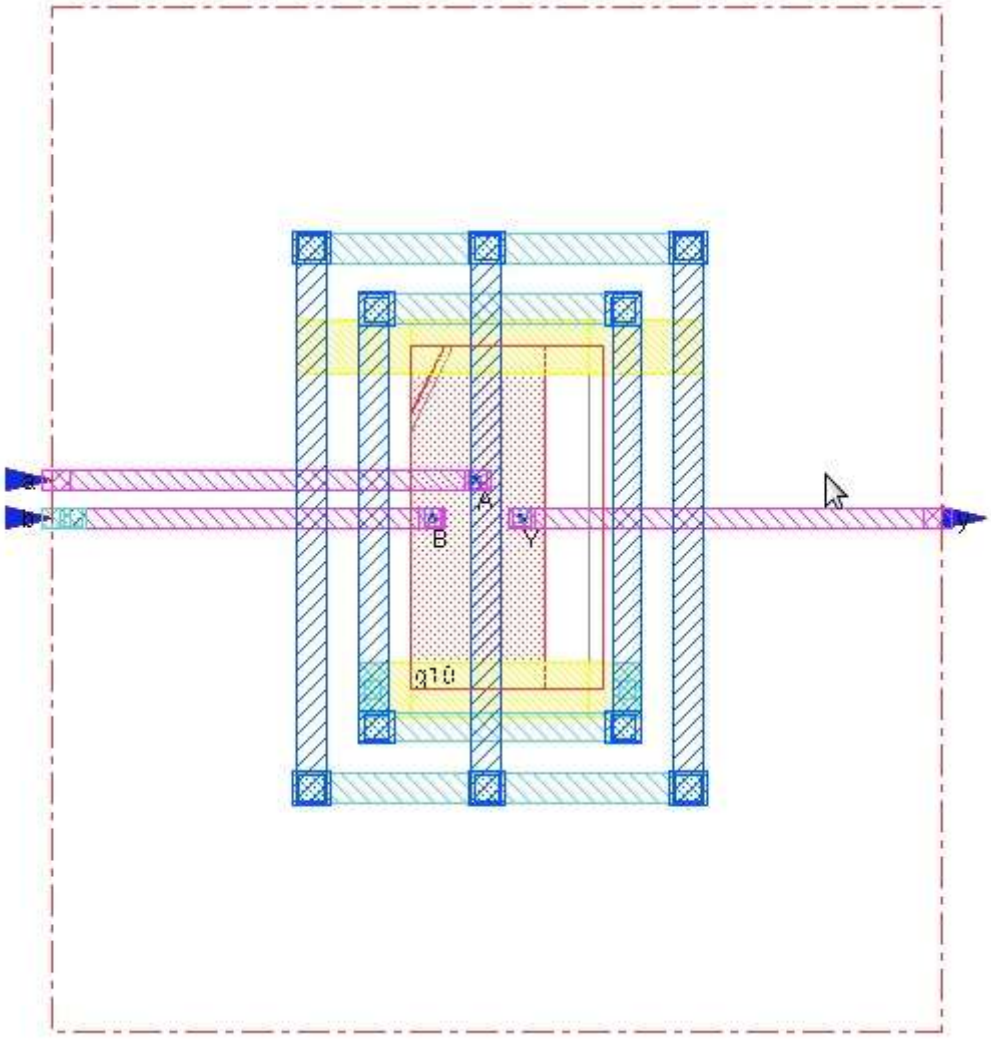
  Write_hdl > Filename_netlist.v

  Write_sdc > Filename_sdc.sdc - Save & Close.
- Right Click from your programme folder – Select open in terminal – Type **csh** – Enter – Type **Source <space> / cad/cshrc.**
- Virtuso window will open – then type **gedit Filename.v**
- New window will open – Type Verilog code for CMOS basic gates and flipflops – File – save – File exit.
- Type **nclaunch<space> -new**
- New window will open in that Click **multiple steps** – **Create CDS file** – save – select **don't include any libraries** – click ok – again click ok.
- Click your file name – Click **vlog** symbol – then Click **tick** symbol – Expand snapshots – Click **Work lib. Filename.v -** Click **Waveform** symbol.
- **Right Click** your **Filename** – Click **send to waveform**
- Give inputs through Simulation icon.
- Get the expected results from the simulation window.
- Take the screenshot of the simulated result.

Analysis Procedure:

- Close all the simulated windows – Go to command window – Type **rc** – click enter - Type- **exit** –click enter- type **rc<space>-f<synthesize.tcl <space> -gui -** click enter.
- Click file name from the process window and obtain the RTL schematic circuit.
- Click **Report - Datapath – Area**
- Click **Report – Power – detailed report – ok**
- Click **Report – Timing – worst path**
- Take the screen shot of the **power-area-Timing** results.
- Click-File-Click- exit

LAYOUT GENERATION:



VERILOG HDL CODE FOR AND GATE

```
module andgate (a,b,y);
output y;
input a,b;
assign y = a & b;
endmodule
```

Layout Generation Procedure:

- In command window Type **encounter** – In encounter window – select **File – Import design** – browse and add – **Filename_netlist.v** - Click close.
- Click – **Load – default globals – open – ok.**
- Click **F** – Click **Floor plan** – Select **Specify Floorplan**
- Set Values as shown below

  Left = 5, Right = 5, Top = 5, Bottom = 5
- Select Floorplan origin at **Centre – Apply – ok.**
- **Power – Power planning – Add Ring** – Browse – **Select V_{dd} & V_{ss}** – Click **add** – Click **ok**.
- Set Ring Configuration values – **Top = metal 5, Bottom = metal 5, Left = metal 6, Right = metal 6** - Select offset as **Center in channel** - Click **ok**
- **Power – Power planning – Add stripe** – Browse – **Select V_{dd} & V_{ss}** – Click **add** - Click **ok** – Select **Layer** – Select **metal 6** – Select **set patterns** – **Number of sets = 1** – Click **ok.**
- **Route – Special route** - Browse – **Select V_{dd} & V_{ss}** – Click **add** - Click ok.
- **Place** – Select **Place standard cell** - Click **ok**.
- Finally **Press F.**
- Obtain the Layout generation of the corresponding logic.

INFERENCE AND DISCUSSIONS:

RESULT:

Thus the CMOS basic gates was designed using Verilog HDL, Simulated, Synthesized and analyzed using Cadence Tool.

Description	Marks Allotted	Marks Obtained
Performance	25	
Record	15	
Viva-Voce	10	
Total	50	

APPLICATIONS:

1. Counters
2. Registers
3. Frequency Divider circuits
4. Data transfer

VIVA-VOCE QUESTIONS:

1. Why NAND and NOR gates are called as universal gates?
2. Who invented the first Flip-flop?
3. What is transparent mode?
4. What is the difference between latch and Flip-flop?

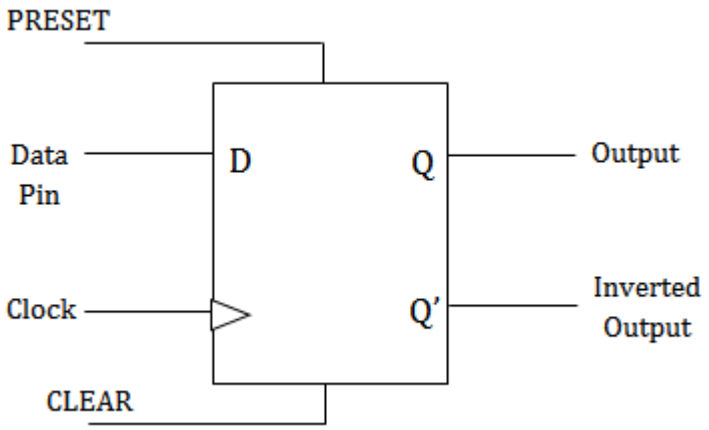
APPLICATION ORIENTED QUESTION:

1. Discuss about layout and stick diagram in detail?
2. Draw the flow chart for VLSI design flow?

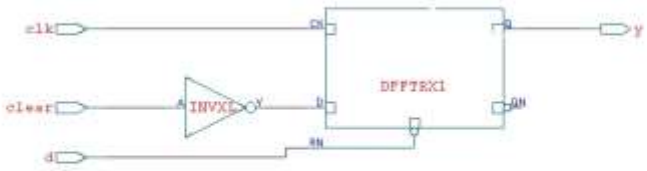
REFERENCES:

1. N.Weste, K.Eshraghian, "Principles of CMOS VLSI Design", Second Edition, Addision Wesley 1993
2. R.Jacob Baker, Harry W.LI., David E.Boyee, "CMOS Circuit Design, Layout and Simulation", Prentice Hall of India 2005
3. A.Pucknell, Kamran Eshraghian, "BASIC VLSI Design", Third Edition, Prentice Hall of India, 2007.

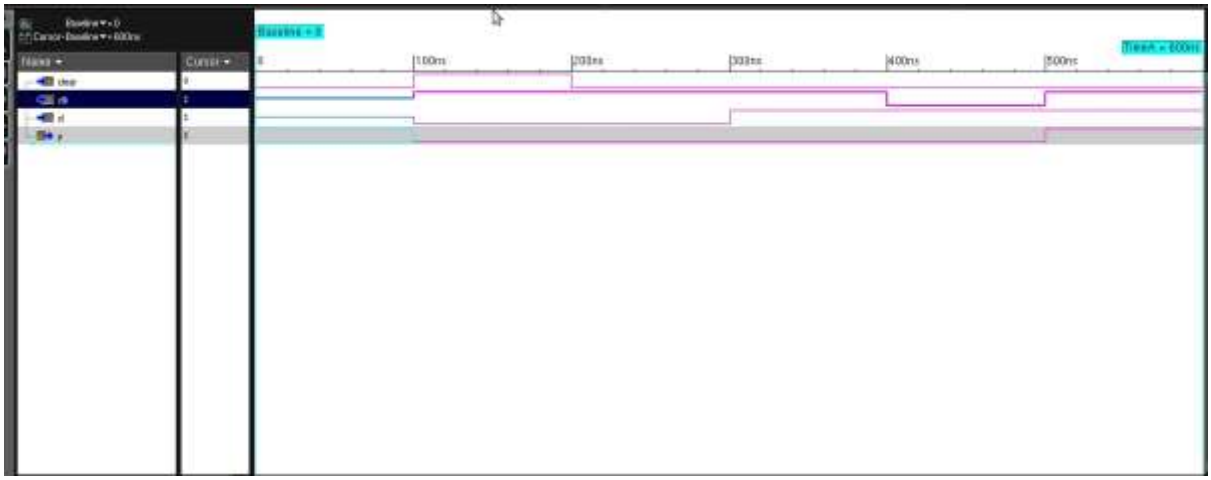
D Flipflop Schematic



RTL Schematic View



Simulation Window



Expt.No.: 8b.	**Design and Simulation of Flip-Flops & Generate Manual/Automatic Layout Using Cadence Virtuoso**
Date:	

AIM:

To write a Verilog code for flip-flops and to perform simulation, synthesis, analyze the power, area and timing report by performing pre layout and post layout simulations in Cadence Virtuoso Tool.

OBJECTIVES:

On completing this experiment the students will be able to

1. Design flip-flops using Verilog code Hardware description language.
2. Simulate, synthesis, analyze the power, area and timing report by performing pre layout and post layout simulations in Cadence Virtuoso Tool.

APPARATUS REQUIRED:

Sl.No.	Name of the Apparatus	Quantity
1	PC	1
2	Cadence Virtuoso Software	-

THEORY:

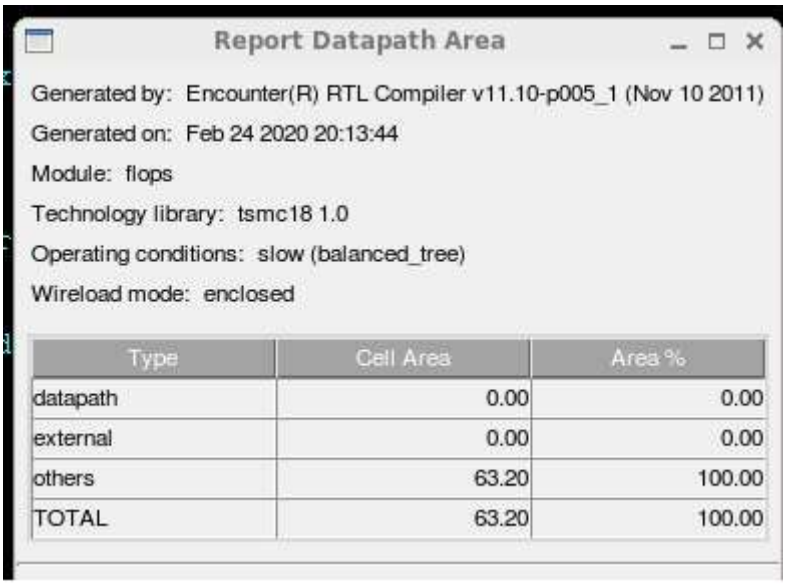
Combinational Logic circuits that change state depending upon the actual signals being applied to their inputs at that time, Sequential Logic circuits have some form of inherent "Memory" built in.

This means that sequential logic circuits are able to take into account their previous input state as well as those actually present, a sort of "before" and "after" effect is involved with sequential circuits.

Flip-Flops:

The Flip-Flop remains locked on an output of either 0 or 1 until it is given some sequence of inputs, in which case its output will change.

Area Report



Report Datapath Area

Generated by: Encounter(R) RTL Compiler v11.10-p005_1 (Nov 10 2011)

Generated on: Feb 24 2020 20:13:44

Module: flops

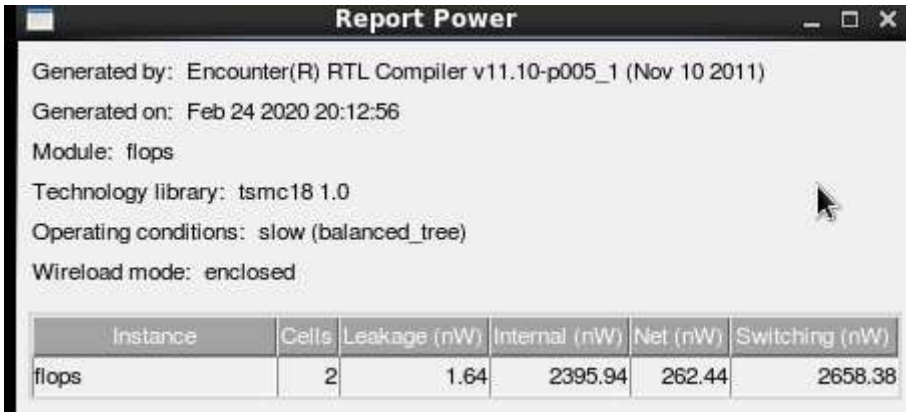
Technology library: tsmc18 1.0

Operating conditions: slow (balanced_tree)

Wireload mode: enclosed

Type	Cell Area	Area %
datapath	0.00	0.00
external	0.00	0.00
others	63.20	100.00
TOTAL	63.20	100.00

Power Report



Report Power

Generated by: Encounter(R) RTL Compiler v11.10-p005_1 (Nov 10 2011)

Generated on: Feb 24 2020 20:12:56

Module: flops

Technology library: tsmc18 1.0

Operating conditions: slow (balanced_tree)

Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
flops	2	1.64	2395.94	262.44	2658.38

Timing Report

Detailed Timing Report

PROCEDURE:

Simulation-procedure:

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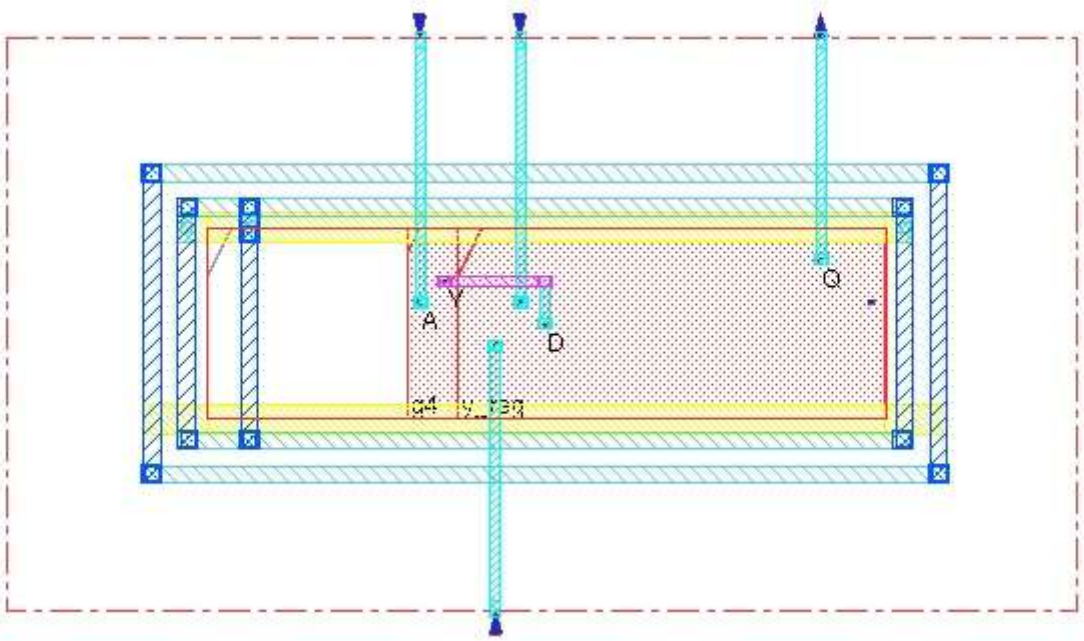
Layout Generation of DFF



VERILOG HDL CODE FOR DFLIPFLOP

```
module dff(d,clk,clr,q);
input d,clk,clr;
output q;
reg q;
always @ (posedge clk)
begin
if (clr==1)
q<=1'b0;
else
q<=d;
end
endmodule
```

Layout Generation Procedure:

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- Click – **Load – default globals – open – ok.**
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INFERENCE AND DISCUSSIONS:

RESULT:

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Record	15	
Viva-Voce	10	
Total	50	