

A Noise-Gated PLL for Clock Recovery in a Free-Space Laser Communication System

by

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Abstract

In this thesis, I developed a phase-locked loop system for data clock recovery in a free-space laser communication application. The clock recovery unit is designed to operate at extremely low optical received power, tolerate a fading channel, and also account for Doppler effects. I explored the feasibility of adding a noise-gating system to the clock recovery unit in order to improve link margin in low-data-rate scenarios. I measured key system performance metrics, such as bandwidth, rejection, lock range and phase noise, and tested system integration with the existing optical communications testbed.

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Contents

| | | |
|----------|--|-----------|
| 1 | Introduction | 11 |
| 1.1 | Context and Motivation | 11 |
| 1.2 | Problem Definition and Objectives | 14 |
| 2 | Theoretical Background | 15 |
| 2.1 | Differential Phase-Shift Keying | 15 |
| 2.2 | Burst Modulation | 16 |
| 2.3 | Clock Recovery and the Phase-Locked Loop | 17 |
| 2.3.1 | Phase Detector | 18 |
| 2.3.2 | Voltage-Controlled Oscillator | 21 |
| 2.3.3 | Loop Filter | 21 |
| 2.3.4 | PLL Advantages | 22 |
| 3 | Multi-rate Clock Recovery System Design | 23 |
| 3.1 | Overview | 23 |
| 3.2 | Automatic Gain Control | 24 |
| 3.2.1 | Circuit Analysis | 25 |
| 3.2.2 | Dynamic Analysis | 29 |
| 3.3 | Phase-Locked Loop | 33 |
| 3.3.1 | Phase Detector | 36 |
| 3.3.2 | Loop Filter | 39 |
| 3.3.3 | Dynamic Analysis | 41 |

| | |
|--|-----------|
| 4 Minimum-Rate Clock Recovery System Design | 45 |
| 4.1 Overview | 45 |
| 4.2 Loop Filter | 46 |
| 4.3 Phase Detector | 47 |
| 4.4 Signal Modifier | 50 |
| 4.5 Dynamic Analysis | 54 |
| 5 Data Acquisition and Analysis | 57 |
| 5.1 Clock Recovery System Evaluation | 57 |
| 5.2 Future Work | 65 |

List of Figures

| | |
|---|----|
| 2-1 DBPSK Illustration [1] | 16 |
| 2-2 Communication Link Block Diagram | 17 |
| 2-3 PLL Block Diagram [6] | 18 |
| 2-4 Multiplier Phase Detector Output | 19 |
| 2-5 XOR Phase Detector Output [6] | 20 |
| 2-6 Three-state Phase Detector [3] | 20 |
| | |
| 3-1 Multi-rate Clock Recovery Block Diagram | 24 |
| 3-2 AGC Integrator Circuit Schematic | 26 |
| 3-3 VGA Input Stage Circuit Schematic | 27 |
| 3-4 VGA Circuit Schematic | 28 |
| 3-5 VGA Output Stage Circuit Schematic | 29 |
| 3-6 AGC Closed-Loop Bode Plot | 32 |
| 3-7 AGC Disturbance Rejection Plot | 33 |
| 3-8 In-Phase/Quadrature Reference Circuit Schematic | 34 |
| 3-9 IF Reference Phase Shifter Bode Plot | 35 |
| 3-10 LVDS Receiver Circuit Schematic | 36 |
| 3-11 Phase Detector Circuit Schematic | 37 |
| 3-12 Double-Balanced Mixer Circuit Schematic [4] | 37 |
| 3-13 Phase Detector Discriminant | 38 |
| 3-14 Loop Filter Circuit Schematic | 39 |
| 3-15 Loop Transmission Bode Plot | 43 |
| | |
| 4-1 Minimum-Rate Clock Recovery Block Diagram | 46 |

| | | |
|------|--|----|
| 4-2 | Minimum-Rate Loop Filter Circuit Schematic | 47 |
| 4-3 | Signal Modifier Waveform Plot | 48 |
| 4-4 | Signal Modifier Discriminant | 49 |
| 4-5 | Signal Modifier Circuit Schematic | 50 |
| 4-6 | MC74AC163D Counter | 51 |
| 4-7 | Signal Modifier Logic Circuit | 53 |
| 4-8 | Signal Modifier Logic Illustration | 54 |
| 4-9 | Minimum-Rate Loop Transmission Bode Plot | 55 |
| 5-1 | Minimum-Rate System Frequency Rejection Plot | 58 |
| 5-2 | Minimum-Rate System Phase Rejection Plot | 59 |
| 5-3 | Minimum-Rate System Loop Transmission | 59 |
| 5-4 | Phase Noise Measurement with Loop Unlocked | 60 |
| 5-5 | RF Generator Phase Noise Measurement | 60 |
| 5-6 | Phase Noise Measurement with Gating Enabled and CW Input | 61 |
| 5-7 | Phase Detector Differential Input | 62 |
| 5-8 | Phase Detector Output | 63 |
| 5-9 | Phase Detector Discriminant | 63 |
| 5-10 | Persistent Plot of Gating Window Alignment | 64 |

Chapter 1

Introduction

I started working at the M.I.T. Lincoln Laboratory as a research assistant in February 2011. My initial work concerned testing and power budgeting for the transmit side of a laser communication system. The system consisted of a master laser, which determined the transmission wavelength to be modulated with data, and several pump lasers, which fed an erbium-doped fiber amplifier (EDFA) used as the power amplifier. My next assignment, and the focus of my thesis, is to develop a phase-locked loop (PLL) circuit that will be used in the clock recovery portion of the laser communication link.

In Chapter 1 of this thesis, I will provide some background on laser communication systems and outline the objectives of the phase-locked loop design. Chapter 2 provides some background theory on clock recovery and phase-locked loops. In Chapter 3, I explain the design of a multi-rate clock recovery system. Chapter 4 details the design of a fixed-rate PLL with a noise gate. My measurements and evaluation of the two systems, and suggestions for future work, are provided in Chapter 5.

1.1 Context and Motivation

Free-space laser communication (lasercom, for short) became popular in the early 1960s. Most of the early development was focused on high-data-rate systems that could compete with radio frequency (RF) communication technology, which was dom-

inant at the time. Later development centered on space-qualified hardware, and a laser crosslink subsystem that could serve as an upgrade for the existing satellite communication network. Unfortunately, technical issues and budget constraints caused many of the early lasercom programs to be cut before they could be completed. The M.I.T. Lincoln Laboratory played a significant role in laser communication development during this time, and succeeded in designing a receiver that used a heterodyne detection scheme. A direct comparison of laser communication technology and RF technology was conducted in the mid-1980s, in which the laser system was shown to have significant advantages over RF in cost, weight and power consumption. More recently, in 1992, scientists at NASA's Jet Propulsion Laboratory demonstrated a laser communication link to a spacecraft at a range of six million kilometers. Presently, research at the Lincoln Laboratory has been focused on high-bandwidth laser communication systems to serve a variety of links.

Laser communication links can connect, in various combinations, terminals located on the ground, in the air, or in space. The space terminals can be satellites in low-earth orbit (LEO) or geostationary/geosynchronous-earth orbit (GEO). LEO satellites are often used for data gathering, while GEO satellites are often used as communication relays. LEO satellites typically orbit at an altitude of hundreds of kilometers, and have a period (time to complete an orbit) of about an hour and a half. Geosynchronous satellites orbit the Earth at an altitude of 35,786km, and tend to trace out a figure-eight pattern in the sky due to a slight inclination from the equator. Geostationary satellites, a subset of geosynchronous, are so called because they appear to always be in the same place in the sky. These satellites are essentially dead-center with the equator (the inclination is near zero).

A common problem with laser communication to a ground terminal is that lasers cannot easily pass through clouds. Thus, on a cloudy day, a vital communication link to a data-gathering satellite could be completely blocked. One way around this is to establish crosslinks between two or more satellites, and pass the information laterally to an area with no cloud cover. Another approach is to send the information to an airplane flying above the clouds (a space-to-air link), which can store the data and

relay it down to the ground later.

Since its earliest development, laser communication has been presented as an alternative to RF technology. Lasercom offers significant advantages over RF, many of which stem from the fact that the wavelength of a laser is on the order of a thousand times smaller than that of a radio-frequency wave. One advantage of the smaller wavelength is greatly increased bandwidth. While a microwave link's bandwidth might be entirely consumed by a single 30GHz channel, a laser link could support 1,000 of these channels and only consume 10% of the carrier. Of course, this potential utilization is limited in reality by the capability of the receiver.

Another advantage offered by the smaller wavelength of laser communication systems is narrower beamwidth. The beamwidth of a wave can be expressed as:

$$\theta = \frac{4\lambda}{\pi D} \quad (1.1)$$

where θ is the beamwidth, λ is the wavelength, and D is the diameter of the aperture. Even if there were a factor of ten difference in aperture size, the laser would still have a beamwidth hundreds of times smaller than the RF wave. Two benefits of narrow beamwidth are enhanced security and greater power efficiency. If we were to compare typical installations of RF and laser systems on geosynchronous satellites, the RF system might cover an area on the ground 1880km in diameter, while the laser might offer an 800m diameter. This means the laser can ensure better privacy in communication - it will be harder for others to intercept. Another direct benefit of the smaller wavelength is greater directivity. Since the laser's beamwidth is so narrow, all its power is concentrated in a much smaller area. This means that the antenna can be much smaller in a laser system than in an RF system, and also the signal can be transmitted at a much lower power.

A typical lasercom transmitter consists of a master laser, which determines the transmission wavelength, a modulator, which applies the data to be transmitted, and a power amplifier, which boosts the signal prior to transmission. A receiver typically consists of a demodulator, which extracts the transmission from the laser carrier, a

low noise amplifier, which boosts the detected signal, a clock recovery system, which extracts the data clock from the transmission, and a data recovery system, which uses the recovered clock signal to reconstruct the transmitted data.

1.2 Problem Definition and Objectives

We seek to design a clock recovery subsystem for a free-space laser communication link that will derive and maintain a data clock from the received data stream. The system must recover the clock with low phase jitter, and must also acquire the clock with high probability within a specified period of time. By exploring a gated PLL design, we aim to greatly improve the signal-to-noise ratio (SNR) of the system, which will in turn reduce phase jitter in the recovered clock - particularly at low data rates. If possible, we hope to use gating even during the PLL's acquisition phase, which will increase link margin. The potential to increase SNR through gating is tremendous, and can yield significant benefits in link design flexibility. For example, with increased SNR, we have the option to decrease transmission power and aperture size in favor of cost, power and space savings.

Chapter 2

Theoretical Background

2.1 Differential Phase-Shift Keying

An important consideration in any communication system design is the choice of encoding scheme. The system we are developing uses differentially-encoded binary phase-shift keying (DBPSK). Phase-shift keying (PSK) is a method of data encoding in which the phase of the optical carrier waveform is modulated to represent the data being transmitted. The data may be represented by changes in absolute phase, which requires precise phase alignment between the transmitter and receiver, or it may be represented by relative changes in phase, which is referred to as a differential encoding.

Differential encoding can eliminate the need for preservation of absolute phase in the carrier waveform. This can be particularly advantageous in situations where the communication channel can introduce phase shifts in the carrier waveform, such as in atmospheric communications. In fact, in cases where the channel introduces an unknown phase shift, the differential encoding scheme can have a bit-error rate lower than that of PSK systems based on absolute phase [1]. The binary part of DBPSK simply means that there are two symbols we are concerned with - zero and one. This makes transmission particularly simple - we can represent a zero by not changing the phase and a one by reversing it. An illustration of a possible DBPSK implementation is shown in Figure 2-1.

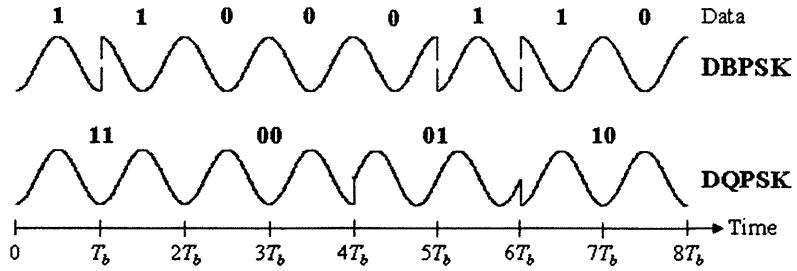


Figure 2-1: DBPSK Illustration [1]

2.2 Burst Modulation

In order to achieve different data rates, a second modulator applies a window to the transmitted signal so that the data arrives in bursts. By varying the duty cycle of this window, we can achieve different data rates while maintaining the same data clock rate. An important consequence of this scheme is that, at low data rates, the data transmission will look like clusters of pulses with significant dead space in between. The consequence of this is that the power in the clock tone - the useful signal power - is reduced, while the noise power is increased. The clock recovery system must be designed with sufficient SNR to maintain lock even at these low data rates.

An important goal of this thesis is to explore a gated PLL circuit. A gated PLL is one that can be connected and disconnected from its input at appropriate times. This is particularly useful in communication scenarios where the usage patterns are “bursty”, meaning there are short intervals of activity interspersed with long periods of inactivity. Gating is a means of synchronizing a sample window with the burst transmissions. A high-level diagram of the optical communication link is shown in Figure 2-2.

The data modulator applies data pulses to the laser at the rate of the transmitter (TX) clock. The signal level at the receiver is dictated by link parameters such as the transmission level and range, while the noise level is set by the EDFA. The ratio of these quantities is the SNR. In between burst transmissions, the clock recovery system is subjected to amplified spontaneous emission (ASE) noise from the receiver EDFA. This severely diminishes the PLL’s signal-to-noise ratio, which in turn makes

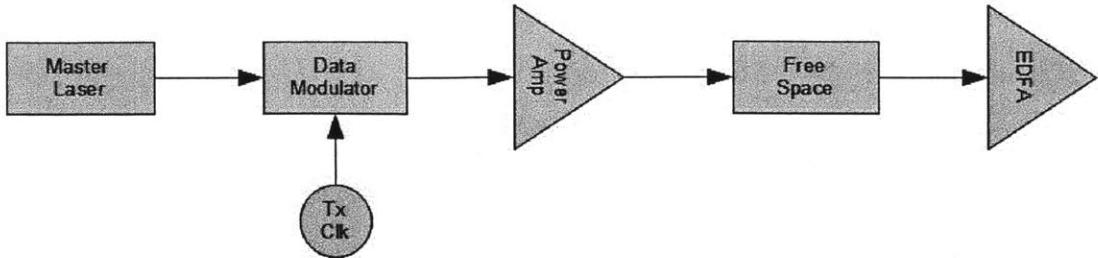


Figure 2-2: Communication Link Block Diagram

acquisition more difficult, and increases phase noise. To get around this, we add a noise gate to the receiver, which can disable the output of the phase detector (PD), causing the voltage-controlled oscillator (VCO) to hold steady at its current frequency. Once communications resume, we can re-enable the PD and allow the PLL to resume tracking. The noise gate will have some assumed duty cycle, a free-running frequency, and a phase that is not typically aligned with the data stream. The goal is to match the noise gate's operation to that of the modulator on the transmit side. The noise gate can be especially beneficial if it can be operated during acquisition.

2.3 Clock Recovery and the Phase-Locked Loop

A clock recovery system is designed to extract the clock signal that is implied by the rate at which the optical data pulses arrive. Once the data clock is recovered, it can be used as a reference to pick out each data bit from the carrier. In our system, the clock recovery circuit is implemented as a PLL. A PLL is a particular type of feedback system that is designed to exactly match the frequency of a given reference waveform - in our case, the received optical data stream. When the system is exactly matched at a stable average frequency, it is said to be “locked.” The time period during which the PLL aligns itself to the transmitter’s frequency and phase is called “acquisition.” Acquisition is only possible if the receiver has sufficient SNR and if the transmitter is within the PLL’s capture range. The capture range is determined by the parameters of the circuit elements that make up the PLL. When the PLL has not

acquired a signal, it exhibits a default or “free-running” frequency and instantaneous phase, independent of what is being transmitted.

Generally speaking, a PLL is composed of a phase detector, a voltage-controlled oscillator, and a loop filter. A block diagram illustrating the interconnection of the three elements is shown in Figure 2-3.

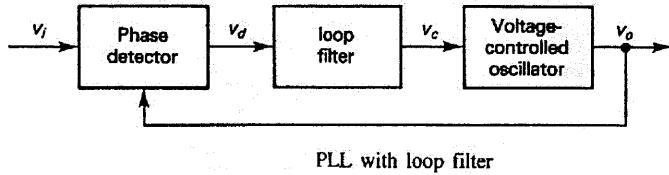


Figure 2-3: PLL Block Diagram [6]

2.3.1 Phase Detector

The phase detector produces an output voltage that is proportional to the phase difference between the input signal, v_i , and the VCO’s output, v_o . This can be modeled as

$$v_d = K_d \theta_e + V_{do} \quad (2.1)$$

where K_d is the PD gain, θ_e is the phase error, and V_{do} is the detector offset voltage. The PD’s nominal output level when the PLL is in a free-running state is called its free-running voltage.

There are several ways of realizing a phase detector, including an analog multiplier, an exclusive-or (XOR) gate and a three-state phase detector. An analog multiplier simply multiplies or “mixes” the input signal with the reference VCO. The resulting output voltage is a function of the phase difference between the signal and the VCO. A plot of this characteristic is shown in Figure 2-4.

A disadvantage of the multiplier as a phase detector is that its phase detector gain K_d depends on the amplitude of both the input signal and the VCO output. This

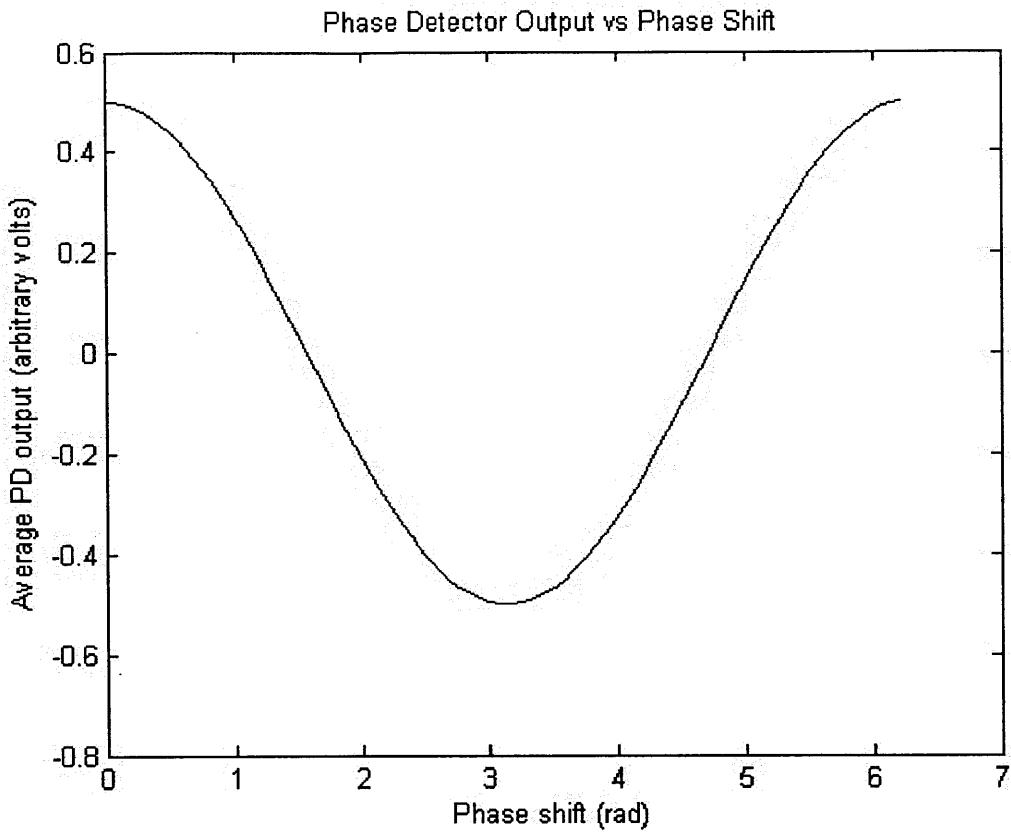


Figure 2-4: Multiplier Phase Detector Output

can degrade loop stability in situations where the input signal amplitude is highly variable.

The XOR gate phase detector is not as sensitive to input signal amplitude. In fact, its K_d does not depend on either the input signal amplitude or that of the VCO output. It actually behaves a lot like a multiplier with both of its inputs driven into clipping. Its output V_a versus phase error is shown in Figure 2-5.

One disadvantage of the XOR phase detector is that it will not respond to an input signal that doesn't exceed its digital thresholds. These thresholds are designed to improve noise immunity in a digital environment, but can cause problems when trying to couple in an analog signal.

The three-state phase detector is composed of two DQ flip flops, one triggered by the input signal, the other by the VCO. A NAND gate resets the flip flops when both

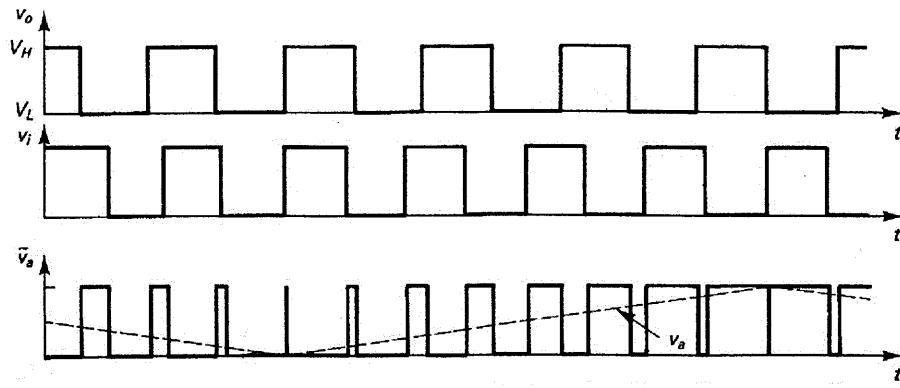


Figure 2-5: XOR Phase Detector Output [6]

of their inputs go high (they are both “set”). An illustration of the three-state circuit is shown in Figure 2-6.

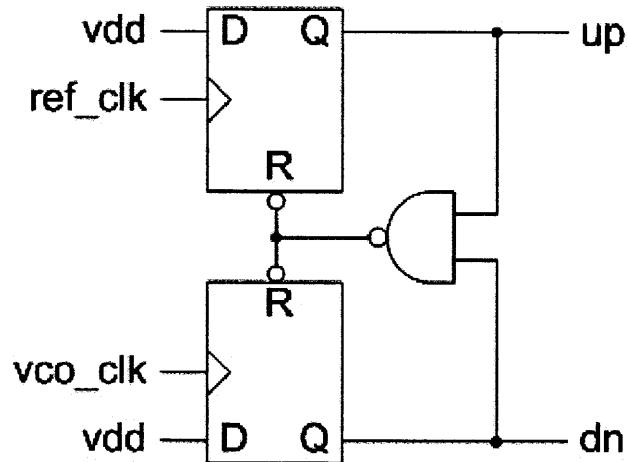


Figure 2-6: Three-state Phase Detector [3]

This type of phase detector is insensitive to signal amplitude and also can respond to phase errors from 0 to 2π - twice the range of the other detectors. It is, however, very sensitive to noise. Unfortunately, our application will often have negative SNR (more noise power than signal power), so this type of detector is unsuitable.

We developed a custom phase detector, described in Section 3.3.1, that is similar to the analog multiplier and XOR gate but eliminates many of their disadvantages.

2.3.2 Voltage-Controlled Oscillator

The VCO changes the frequency of its output in response to an input voltage. We can represent the frequency deviation between the VCO output and our reference waveform as

$$\Delta\omega_o = K_o(v_c - V_{co}) \quad (2.2)$$

where K_o is the VCO gain, v_c is the control voltage, and V_{co} is the control voltage required to achieve lock (or equivalently, for $\Delta\omega_o = 0$). Since frequency is the derivative of phase, we can represent the output phase of the VCO as the integral of its frequency deviation $\Delta\omega_o$:

$$\theta_o = \int \Delta\omega_o dt \quad (2.3)$$

It is this inherent integration which yields zero frequency error in “locked” mode. Our application additionally requires zero phase error and low phase jitter. To achieve this, we have to use an active loop filter.

2.3.3 Loop Filter

The function of the loop filter is to adjust the PD’s output voltage before it reaches the VCO. Through our choice of loop filter, PD, and VCO, we can reduce steady-state phase error, increase phase disturbance rejection, and control the PLL’s bandwidth. Together with SNR, these parameters drive phase jitter, which is the key performance metric of a PLL.

The most basic loop filter is a passive lowpass filter, which helps reduce harmonic content in the phase detector’s output. It will not, however reduce steady-state phase error, as its gain is limited to unity. To reduce phase error, we have to use an active filter.

Basic control theory tells us that steady-state error is reduced by a factor of the system’s DC open-loop gain. An integrator will provide theoretically infinite DC

gain, thus reducing the steady-state error to zero. It's very common to add an active integrator to a PLL in order to reduce phase error, but careful consideration must be made in order to ensure loop stability. This second integrator introduces another 90 degrees of phase shift that will cause the system to oscillate at the unity gain crossover frequency. To stabilize the loop, we have to add a zero near the crossover frequency, so that we have positive phase margin.

A control loop with one integrator is known as a first-order loop. A second-order loop has two integrators, a third-order loop would have three, and so on. While a second-order PLL has zero phase error, it has a disadvantage in that its lock range - the frequency range over which it can achieve phase lock - is limited. We can address this by designing the active integrator so that it can be “turned off”, allowing for an increased lock range during acquisition, and “turned on” again once the signal is locked. Thus, we can enjoy the advantages of both a first-order and a second-order loop.

2.3.4 PLL Advantages

It may seem tempting to forgo the complexity of PLL design and instead use a narrow bandpass filter to pass only the clock frequency component in the carrier waveform. This may seem appealingly simple, but the PLL offers many distinct advantages. For one, it can more easily combat background noise, as it specifically seeks to lock on to periodic signals, and the integrating nature of the VCO (in terms of phase) will effectively suppress noise that can be modeled as additive, white, and Gaussian (which is often how we model most noise). A PLL can also track a clock signal that is drifting with time due to Doppler effects, which is particularly relevant in satellite communications. Finally, a PLL can be configured to track a range of frequencies, enabling it to support a variety of data rates on the communication link.

Chapter 3

Multi-rate Clock Recovery System Design

3.1 Overview

The multi-rate clock recovery system is designed to support a variety data rates from several gigabits per second (Gbps) to tens of megabits per second (Mbps). A block diagram of this system is provided in Figure 3-1. The multi-rate system uses a heterodyne detection scheme for clock recovery, which means that it mixes the RF input signal down to an intermediate frequency (IF) before it reaches the phase detector. The presence of this IF band facilitates automatic gain control (AGC) to help hold the phase-locked loop bandwidth constant.

The multi-rate clock recovery system is designed to support optical communication over a fading, noisy channel at a variety of data rates. It is capable of receiving a wide dynamic range of optical input powers and recovering the data clock with low phase jitter at all anticipated power levels. It is also designed to tolerate Doppler shift in the incoming clock tone and survive temporary fading of the received optical power.

The system is comprised of two loops: the automatic gain control, and the PLL. The AGC loop attempts to maintain constant input signal amplitude, which ensures constant PLL bandwidth, by multiplying the IF input by an adjustable gain. The

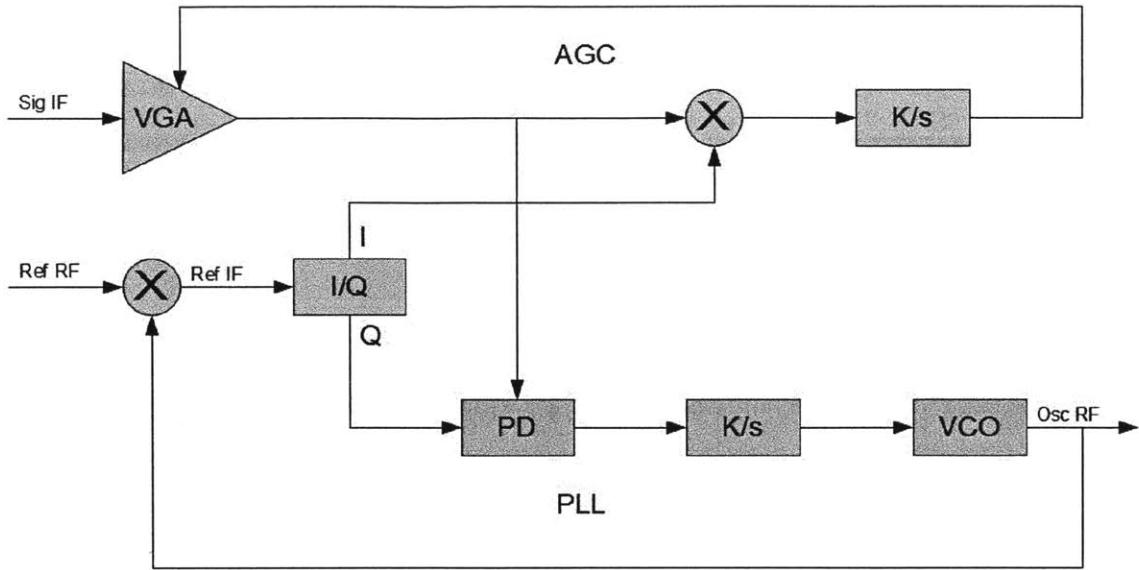


Figure 3-1: Multi-rate Clock Recovery Block Diagram

PLL operates on the amplitude-controlled input IF signal and locks to its average frequency and absolute phase. Not shown in the block diagram are the RF reference oscillator, which provides the input labeled “Ref RF,” and the second RF mixer, which mixes the RF input signal with the reference oscillator’s output to produce the intermediate-frequency signal input, labeled “Sig IF”. The reference RF signal is also mixed with the VCO’s RF output to produce an IF reference signal. This signal is split into in-phase (I) and quadrature (Q) reference signals. The in-phase reference is used by the AGC loop, and the quadrature reference is used by the PLL.

3.2 Automatic Gain Control

The AGC loop is a critical part of this system design because the input optical power (which directly corresponds to RF signal amplitude) has a very wide dynamic range. The PLL bandwidth depends on the signal amplitude, so it is very important for system stability and phase noise performance that the input amplitude be well-controlled over the dynamic range of input optical power. The AGC provides this control, but only while the PLL is locked.

The AGC loop mixes the IF input signal with the in-phase IF reference signal, which, when the PLL is locked, produces a DC output proportional to the amplitude of the input signal plus a component at twice the input signal frequency. To demonstrate this, consider two sinusoidal input signals of amplitude A_1 and A_2 , and frequency ω_1 and ω_2 . Using a basic trigonometric identity, we can see that

$$A_1 \sin(\omega_1 t) A_2 \sin(\omega_2 t) = \frac{A_1 A_2}{2} \cos[(\omega_1 - \omega_2)t] - \frac{A_1 A_2}{2} \cos[(\omega_1 + \omega_2)t] \quad (3.1)$$

When $\omega_1 = \omega_2$, as is the case when the PLL is locked, this reduces to

$$A_1 \sin(\omega_1 t) A_2 \sin(\omega_2 t) = \frac{A_1 A_2}{2} (1 - \cos[(2\omega_1)t]) \quad (3.2)$$

The amplitude of the reference IF signal is well-controlled, so the DC term will vary with the input signal amplitude, which is directly related to input optical power. The double-frequency component is attenuated by the loop filter. The loop filter's function is to compare the DC level from the mixer to a reference value, and produce a voltage command that adjusts a variable-gain amplifier (VGA). The VGA is the mechanism by which the AGC loop exerts its control over the input amplitude. Thus, the signal is expanded or compressed to fit into a fixed amplitude envelope.

3.2.1 Circuit Analysis

The mixer used in the AGC loop is the same as that in the PLL. The active double-balanced mixer's use as the PLL's phase detector is described in Section 3.3.1. In the AGC loop, the mixer is used to multiply the input signal with the in-phase reference signal. The mixer output is passed to the loop filter, the schematic for which is given in Figure 3-2.

The op amp is configured as an inverting integrator, which implements the transfer function

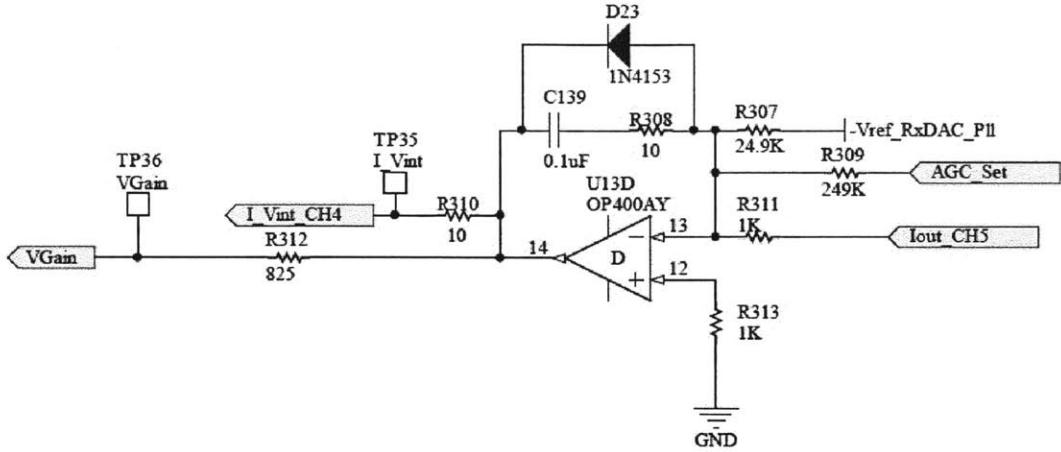


Figure 3-2: AGC Integrator Circuit Schematic

$$A(s) = \frac{-K}{s} \quad (3.3)$$

where $K = \frac{1}{R_{311}C_{139}}$. Resistor R_{308} adds a zero to the transfer function, and can be used to cancel parasitic poles in the forward path. The complete transfer function (ignoring the zero) is then

$$A(s) = \frac{-1}{R_{311}C_{139}s} \quad (3.4)$$

The diode in parallel with C_{139} and R_{308} provides unipolar operation required by the VGA. The AGC_Set and -Vref_RxDAC_Pl inputs can be used separately or in tandem to set the reference point that the loop tries to achieve. The integrator will adjust its output so that the sum of the currents at its inverting terminal is zero. This means it will try to assert that

$$I_{out_CH5} = \frac{1}{24.9}(-V_{ref_RxDAC_Pl}) - \frac{1}{249}AGC_Set \quad (3.5)$$

For example, if $-V_{ref_RxDAC_Pl} = -5V$ and $AGC_Set = 0V$, then the loop will try to maintain I_{out_CH5} at about 200mV.

We chose to use the AD600 as our variable-gain amplifier. The AD600 has two

channels, each with up to 40dB of gain. By cascading the two channels, we can achieve 80dB gain (in V/V), which allows us to control signal amplitude over a dynamic range of 40dB in optical input power. The AD600 also has low noise and wide bandwidth, which is important for this application. A schematic illustrating the input stage ahead of the AD600 is provided in Figure 3-3.

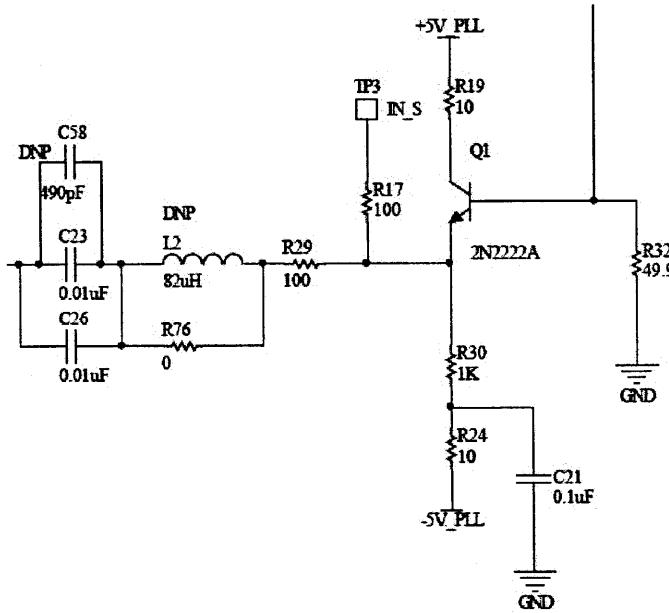


Figure 3-3: VGA Input Stage Circuit Schematic

The IF signal input arrives at the base of transistor Q1, which buffers the signal. The RLC network at the transistor's emitter is designed to be configurable as a band-pass filter, to help remove noise outside the band of interest. A schematic illustrating the connection of the AD600 is provided in Figure 3-4.

The AD600's control voltage inputs, C1HI/LO and C2HI/LO, are designed to be driven differentially from 0V to 1.25V. By applying a bias of about 1.9V to C1LO and about 0.6V to C2LO (+Vref_RXDAC_PLL is +5V), we can stagger the command voltage applied to each of the stages, so that the first stage fully increases its gain before the second stage begins to increase its gain. This is recommended by the manufacturer in order to maximize SNR. VGAIN is the voltage command produced by the integrator. The output stage after the VGA is shown in the schematic in

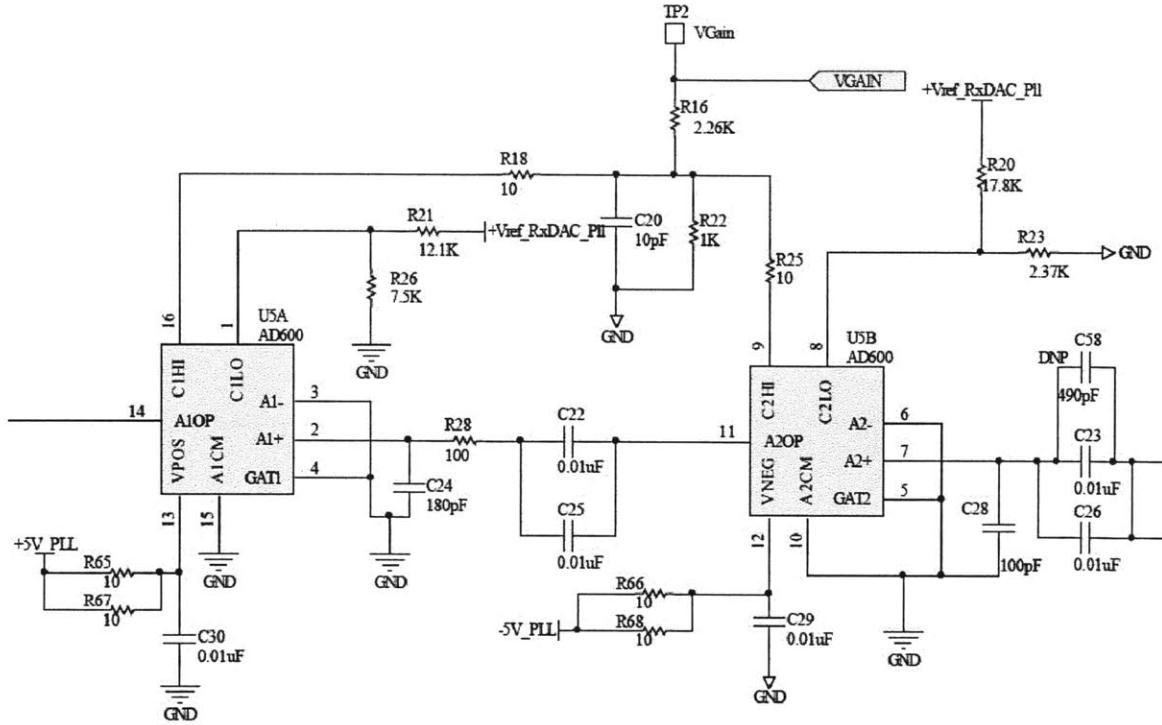


Figure 3-4: VGA Circuit Schematic

Figure 3-5.

Transistors Q2 and Q3 are designed to provide a fixed gain of about 5V/V to the input signal, in order to map the AGC's dynamic range to the input levels required by the communication system. Diodes D3 and D4 clip the input signal in order to avoid saturating the op amps in the mixer stage (when the input signal is large, prior to acquisition).

The input signal can be very large if the optical signal power is on the higher end of its anticipated range, or if the AGC loop is not closed. The AGC loop will not be closed if the PLL is in its acquisition phase. The reference and input signal frequencies will not be the same, so no DC voltage will appear at the integrator's input, leaving only the reference voltage. The negative reference voltage will cause the inverting integrator to swing to its positive rail, commanding maximum gain. This, in turn, produces a potentially very large input signal amplitude, which must be clipped in order to protect the op amps in the mixer from saturating.

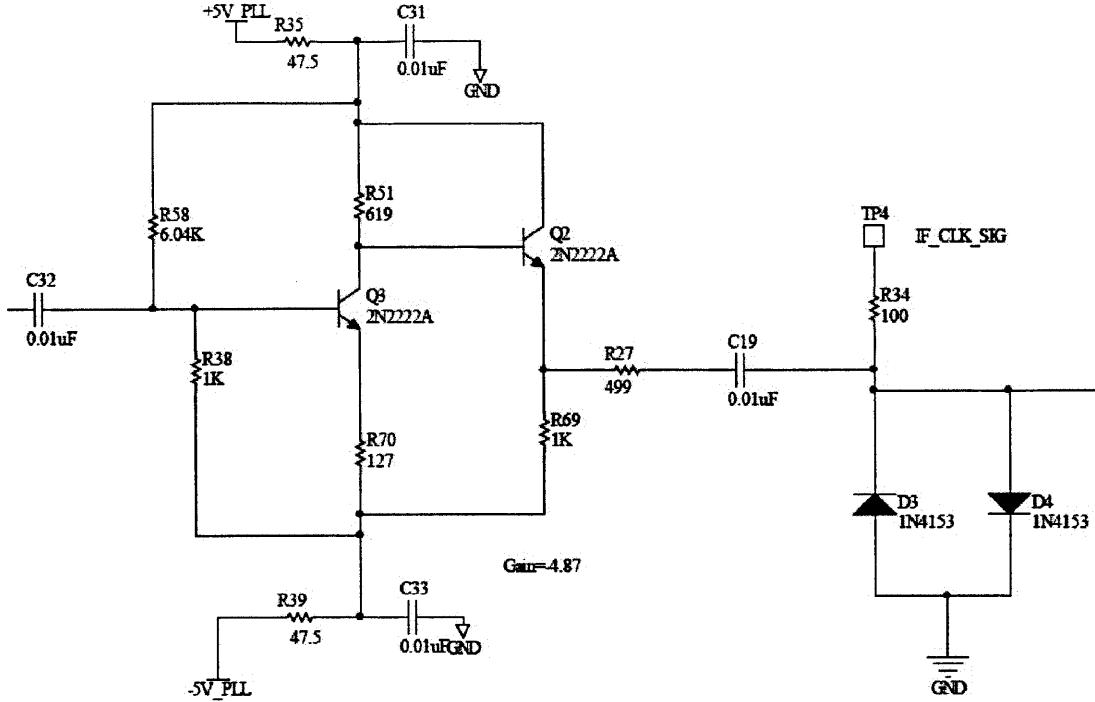


Figure 3-5: VGA Output Stage Circuit Schematic

3.2.2 Dynamic Analysis

Our variable-gain amplifier presents a challenge in analyzing the dynamics of the AGC loop. Linear feedback analysis, as its name implies, relies on the fact that the system of interest is linear. In an AGC, the loop gain is a function of signal amplitude. Furthermore, the AD600's gain scales linearly in decibels with voltage, which means its gain changes exponentially for linearly increasing control voltage. Analysis of this circuit leads to a transcendental equation of the form $v = \exp^{\alpha v}$. Transcendental equations are usually solved by graphical or numerical methods. In this case, we can work around the problem by linearizing.

The AGC loop tries to maintain a constant target amplitude V_{target} by varying its gain A_v . Thus, it tries to satisfy the equation

$$V_i A_v = V_{target} \quad (3.6)$$

where V_i is the input amplitude. We also require that the loop bandwidth remains

fairly constant over the expected range of input power (and consequently, input amplitude). Constant bandwidth means the closed-loop behavior will be the same at every power level. The effective time constant of the loop varies only with the size of the change in input power. We can linearize the gain vs control voltage characteristic, and represent it as a constant:

$$V_i \frac{dA_v}{dV_{agc}} = C_1 \quad (3.7)$$

V_{agc} is the AGC control voltage. This approach works if $\frac{dA_v}{dV_{agc}}$ is exponential - the local “slope” of the gain vs control voltage characteristic will change depending on the operating point. C_1 is the linearization of the AGC’s gain vs. control voltage characteristic around the operating point for a particular V_{target} . If we divide equation 3.7 by equation 3.6 and rearrange terms, we get

$$\frac{dA_v}{A_v} = \frac{dV_{agc} C_1}{V_{target}} \quad (3.8)$$

Taking the integral of equation 3.8 yields

$$\ln A_v + C_2 = \frac{V_{agc} C_1}{V_{target}} \quad (3.9)$$

As explained in the previous section, the gain of the AD600 will vary from 0dB to 80dB for a control voltage range of -0.625V to 0.625V (differential). Using this information, we can write the following two equations:

$$2.303 \log A_{v,max} + C_2 = \frac{V_{agc,max} C_1}{V_{target}} \quad (3.10)$$

$$2.303 \log A_{v,min} + C_2 = \frac{V_{agc,min} C_1}{V_{target}} \quad (3.11)$$

Where 2.303 is the conversion factor between ln and log. Adding equations 3.10 and 3.11, we have

$$2C_2 + 2.303\left(\frac{80dB}{20} + \frac{0dB}{20}\right) = 0 \quad (3.12)$$

which gives $C_2 = -4.606$. We can now use equation 3.11 to solve for C_1 :

$$C_1 = \frac{C_2 V_{target}}{V_{agc,min}} \quad (3.13)$$

We showed earlier that the AGC loop will try to maintain Iout_CH5 at about 200mV. V_{target} is the input amplitude directly after the VGA. After the VGA, the input goes through a transistor stage which provides a gain of about 5V/V and an op amp stage which provides a gain of 2V/V. It is then mixed with the in-phase reference signal, in order to find its average value, which can be represented by an additional gain of $\frac{2}{\pi}$. This means there is a gain of $\frac{20}{\pi}$ between V_{target} and Iout_CH5, so $V_{target} = 31mV$. Using this value of V_{target} , we get $C_1 = 0.229$. Using the values for R_{311} and C_{139} given in the schematic, the AGC's integrator implements the following transfer function:

$$A(s) = \frac{-10^4}{s} \quad (3.14)$$

Finally, the resistor network between the integrator output and the VGA control voltage provides an attenuation of

$$K_{atten} = \frac{R_{22}}{R_{312} + R_{16} + R_{22}} = 0.245 \quad (3.15)$$

Thus, our loop transmission for the AGC operating around a target of 31mV is

$$L(s) = C_1 K_{atten} A(s) = \frac{-561}{s} \quad (3.16)$$

This loop transmission may appear unstable from the perspective of negative feedback analysis. However, the summing node at the input to the integrator does not have the usual inversion. This is actually a positive feedback system with an inversion in the forward path, which is analogous to a negative feedback system with no inversion. Plots of the closed-loop transfer function and disturbance rejection are

provided in Figures 3-6 and 3-7. The loop bandwidth at this operating point is about 89Hz and the phase margin is close to 90 degrees.

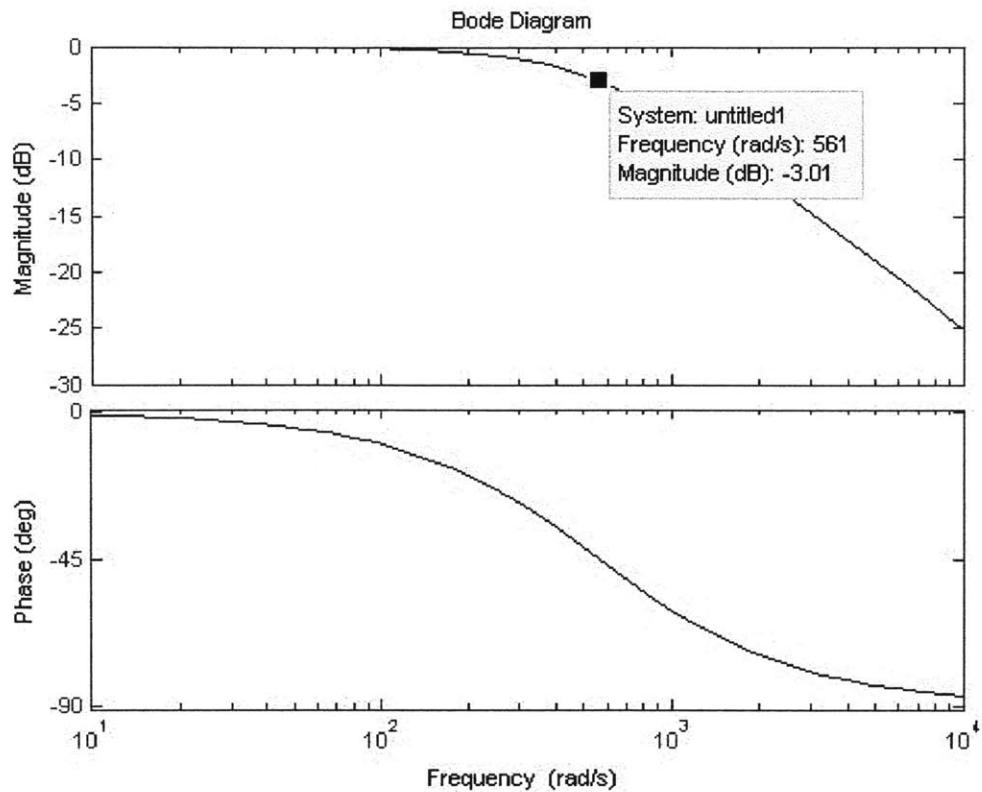


Figure 3-6: AGC Closed-Loop Bode Plot

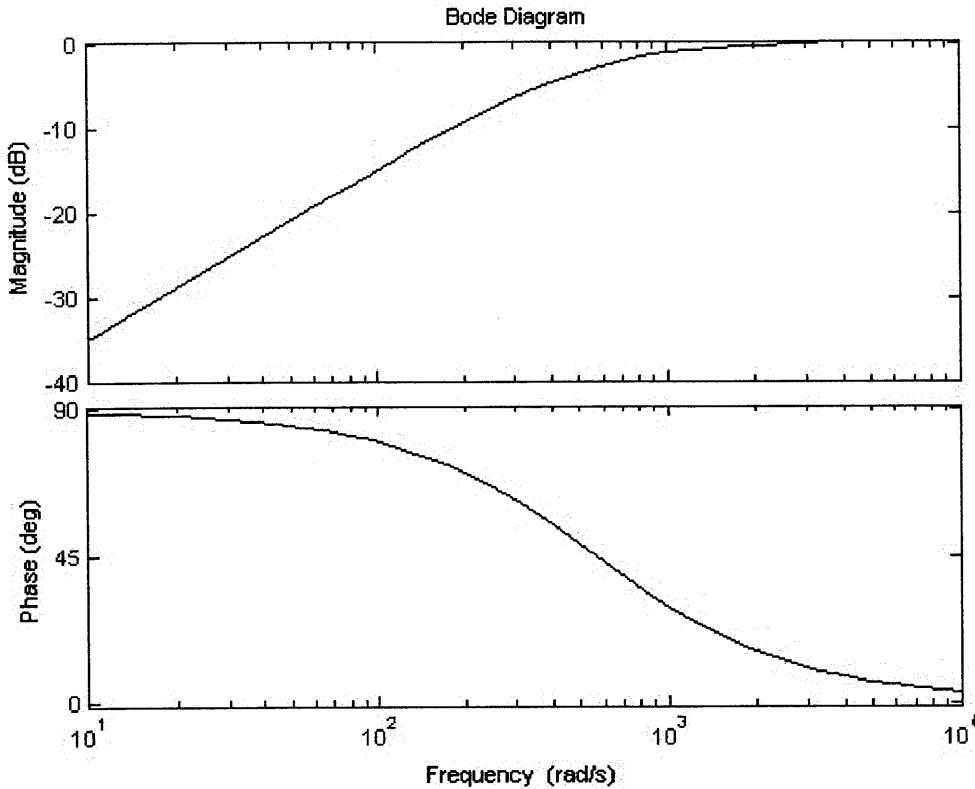


Figure 3-7: AGC Disturbance Rejection Plot

3.3 Phase-Locked Loop

As explained in Chapter 2, the PLL consists of a VCO, a phase detector and a loop filter. The function of the PLL is to lock to the average frequency and absolute phase of the input signal, thereby recovering the data clock inherent to the pulses of received optical power. The design of the phase detector and loop filter and the loop's dynamic characteristics will be explained in each of the following sections. The PLL operates on the input IF signal and a version of the IF reference signal that is shifted so that it is in quadrature with the original reference signal. The phase shift is accomplished with the circuit shown in Figure 3-8.

The op amp labeled U28C is configured as a lowpass filter with nominal gain of 20 in the passband and a corner frequency of about 40kHz. Thus, at frequencies sufficiently above the corner frequency, the phase shift is 90 degrees. A bode plot of

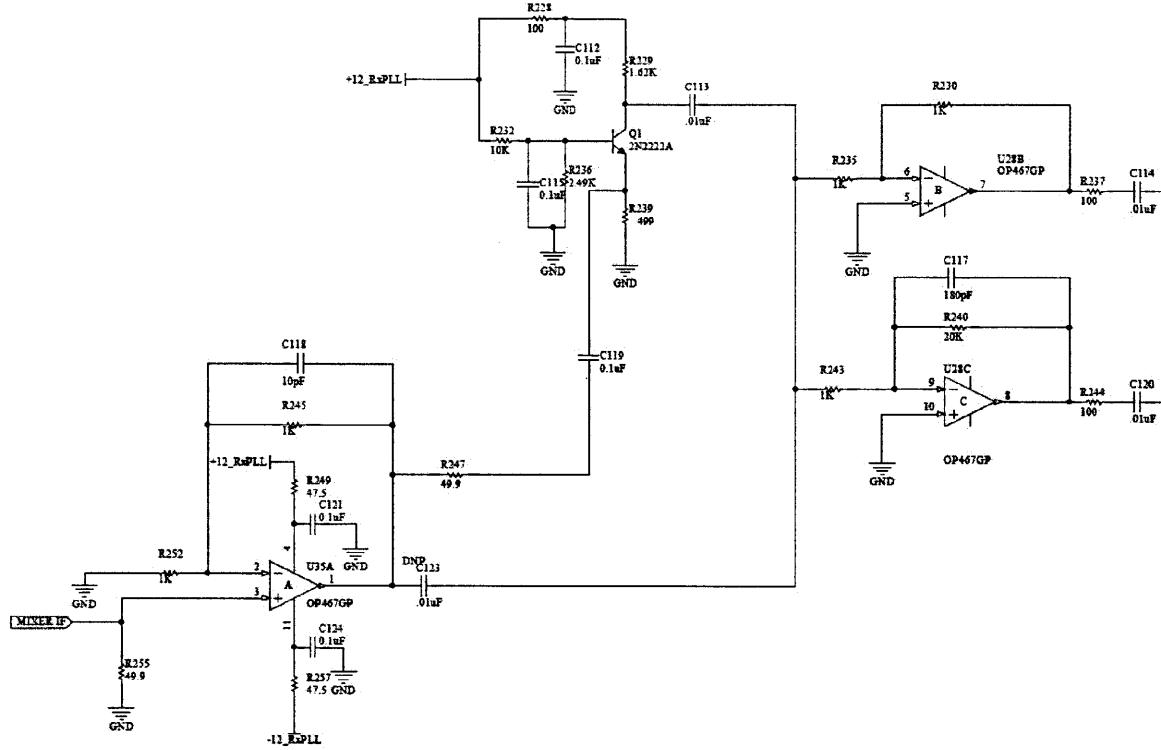


Figure 3-8: In-Phase/Quadrature Reference Circuit Schematic

this characteristic is provided in Figure 3-9 for reference.

Op amp U35A receives the IF reference signal directly from the RF mixer (not shown on this schematic) and applies a gain of 2. There is an optional transistor stage, Q1, which provides an additional gain of about 2. U28B buffers the in-phase reference signal and U28C performs the quadrature shift. The in-phase and quadrature reference signals are then passed to an LVDS (low-voltage differential signalling) receiver, shown in Figure 3-10. C_{114} and C_{120} AC-couple the signal so it can be centered about the proper common-mode voltage for the differential receiver.

Diodes D20 and D21 are included to limit the signal swing into the UT54LVDS032 differential receiver IC. The UT54LVDS032 boosts the IF reference signals from a nominal 600mVpp to about 3Vpp. Jumpers P3 and P4 allow the polarity of the reference signals to be switched, if needed. Polarity is very important, particularly for the AGC loop - we have to ensure that the DC level generated is positive so that the integrator input has a chance at falling to zero (recall that the reference voltage

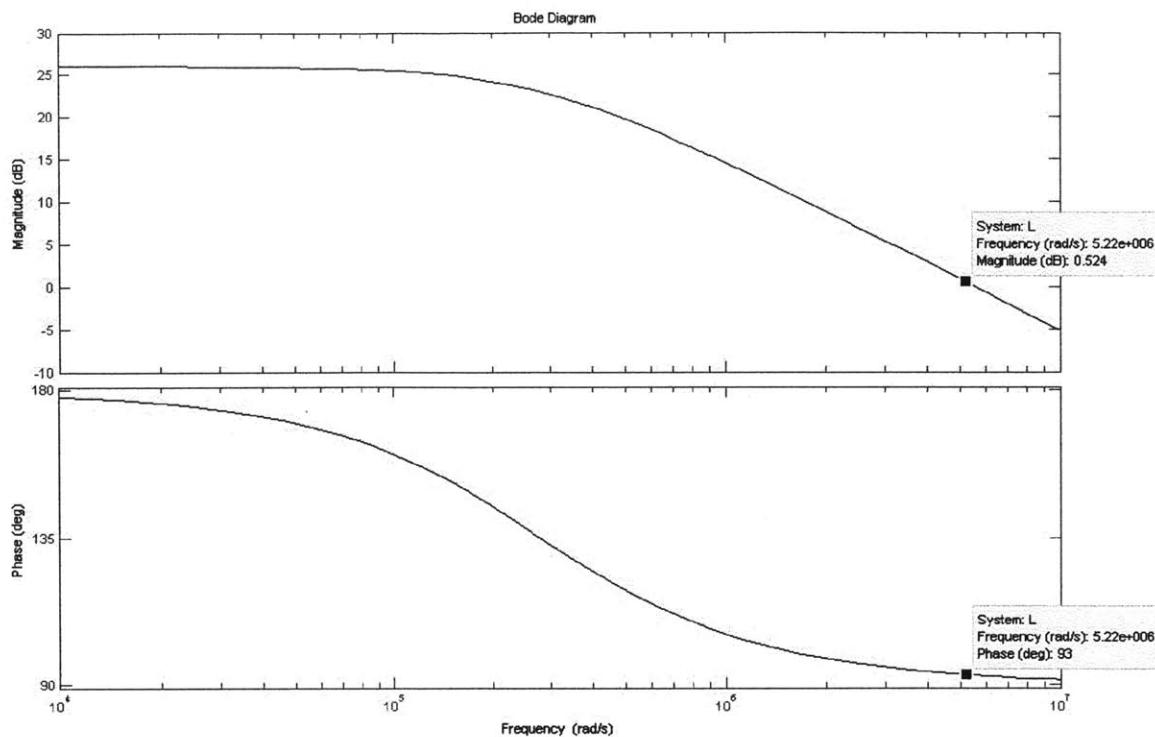


Figure 3-9: IF Reference Phase Shifter Bode Plot

is negative). The differential receiver IC drives the mixers in the AGC and PLL with the in-phase and quadrature reference signals, respectively.

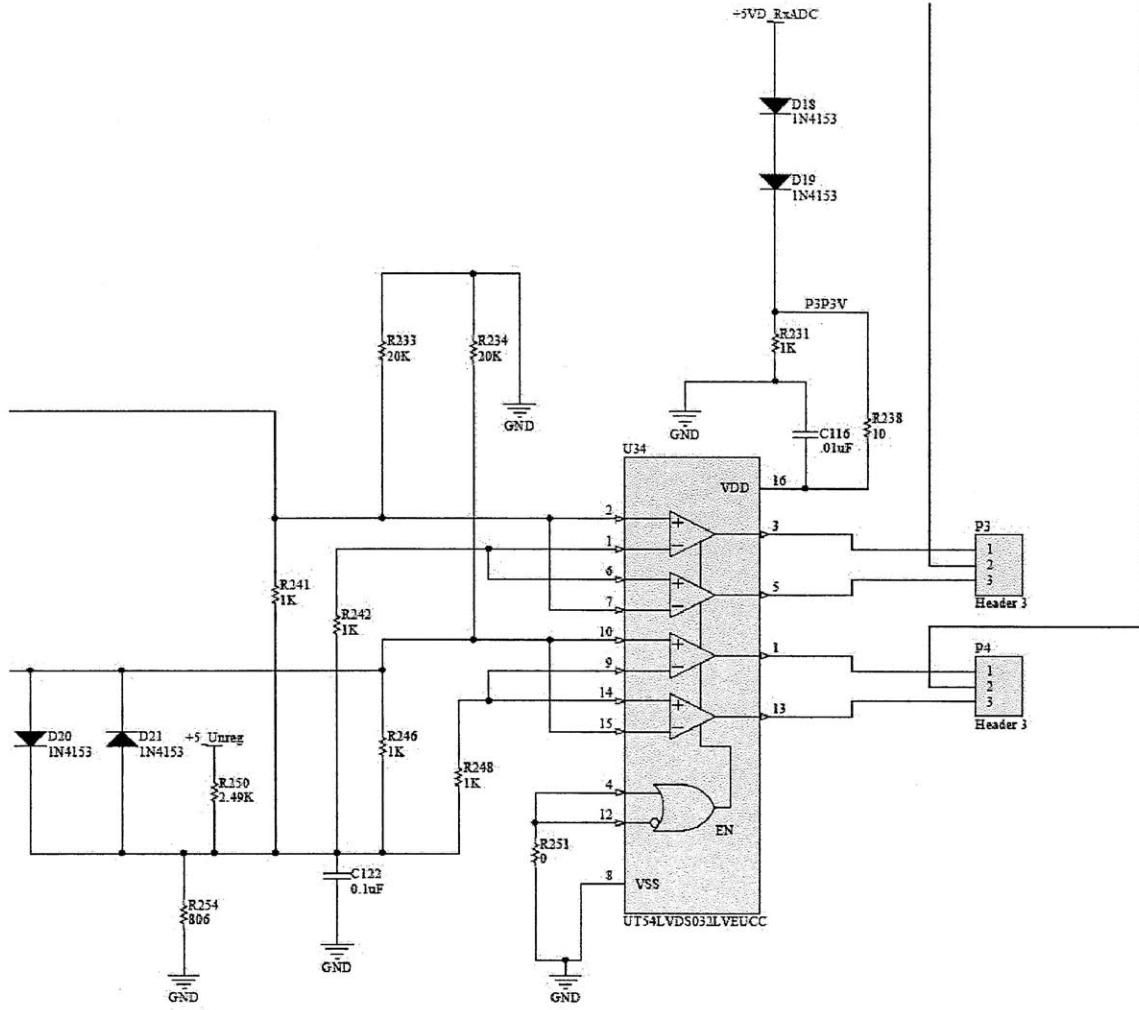


Figure 3-10: LVDS Receiver Circuit Schematic

3.3.1 Phase Detector

The phase detector provides an output voltage to the loop filter that is a measure of the phase difference between the input signal and the quadrature reference signal. It is realized in the circuit shown in Figure 3-11.

In our system, the PD is implemented as an active equivalent of a double-balanced mixer. A typical passive double-balanced mixer is composed of a diode bridge and two baluns (balanced to unbalanced signal converters), as shown in Figure 3-12.

The signal at the local oscillator (LO, here labeled L) port causes the signal at the RF (labeled R) port to be transmitted to the IF (labeled I) port with alternating

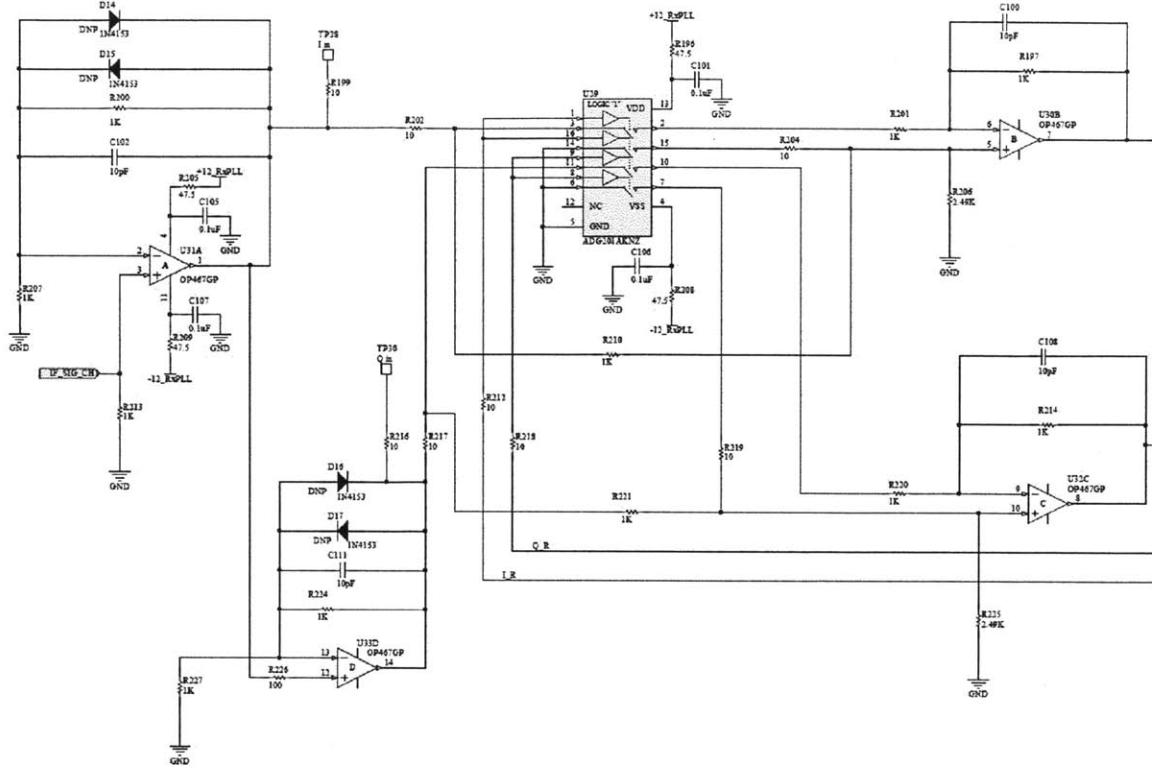


Figure 3-11: Phase Detector Circuit Schematic

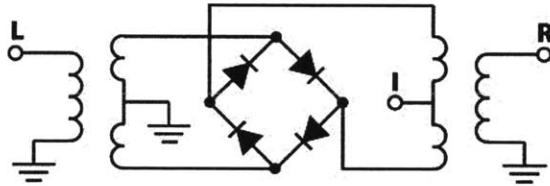


Figure 3-12: Double-Balanced Mixer Circuit Schematic [4]

polarity. This is equivalent to mixing the RF signal with a signal of amplitude +1 and -1 and the same frequency as the LO. Our PD emulates this behavior using an op amp and an analog switch IC. The op amp is configured so it can be toggled between a gain of 1 and -1, using the switch IC to present the IF signal input at one terminal or the other. The IF reference signal drives the switch IC and causes the mixing action. We are effectively mixing the input signal with a square wave. The output of the phase detector will vary with phase shift as in the plot shown in Figure 3-13.

This type of plot is called the phase detector discriminant. As the plot indicates,

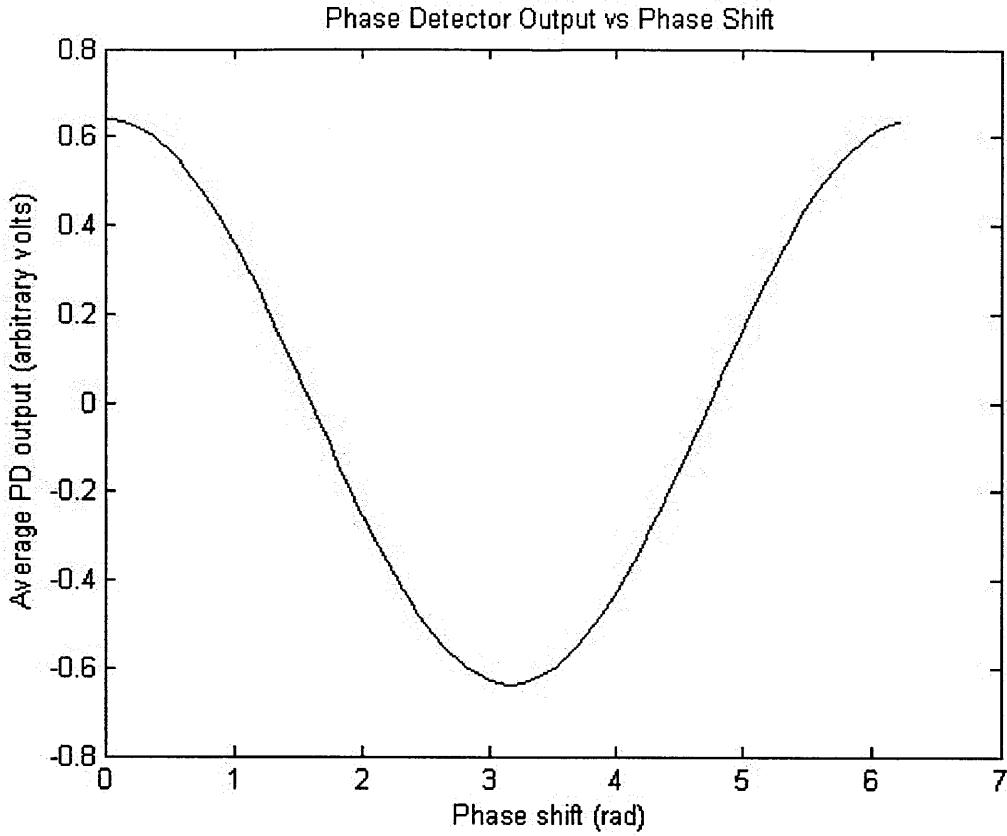


Figure 3-13: Phase Detector Discriminant

the PD output is 0 when the signals are out of phase by $\frac{\pi}{2}$ or $\frac{3\pi}{2}$ radians. The maximum value occurs at a phase shift of 0 or 2π radians and the minimum at π radians. The maximum and minimum values depend on the amplitude of the input signal, and will be equal to the magnitude of the signal's half-cycle average. This is equivalent to mixing the signal with a sine wave of amplitude $\frac{4}{\pi}$ (the fundamental frequency component of the square wave). If the input amplitude is V_i , then the output will vary between $\frac{2V_i}{\pi}$ and $-\frac{2V_i}{\pi}$ over a range of phase error from 0 to π . Thus, the phase detector gain is:

$$K_d = \frac{4V_i}{\pi^2} \quad (3.17)$$

Note that the PD output is continuous and periodic with period 2π . This means that K_d , the “slope” of the phase detector characteristic, can be either positive or

negative, depending on the relative phase shift between the signal and reference.

3.3.2 Loop Filter

The primary purposes of the loop filter are to set the system's bandwidth, while ensuring its stability, and, if desired, to ensure there is zero phase error between the transmitted clock and recovered clock. We also built in some extra functionality, such as offset nulling, a VCO pretune capability, and a switchable integrator for improved acquisition range. A schematic of the loop filter is provided in Figure 3-14.

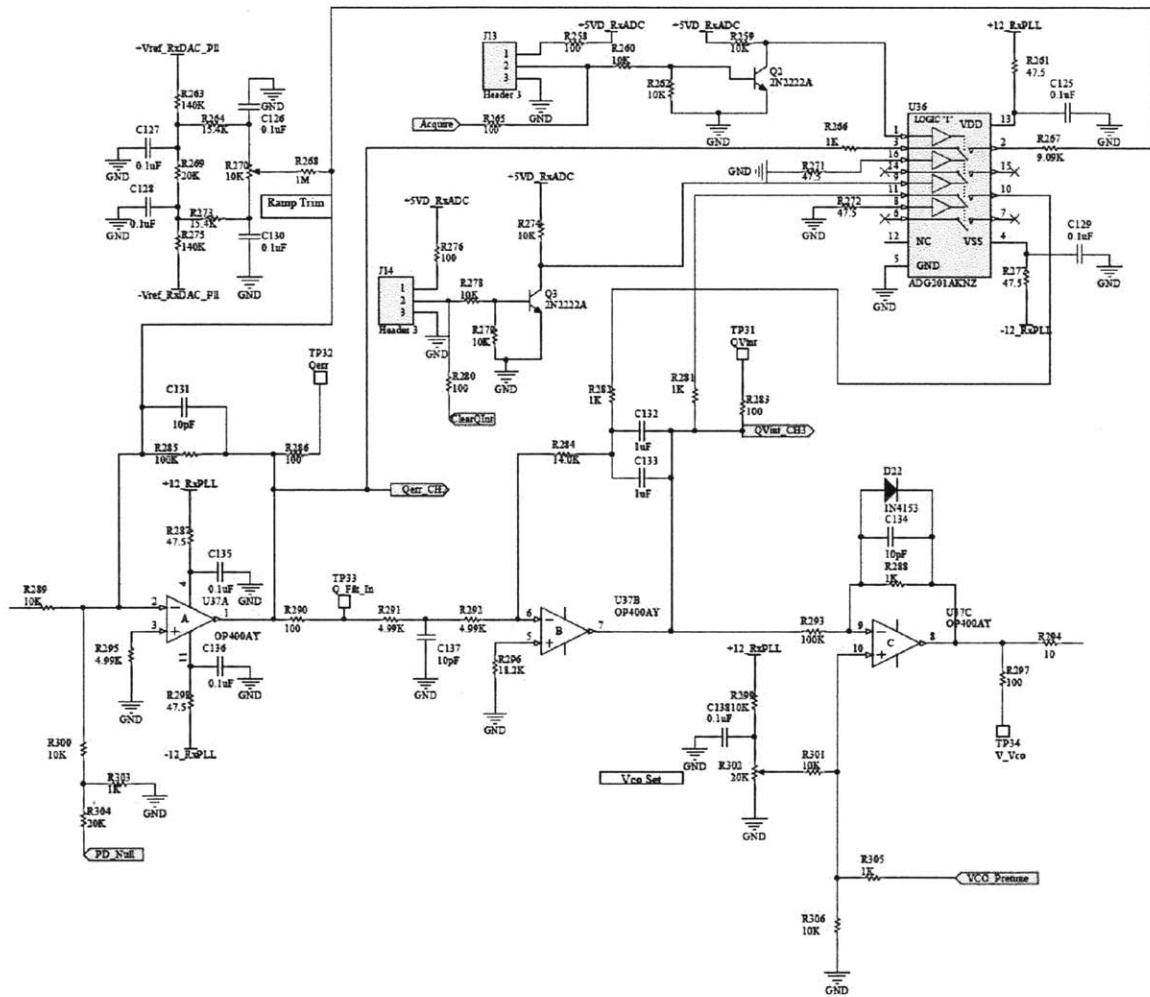


Figure 3-14: Loop Filter Circuit Schematic

The input to the loop filter is applied at resistor R_{289} . The op amp labeled U37A

applies a gain of -10 to the input signal, and also serves as a summing node for the phase detector nulling capability. A DC offset voltage can be applied from either the PD_Null input, which is driven by a DAC, or from the node labeled “Ramp Trim”, which is connected to a potentiometer. This nulling capability is useful for tuning out the phase detector’s response to noise from amplified spontaneous emission in the optical preamplifier, which tends to increase DC offset. This offset competes with the detected phase and will push the integrator to one of its rails, leaving the VCO at the wrong frequency. This nulling scheme is particularly helpful at lower signal powers and data rates.

The next op amp, U37B, is configured as an inverting integrator. This integrator ensures that there is zero phase error between the transmitted clock and the recovered clock. R_{284} adds a zero to the loop transmission and ensures that it remains stable in the presence of two integrators.

The final op amp, U37C, limits the range of voltages that can be applied to the VCO. Diode D22 provides unipolar operation required by the VCO, and R_{288} and R_{293} set a gain of $\frac{-1}{100}$, so that the control voltage range is limited to 0 to about 100mV, which corresponds to about a 30kHz tuning range. The integrator’s command is added to the input from VCO_Pretune or VCO_Set, either of which can be used to preset the nominal VCO operating frequency or command a sweep of many frequency ranges, for example during the acquisition process.

We gain another capability through the use of the ADG201 analog switch – we can reduce our loop to first order during acquisition. One of the limitations of a second-order PLL is that its acquisition range is very limited. The ADG201 is configured to short out the integrating capacitor on U37B and reduce the feedback resistance on U37A upon receiving a command either from the “Clear_QInt” (clear quadrature integrator) and “Acquire” digital control lines, or from the manual jumper connections. Enabling the switches greatly reduces loop gain and temporarily enables operation as a first-order loop. This greatly expands the PLL’s acquisition range, at the expense of non-zero phase error. However, once the loop has locked, we can command the ADG201 to open and restore second-order operation.

3.3.3 Dynamic Analysis

Loop dynamics, particularly bandwidth, are a critical factor in clock recovery performance. Having analyzed each component of the PLL, we can now collect terms and develop a feedback block diagram of the entire system. As mentioned before, the three components of interest are the VCO, the phase detector, and the loop filter.

As we saw in chapter 2, the VCO can be modeled with the following two equations:

$$\Delta\omega_o = K_o(v_c - V_{co}) \quad (3.18)$$

$$\theta_o = \int \Delta\omega_o dt \quad (3.19)$$

Using the knowledge that our VCO output frequency changes by 30kHz for a 100mV change in control voltage, we can calculate that K_o is about 300kHz/V. We can also solve for the output phase in terms of the input control voltage:

$$\theta_o = \int K_o(v_c - V_{co}) dt \quad (3.20)$$

If we just take the “AC” part of this equation (by removing V_{co}), we can represent the transfer function from control voltage to output phase in the Laplace domain as

$$\frac{\theta_o}{v_c}(s) = \frac{K_o}{s} \quad (3.21)$$

where, for our VCO, $K_o = 300\text{kHz/V}$. In the “Phase Detector” subsection, we calculated K_d of the phase detector to be

$$K_d = \frac{4V_i}{\pi^2} \quad (3.22)$$

As explained in the ”Automatic Gain Control” section, V_i is fixed to be 31mV. However, this is the amplitude just after the VGA. The signal applied to the PLL’s mixer is given an additional gain of about 20, so that V_i is actually 620mV. This means $K_d = \frac{2.48V}{\pi^2}$. The loop filter implements the transfer function

$$A(s) = \frac{\frac{-1}{10}(0.028s + 1)}{0.02s} \quad (3.23)$$

Note that if we were to cascade these three elements as they are, the loop would exhibit positive feedback and be unstable. Recall, however, that the sign of K_d can be positive or negative. The loop will naturally seek out an operating point which is stable, meaning it will settle on the correct “slope” of the phase detector discriminant so that negative feedback is maintained. Having addressed this concern, the loop transmission is:

$$L(s) = \frac{211s + 7538}{0.02s^2} \quad (3.24)$$

The bode plot of this loop transmission is shown in Figure 3-15. As can be seen in the plot, the crossover frequency is 10.6krad/s, or about 1.7kHz, and the phase margin is close to 90 degrees.

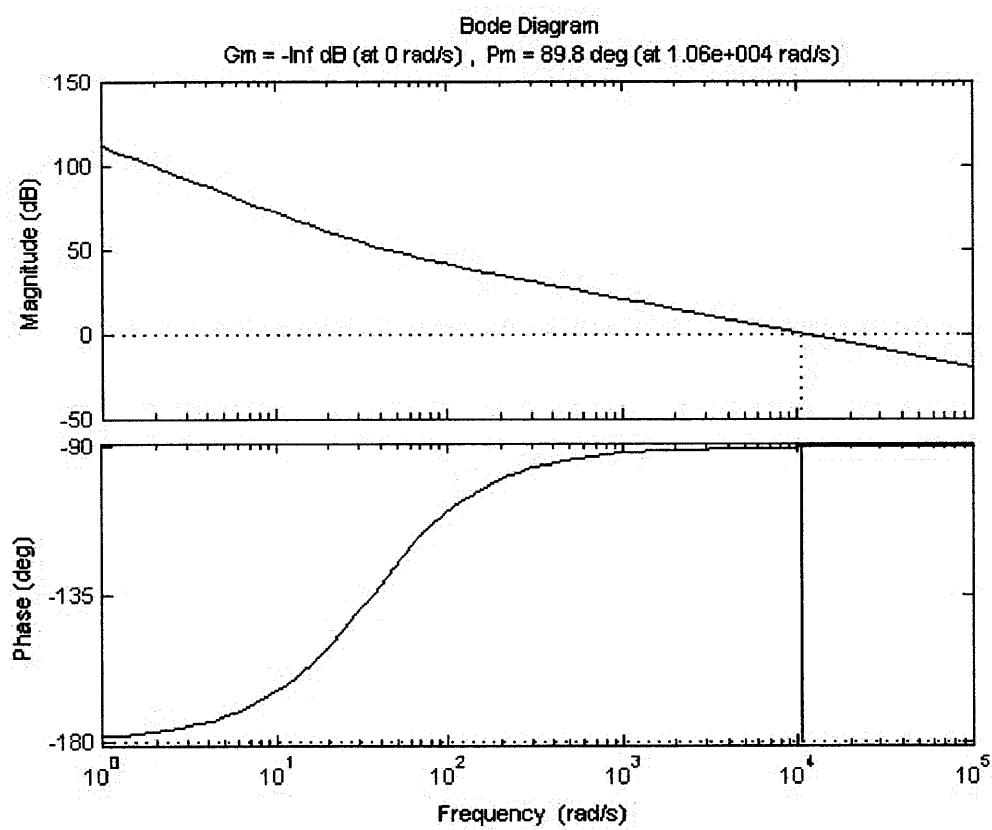


Figure 3-15: Loop Transmission Bode Plot

Chapter 4

Minimum-Rate Clock Recovery System Design

4.1 Overview

The minimum-rate clock recovery system is meant to support only the lowest data rate used by the communication link. The minimum-rate design is based heavily on the multi-rate design, with a few important distinctions. This system uses a more conventional homodyne detection scheme, which means that it mixes the RF input directly down to baseband (specifically, down to DC when the PLL is locked). The lack of an IF signal makes AGC more difficult. The high peak power to average power ratio in the recovered waveform makes it likely that an RF amplifier used to control average signal power will quickly be driven into saturation by the high peak power. This system therefore uses only a PLL; however, it is assisted by a noise gate. Communications at the lowest data rate over this particular link are the most susceptible to phase jitter and so stand to benefit the most from the use of a noise gate. A block diagram of this system is provided in Figure 4-1.

The minimum-rate clock recovery system takes the loop filter and local oscillator from the multi-rate design, replaces the phase detector with an ultra-wide bandwidth multiplier, and adds a circuit that we call a “signal modifier”. The signal modifier derives a gating waveform from the local oscillator and applies it to one of the mul-

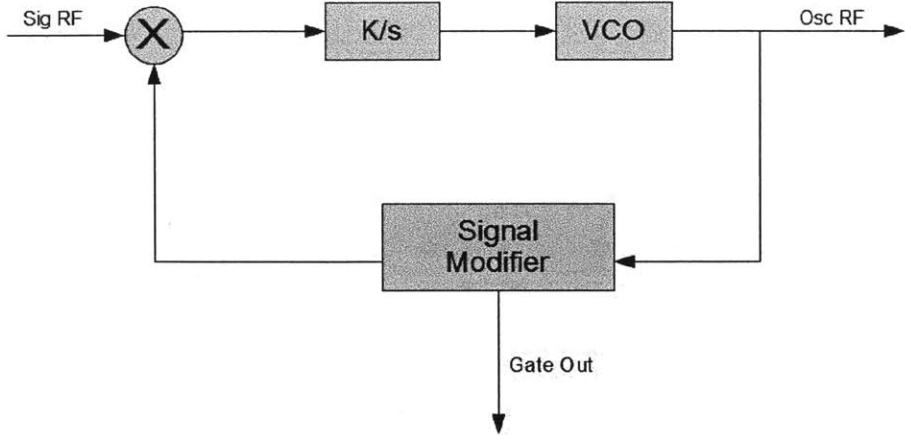


Figure 4-1: Minimum-Rate Clock Recovery Block Diagram

tiplier inputs, effectively mixing this waveform with the incoming RF signal. The signal modifier and multiplier together form the noise gate - when the loop locks, the phase detector is shut down during the periods for which the burst signal is not present.

4.2 Loop Filter

The minimum-rate system's loop filter is similar to that of the multi-rate system. Its schematic is provided in Figure 4-2.

As in the multi-rate design, the loop filter has a switchable integrator, and a programmable loop gain for acquisition or locked operation. It also retains the offset-nulling and VCO pretune capabilities of the previous design. However, the loop gain has to be increased in order to adjust for the reduced K_d of the phase detector. The loop filter's nominal transfer function is

$$A(s) = \frac{\frac{-1}{10}(0.028s + 1)}{0.02s} \quad (4.1)$$

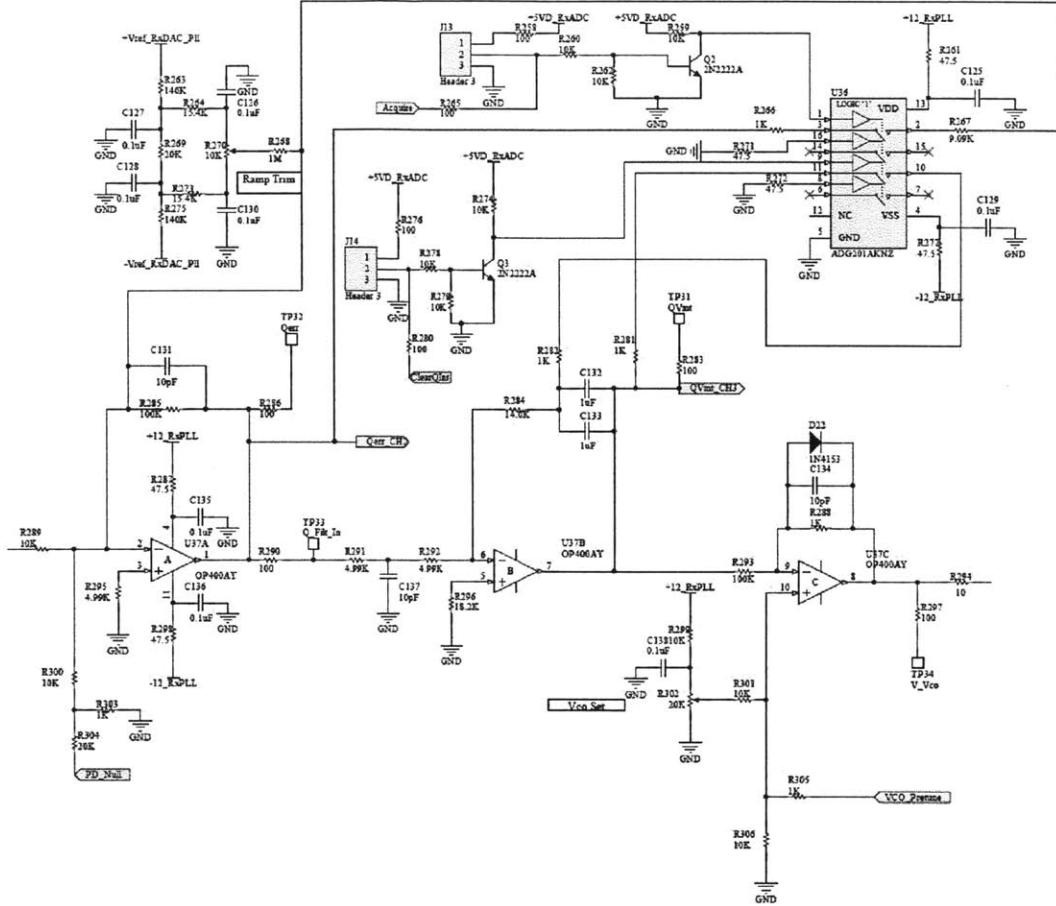


Figure 4-2: Minimum-Rate Loop Filter Circuit Schematic

4.3 Phase Detector

The phase detector in the minimum-rate system is implemented as an analog multiplier. We chose the ADL5391 multiplier for its wide bandwidth of DC - 2GHz. Wideband operation is critical, because we are mixing our gating waveform directly with the received RF signal. DC operation is also crucial, since we are operating the clock recovery system as a homodyne detector, which mixes down to DC when the loop is locked. Additionally, we chose to use a multiplier because it can be commanded to block any input from reaching its output. The active double-balanced mixer does not do this - it will always pass its input in one polarity or the other. In order for gating to be effective, we have to be able to block the noise that is present in the absence of a signal.

The multiplier's operation as a phase detector is very similar to that of the active double-balanced mixer. The two inputs are multiplied together, and the average of the detector output drives the loop filter. However, in this case, the output of the signal modifier is the equivalent of the local oscillator, and the RF input signal is mixed directly against it.

The signal modifier derives a gating signal from the local oscillator and applies it to the phase detector so that only the signals (and noise) present in the burst transmission window will drive the phase-locked loop. Since the clock recovery system is designed to operate at a specific data rate, the size of the burst window is known. Using this knowledge, we can develop a waveform that drives the PLL to seek the "temporal median" of the burst signal window and reject the noise present outside this window. The waveform is shown in the plot in Figure 4-3.

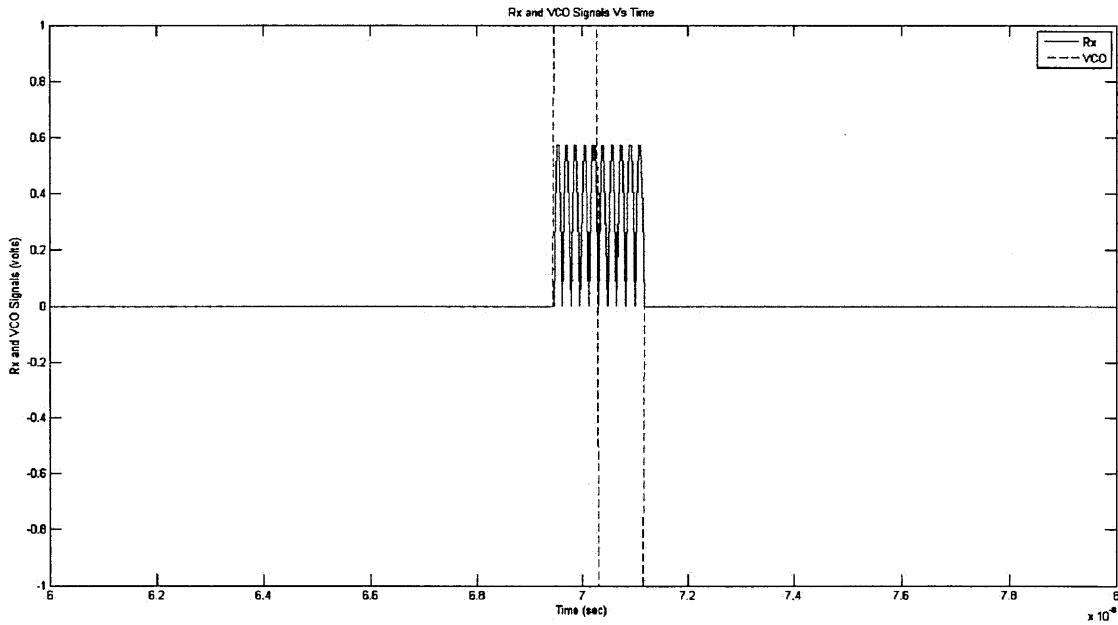


Figure 4-3: Signal Modifier Waveform Plot

The signal modifier waveform is the dashed line, and the incoming RF pulses are represented by the solid line. When signal modifier is applied to the multiplier, the input signal will be multiplied by 1, -1, and 0 as dictated by the modifier waveform. When the modifier waveform is aligned with the burst window, half of the RF pulses

will be multiplied by 1 and half will be multiplied by -1, resulting in an average output of 0. Any deviation from this point will produce a net positive or negative average output that will tend to correct the misalignment. The multiplier discriminant for all possible alignments between the modifier waveform and an example burst signal is plotted in Figure 4-4.

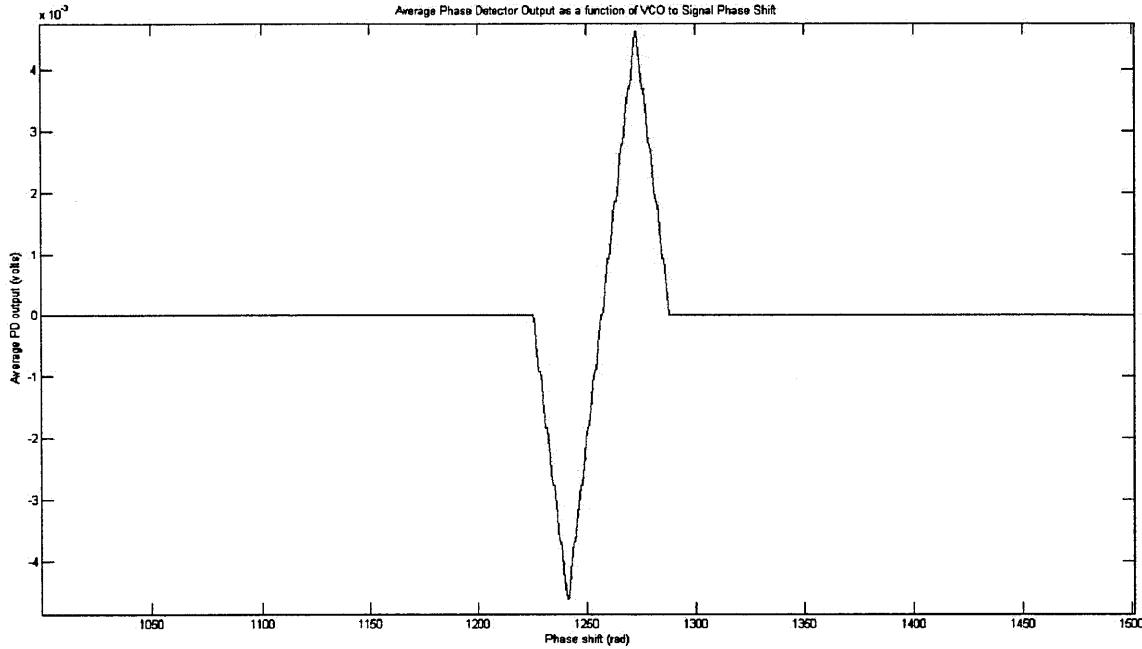


Figure 4-4: Signal Modifier Discriminant

When the modifier and the signal burst are aligned, any noise outside the signal burst will be multiplied by 0. The noise will not be completely removed - the actual amount of attenuation will depend on the capability of the multiplier. The ADL5391 offers about 30dB isolation from input to output.

The phase detector's average output depends on the amplitude of the input RF signal. Additionally, the average will be lower in this implementation due to the large “dead time” between signal bursts. If the RF input amplitude is V_i , and the dead time is D times the length of the signal burst, the average phase detector output will vary between $\pm \frac{2V_i}{(D+0.5)\pi}$. The extra factor of 0.5 is due to the fact that the maximum and minimum occur when the signal modifier waveform overlaps halfway with the signal burst, effectively interacting with only half of the RF signal. The range of phase over

which the discriminant has its minimum and maximum is a function of the number of clock “pulses” contained within the signal burst. Say the signal contains N pulses - this means the range of phase, with respect to the burst window, over which the discriminant maximum and minimum occur (which is $-\frac{\pi}{2}$ to $\frac{\pi}{2}$) corresponds to N clock periods. The effective phase range is then $N\pi$ - this reduces the phase detector gain by a factor of N . The phase detector gain is

$$K_d = \frac{4V_i}{(D + 0.5)N\pi^2} \quad (4.2)$$

which is a factor of $(D + 0.5)N$ lower than in the multi-rate system.

4.4 Signal Modifier

The signal modifier waveform is generated by the circuit shown in Figure 4-5.

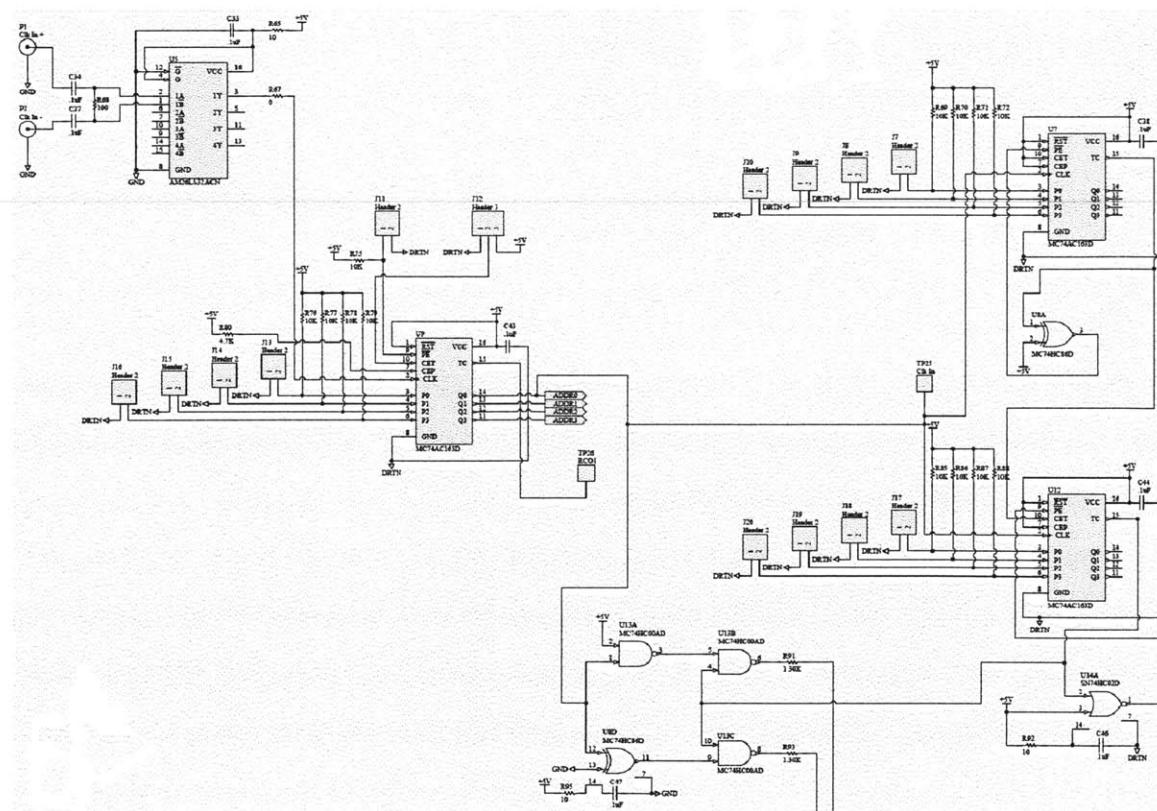


Figure 4-5: Signal Modifier Circuit Schematic

Not pictured in the schematic is the Centellax UXN14M9P programmable frequency divider, which divides the local oscillator frequency by the number of optical pulses in one burst window at the minimum data rate. The resulting signal is connected to the “Clk In +” and “Clk In -” differential inputs of the signal modifier. The AM26LS32ACN is a differential receiver IC, which converts the differential clock into a single-ended signal. The signal modifier circuit uses three MC74AC163D binary counters as programmable frequency dividers to generate a window signal which will exactly match the burst transmission window when the PLL is locked. In order to understand how the window is generated, it is necessary to understand the operation of these counters. A schematic representation of the MC74AC163D is provided in Figure 4-6.

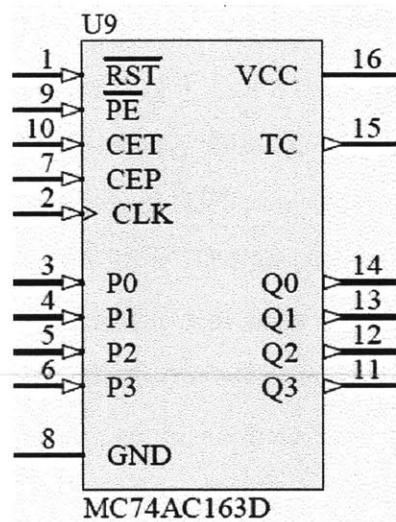


Figure 4-6: MC74AC163D Counter

The MC74AC163D is a 4-bit binary synchronous counter. On each rising edge of the CLK (clock) input, the internal count is incremented and outputs Q0 through Q3 are updated to reflect the binary counter value. The counter is called “synchronous” because all four outputs change simultaneously on each rising clock edge. The counter increments until it reaches a maximum value of 16, at which point it pulses its TC, or “terminal count,” output and resets to zero. The circuit is designed so that the width of the TC pulse is the same as one clock pulse width. The RST (reset) input will

reset the counter state back to zero if it is pulled low. The PE, or “parallel enable,” input allows the counter to be pre-programmed. When PE is pulsed low, the values present at the P0 through P3 inputs are loaded into the counter, and counting begins from that value. The CEP and CET (count enable parallel and count enable trickle) inputs are used to inhibit the counter. It will not count if either of these inputs is held low.

The first counter in the signal modifier circuit, labeled U9, is configured as a frequency divider with a fixed divide ratio of 2. J11 is not installed, so PE is always held high. J12 is installed so that it holds CET high. We take the output from Q0, which will toggle on every clock edge. Using the signal from the differential receiver as the CLK input, Q0 will output a signal at half its frequency. This counter will ignore any external programming and will run continuously.

The two remaining counters, U7 and U12, are used in conjunction as a programmable frequency divider. They both receive the Q0 output from U9 at their CLK inputs. Both have their RST and CEP inputs tied high. However, U12’s CET input is driven by U7’s TC output, and U7’s CET input is tied high. This configuration allows the counters to be used in tandem in order to achieve an extended counting range. Each time U7 reaches its terminal count, its TC output pulses high for one clock period, allowing U12 to count once. In this way, U12 functions as the upper 4 bits in an 8-bit counter. Additionally, both U7’s and U12’s PE inputs are driven by the inverse of their TC outputs. The XOR gate, U8A, and the NOR gate, U14A, are both configured as inverters by tying one of their inputs high. This connection causes the counters to be preset each time they reach their terminal count, allowing them to count the same fixed number of steps before the terminal count is reached. We can use this configuration to program frequency division ratios from 1 to 255.

Consider, for example, that we populate the jumpers so that U7 will be preloaded with a value of A , and U12 with a value of B . U7 will count $(16 - A)$ times before reaching its terminal count and being reset to a count of A . For each terminal count that U7 reaches, U12 is allowed to count once. After $(16 - B)$ such counts, U12 will

reach its terminal count and be reset to a count of B . Thus, for every $(16 - A) * (16 - B)$ input clock pulses, U12's TC output will pulse once. The width of the TC pulse will be the same as that of the Q0 input clock pulse, and the frequency of TC pulses will be $(16 - A) * (16 - B)$ times less than that of Q0. We can generate a gating waveform to match the burst window (when the PLL is locked) by setting the counters to divide Q0 in frequency by $\frac{D}{2}$ (where D is the reciprocal of the duty cycle of the burst window).

In order to generate a bipolar waveform to mix against the input RF signal, we use the logic circuit shown in Figure 4-7.

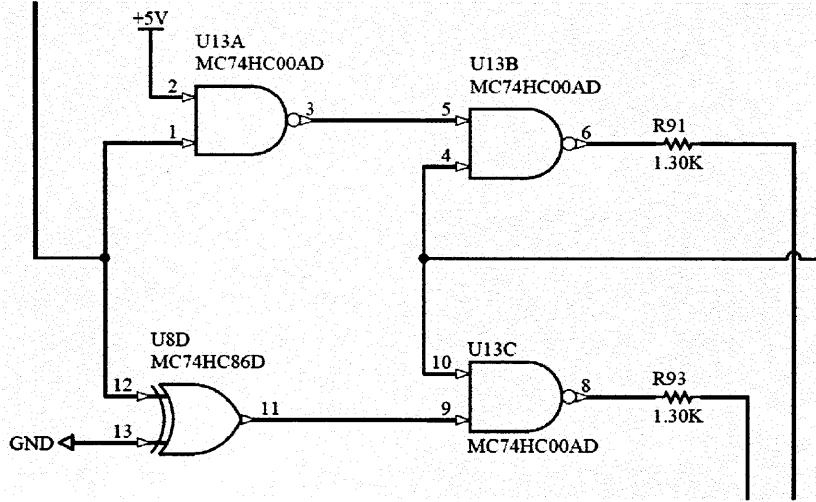


Figure 4-7: Signal Modifier Logic Circuit

The input to U13A and U8D is the Q0 output of the fixed-ratio counter. The input to U13B and U13C is the TC output of the variable-ratio counters, specifically, that of U12. The output of U13B and U13C are pulses of the same width as the Q0 signal and the same frequency of the TC output, but delayed so that one occurs immediately after the other. These pulses are coupled into the differential input of the ADL5391 multiplier. The resulting differential input is a positive-going pulse, immediately followed by a negative-going pulse, and zero otherwise. The creation of these pulses is illustrated in Figure 4-8.

The resulting pulses are differentially coupled into the multiplier, so that the nominal input to the multiplier is 0. The “positive” pulse is coupled into the noninverting

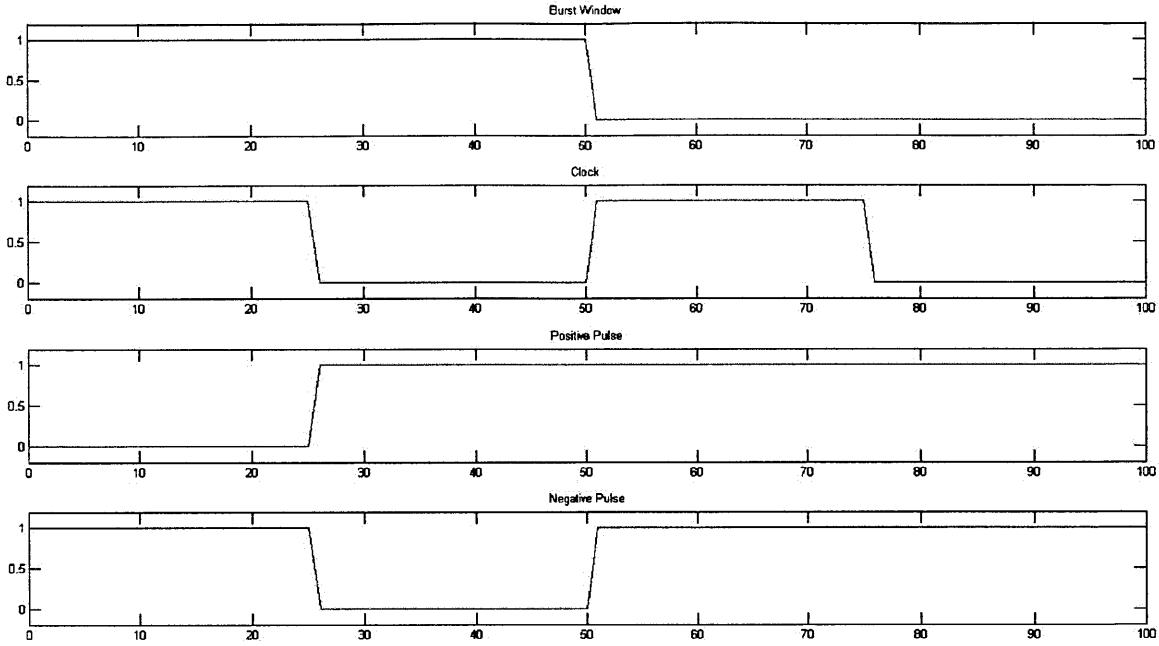


Figure 4-8: Signal Modifier Logic Illustration

input and the “negative” pulse is coupled to the inverting input, so the effective differential input is the signal modifier waveform we desire.

4.5 Dynamic Analysis

The loop transmission of the minimum-rate system is composed of the loop filter transfer function, the phase detector gain, and the VCO transfer function. The phase detector gain is

$$K_d = \frac{4V_i}{(D + 0.5)N\pi^2} \quad (4.3)$$

which, for a nominal input amplitude of 300mV and our chosen values of D and N, calculates to $K_d = 8.745 \times 10^{-6}$. This is a factor of 27,808 lower than the multi-rate system’s K_d , so the loop filter gain will have to be increased significantly in order to compensate. The loop filter’s transfer function is then

$$A(s) = \frac{\frac{-27,808}{10}(0.028s + 1)}{0.02s} \quad (4.4)$$

The VCO's transfer function can be expressed as

$$\frac{\theta_o(s)}{v_c} = \frac{K_o}{s} \quad (4.5)$$

where, for our VCO, $K_o = 300\text{kHz/V}$. From these terms, we get the following loop transmission:

$$L(s) = \frac{204.3s + 7295}{0.02s^2} \quad (4.6)$$

The bode plot of this loop transmission is shown in Figure 4-9. The crossover frequency is 10krad/s , or about 1.6kHz , and the phase margin is close to 90 degrees.

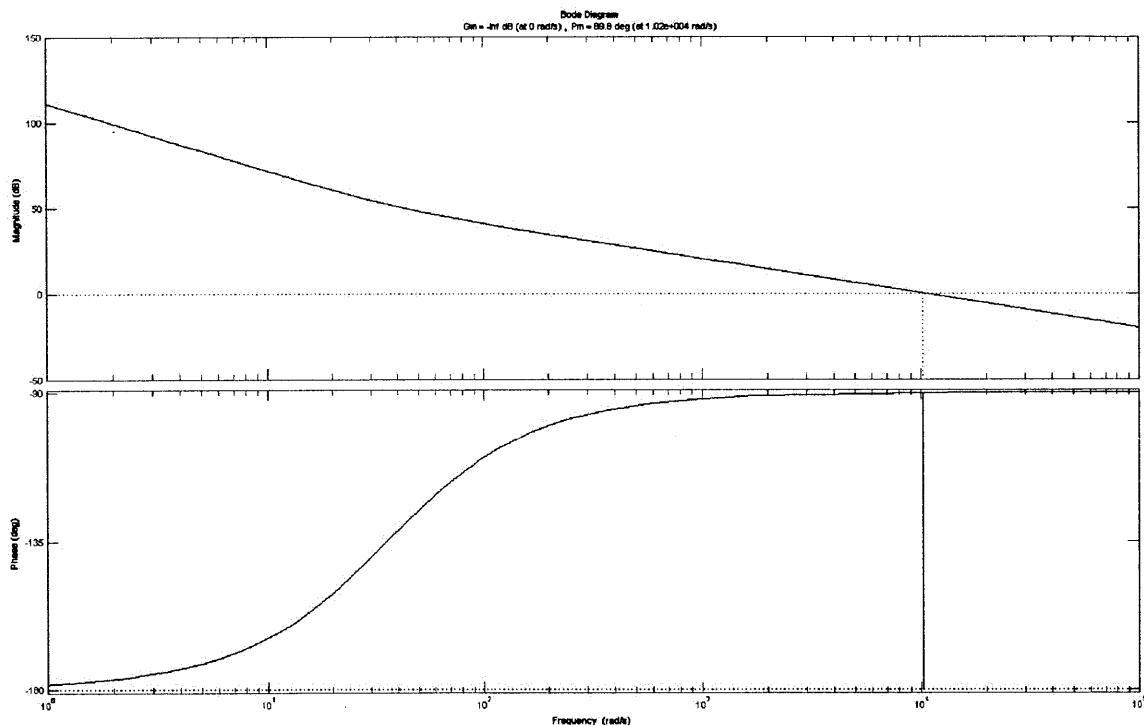


Figure 4-9: Minimum-Rate Loop Transmission Bode Plot

Chapter 5

Data Acquisition and Analysis

5.1 Clock Recovery System Evaluation

There are several key performance metrics to track in the evaluation of our clock recovery systems. These include bandwidth, disturbance rejection, lock range, system integration, and phase jitter in the recovered clock. The PLL's loop bandwidth determines the system's ability to reject noise and to improve the VCO's phase noise characteristic. We can determine bandwidth from the system's loop transmission, but this is difficult to measure directly. Instead, we can inject a sinusoidal oscillation into a reference VCO's control voltage and measure degree to which the response in the phase detector's output voltage is attenuated. This is known as the system's "rejection" curve. The measured rejection is shown in Figure 5-1.

The rejection curve is related to the loop transmission by the equation

$$R(s) = \frac{1}{1 + L(s)} \quad (5.1)$$

where $L(s)$ is the loop transmission. However, the rejection curve in Figure 5-1 represents attenuation of a disturbance in frequency, rather than phase. In order to obtain the loop transmission, we must first differentiate the frequency rejection curve, which gives us the phase rejection curve shown in Figure 5-2.

Finally, if we transform the phase rejection curve according to the equation

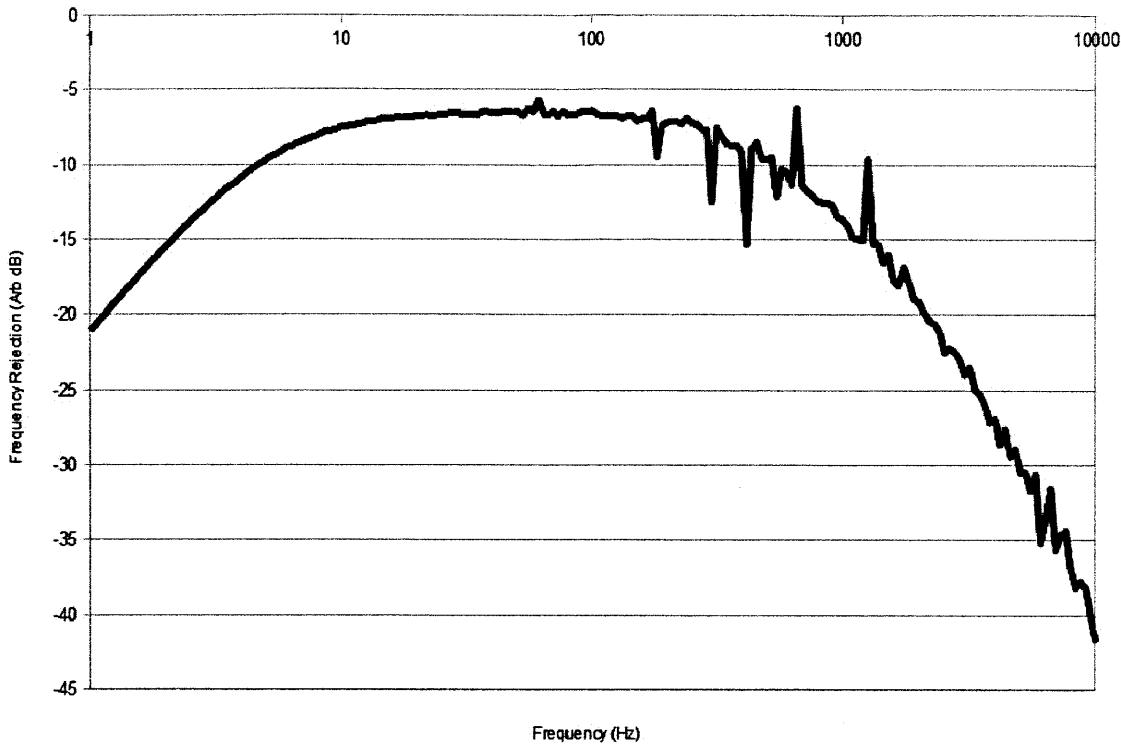


Figure 5-1: Minimum-Rate System Frequency Rejection Plot

$$L(s) = \frac{1}{R(s)} - 1 \quad (5.2)$$

the result is the loop transmission. Since the minimum-rate and multi-rate systems are designed to have roughly the same loop transmission, their frequency and phase rejection plots will also be similar. The measurements shown were taken with the minimum-rate system. The measured loop transmission is shown in Figure 5-3.

Maintaining low phase jitter in the PLL is critically important to clock recovery. Jitter is a function of the PLL's SNR, which we aim to improve through the use of noise gating. Phase jitter can be calculated from phase noise measurements of the recovered clock signal. In order to form a basis for comparison, we first measure the phase noise of an “unlocked” PLL, which exposes the phase noise inherent to the VCO. This measurement is shown in Figure 5-4. This plot represents a sort of “worst case” phase noise, which is reduced by the PLL’s loop gain when the loop is locked.

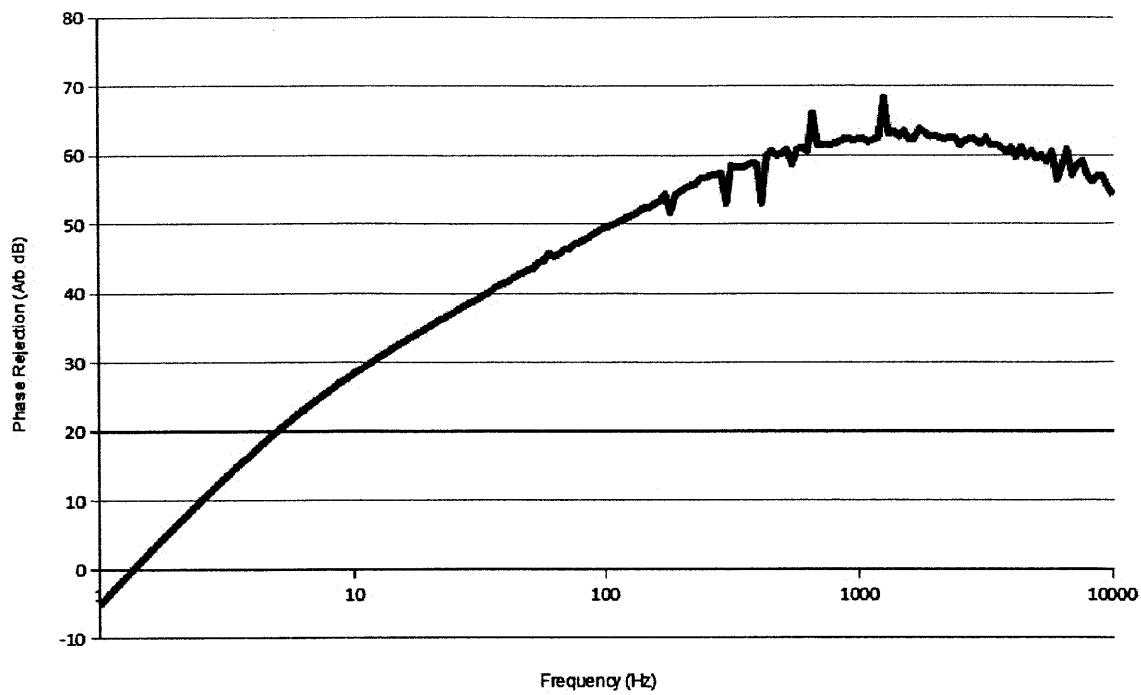


Figure 5-2: Minimum-Rate System Phase Rejection Plot

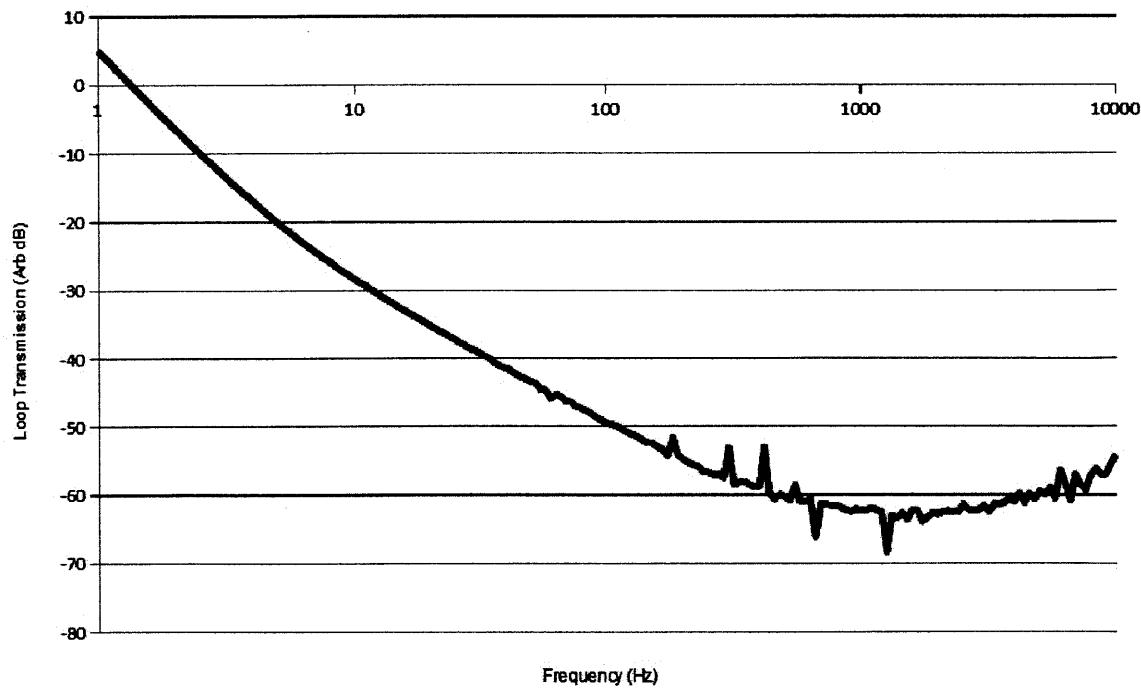


Figure 5-3: Minimum-Rate System Loop Transmission

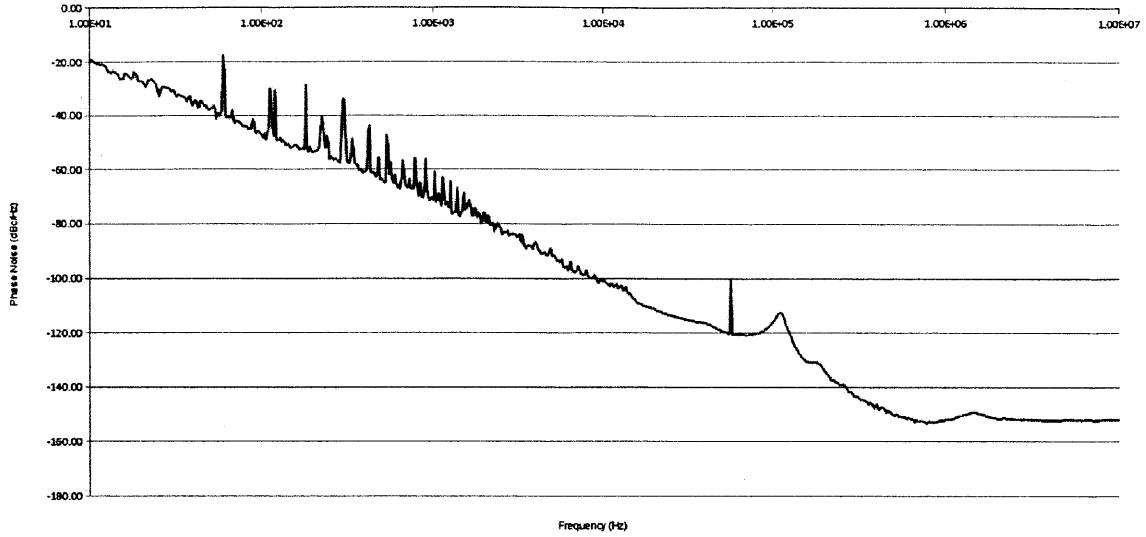


Figure 5-4: Phase Noise Measurement with Loop Unlocked

The “best case” phase noise is that which is inherent to the signal source, in our case an RF signal generator. Its phase noise plot is shown in Figure 5-5. This represents the lowest phase noise the loop will be able to achieve.

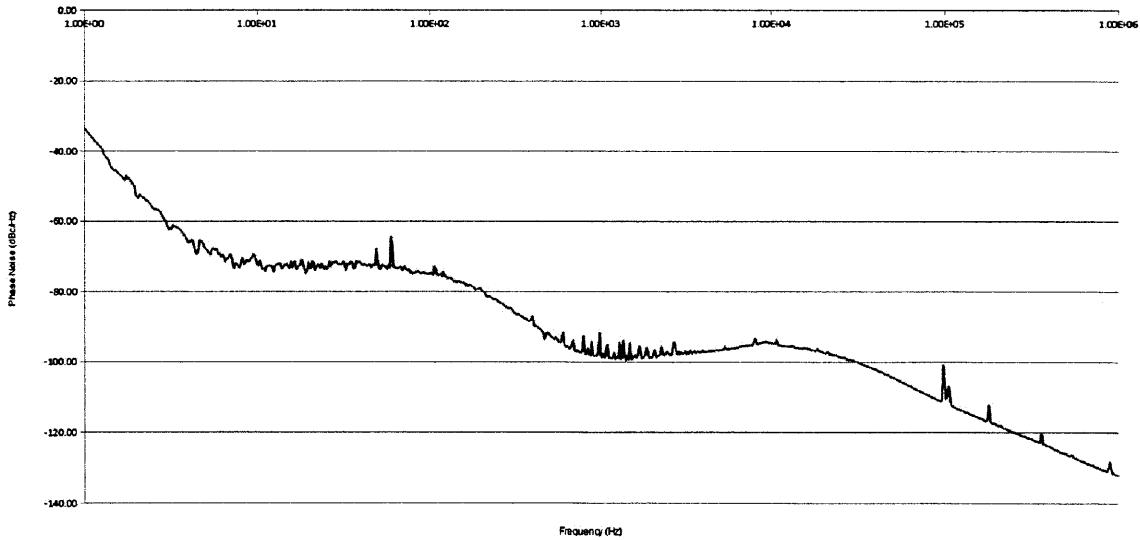


Figure 5-5: RF Generator Phase Noise Measurement

We next measure the phase noise in the recovered clock with the noise gate enabled and a continuous-wave input. This measurement is a bit more optimistic than the

results we would have with a burst signal input, but demonstrates that gated system generally works as expected. The results are shown in Figure 5-6.

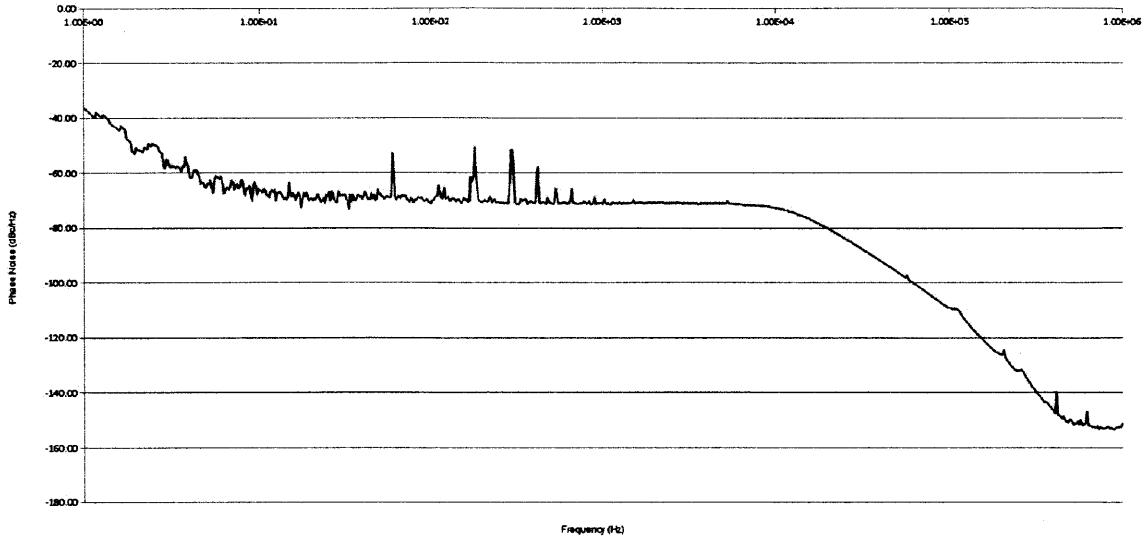


Figure 5-6: Phase Noise Measurement with Gating Enabled and CW Input

These plots illustrate how the loop transmission rejects the phase noise inherent to the VCO, within the system's bandwidth. Additionally, the gated system with continuous-wave input comes very close to the phase noise of the transmitter itself. However, the gated measurement had to be run with an input that was not burst-modulated, due to difficulties in constructing a reliable burst-mode transmitter. As a result, the performance may be somewhat optimistic.

We also captured waveforms which illustrate the operation of the signal modifier and phase detector in the minimum-rate system. Figure 5-7 shows the positive- (upper middle trace) and negative-going (top trace) pulses that are coupled into the multiplier, and the resulting differential input (lower middle trace). The bottom trace is the burst signal input.

Figure 5-8 shows the output of the phase detector when the loop is locked. The top waveform is the gating signal, and the bottom is the burst signal.

Figure 5-9 is a phase detector discriminant. We measured this by disabling the integrator and tuning the VCO slightly off from the target frequency (through the VCO pre-tune input), allowing the burst signal and gating window to sweep past each

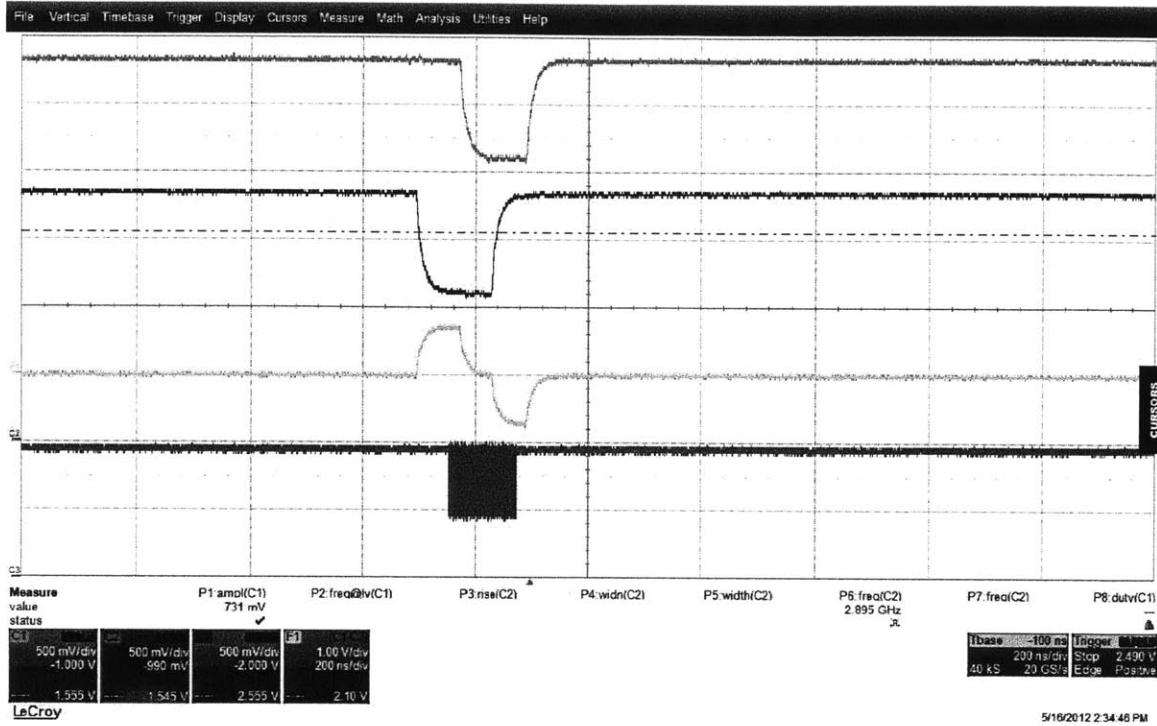


Figure 5-7: Phase Detector Differential Input

other at some rate. We then monitored the phase detector output through a low-bandwidth amplifier, in order to extract its average output value as the phase error is swept.

Finally, Figure 5-10 illustrates the stability of the gating window alignment. It is a persistent plot of the signal burst window (top trace), the gating window (middle trace), and signal burst (bottom trace).

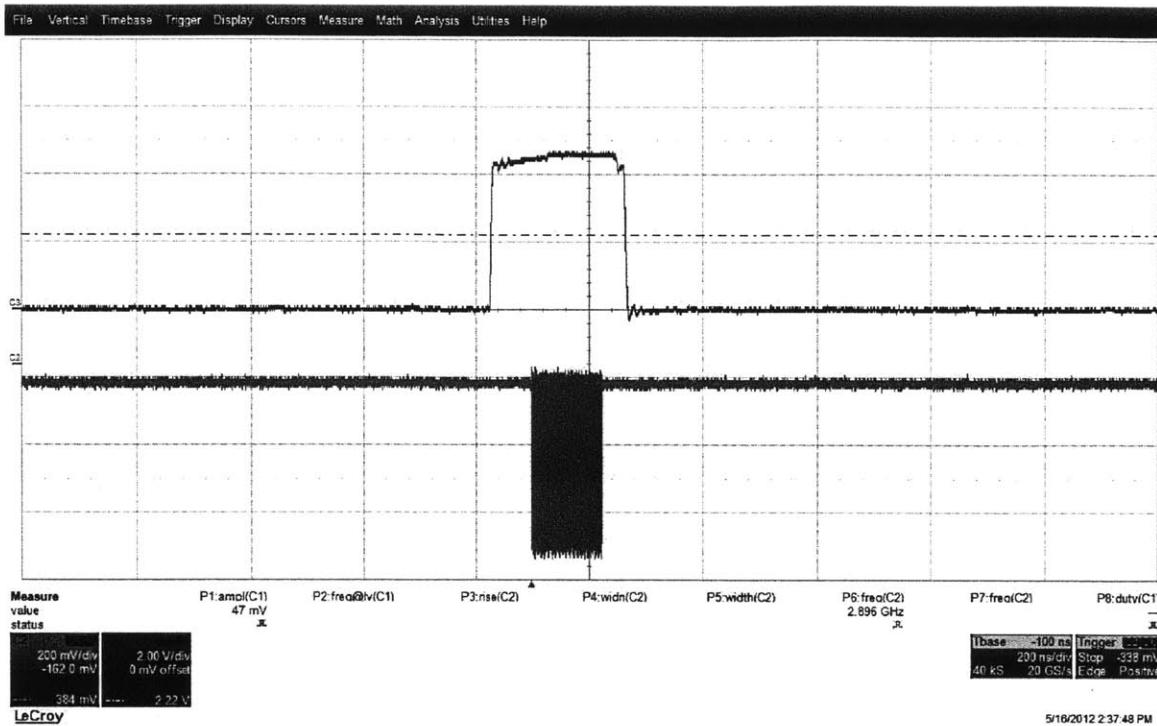


Figure 5-8: Phase Detector Output

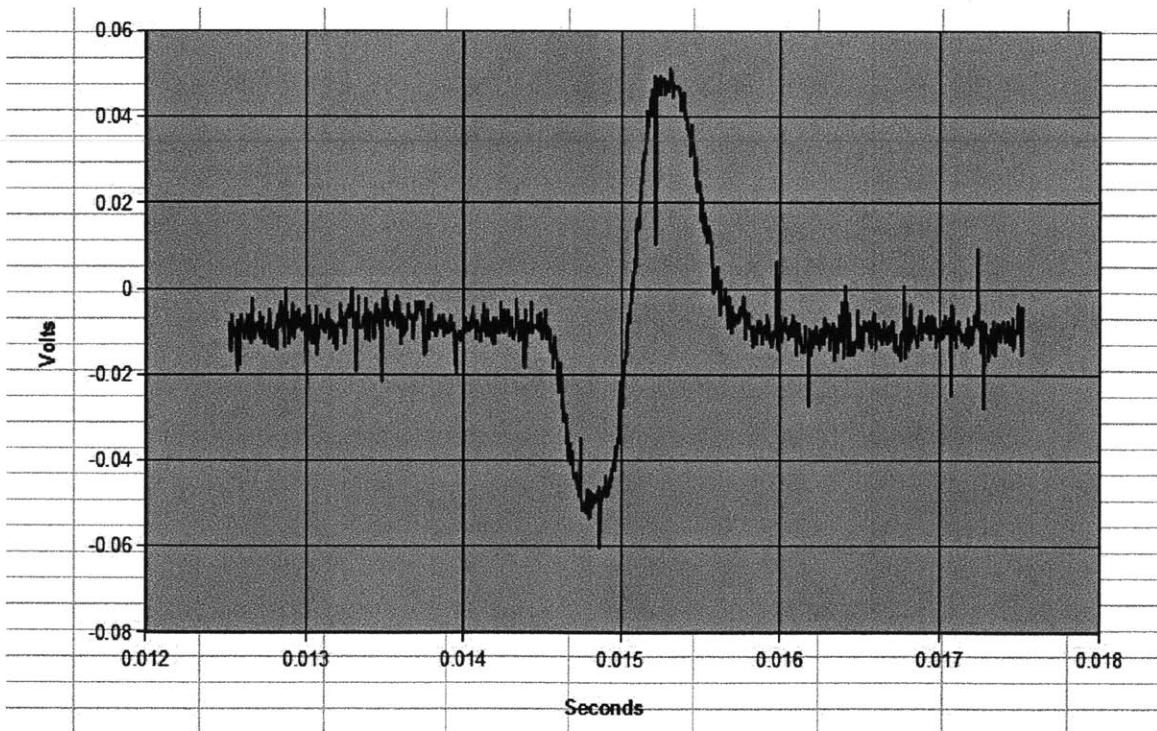


Figure 5-9: Phase Detector Discriminant

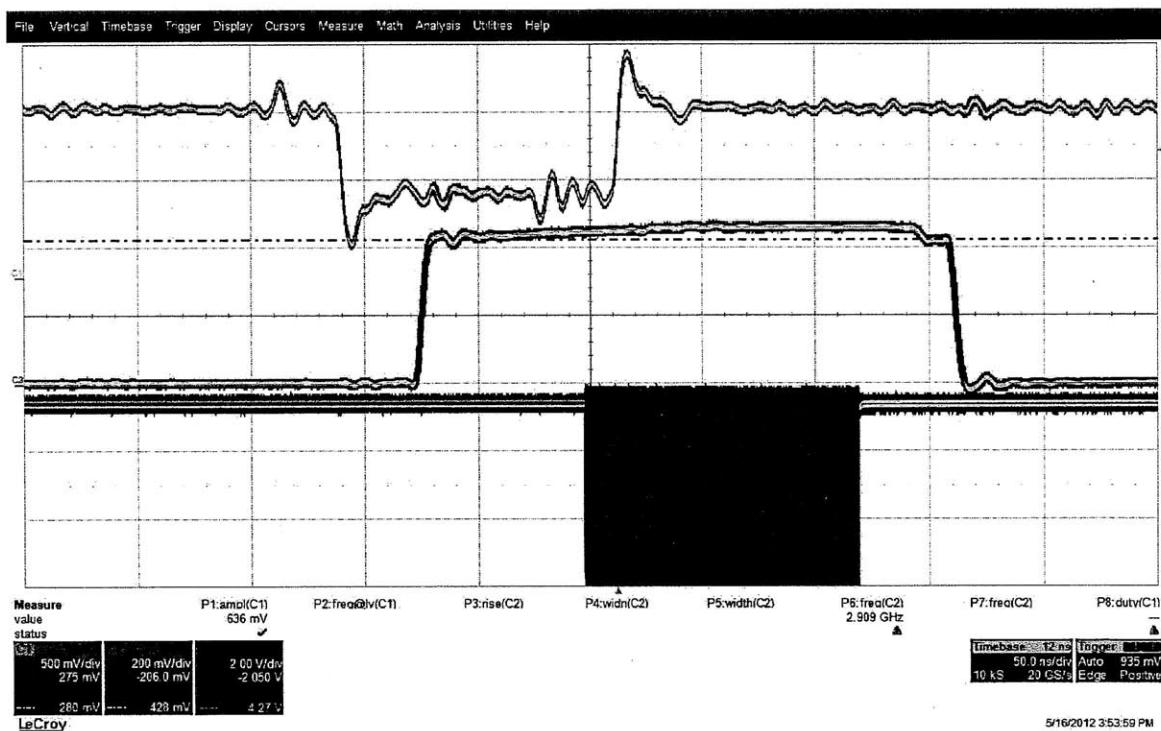


Figure 5-10: Persistent Plot of Gating Window Alignment

5.2 Future Work

The multi-rate clock recovery system has demonstrated very good phase noise performance and has already been integrated successfully with the communications testbed. It serves an excellent starting point for the minimum-rate design, and can also benefit from gating if we modify the noise gate to work with multiple data rates.

One of our design goals was to apply gating during acquisition - we have already succeeded in this. The gating window itself is intended to be used with a spatial tracker, which maintains the pointing alignment of the optical receiver. This tracker can also benefit significantly from gating, and the phase noise performance is already good enough to realize this goal.

While we have made significant progress in applying gating to the minimum-rate clock recovery system, there is still more to do. There is still some difficulty in achieving sufficient phase noise performance for clock recovery applications with a burst-modulated input. One of the disadvantages of the signal modifier approach is that it greatly reduces phase sensitivity - the phase detector's low output competes with device offsets and DC error. By applying a continuous-wave signal to the multiplier and gating its output, we can greatly increase phase sensitivity.

Our work in the immediate future will be focused on improving the phase noise performance of the minimum-rate system until it is suitable for clock recovery. Our next step is to use the minimum-rate approach as an acquisition aid and use a direct approach (gated) approach once the loop has acquired the burst. We could use the signal modifier for the acquisition stage, and once locked, route the VCO output directly to the multiplier input and apply the gating signal to the multiplier's output. This should allow us to enjoy the benefit of enhanced acquisition, enabled by the signal modifier, while maintaining the phase noise performance of the multi-rate design.

It is clear that gating is a very effective way to increase SNR in a feedback system, but it can also introduce nuances to the system which must be carefully considered. I am optimistic that we will be able to see these benefits applied to clock recovery in the near future.

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