COL215P Assignment 1

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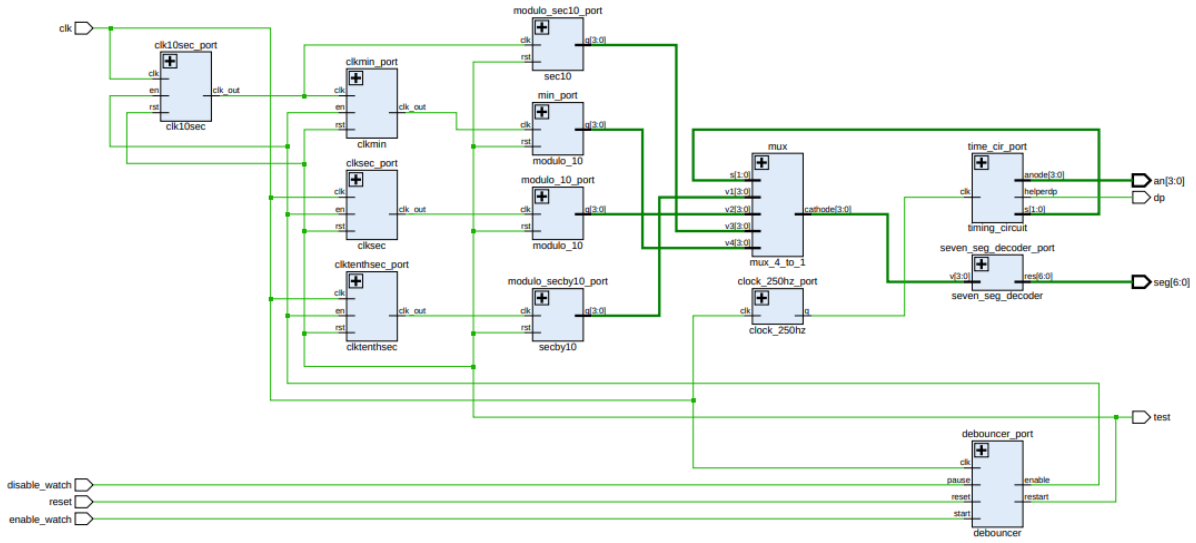

Figure 1: Block Diagram of Stopwatch

1 Overview

The 100MHz clock is feeded to the various clock dividers for minute, 10 seconds, seconds and tenth of second. This gives a clock period of a minute , 10 seconds, seconds and tenth of second respectively. Then their output is passed through the modulo counters and if then fed to the multiplexer and then to the 4 to 7 decoder. The clock is also fed to a clock divider that reduce the frequency of the clock to 250Hz and this signal is fed to the timing circuit which controls the anode. The helper dp is the output for the dots. The test output is for debugging purposes and can be ignore. The explanation for each component is as follows.

2 Design Files Included

2.1 clk10sec , clkmin , clksec, clktenthsec

This modules divides the clock frequency (takes 100Hz as input) and makes them equal to the required frequency and outputs that frequency.

2.2 Modulo

We designed the modulo circuits to take input a clock period and output a 4bit vector. The output is incremented at every rising edge and the output cycles from 0,1,2,3,4,5,6,7,8,9 then back to 0 in case for modulo 10 circuit and similarly for modulo 6 , cycling 0,1,2,3,4,5,0.

2.3 4:1 Multiplexer

It takes minute, 10 seconds, seconds and tenth of second (4 bit vectors) as input and using the select signal it chooses one of them which has to be displayed in that frame of time, and outputs that signal. This signal is then sent to the seven segement decoder.

2.4 Seven Segment Decoder

It is a combinational circuit which takes a 4 bits input from 4 to 1 mux and outputs 7 bits which represent the cathode signals in the LED display. The logic equation of each the output is obtained using following truth table.

A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

Figure 2: Truth Table of Seven Segment Decoder

2.5 Clock divider 250 Hz

It takes 10 MHz clock as input and outputs a clock with frequency 250 Hz. This module maintain a internal counter which toggles the output after every 250000 cycles. This clock's frequency determines the refresh rate of the display which is 4ms.

2.6 Debouncer

The logic for this module is as follow.

2.6.1 start , Pause and enable

Since 2 separate buttons are used for start and pause. We just detected the rising edge when ever one of the button is pressed and then the enable signal becomes 1 or 0 depending upon whether start is pressed or pause is pressed.

2.6.2 reset

When ever the rising edge of the reset button takes place, we again check after 20 cycles of the 100Mhz clock whether the button is still pressed or not. This ensures that the input is stable now thus we can take it as a valid input from the reset button and reset our clock.

2.7 Timing Circuit

This module takes input clock with frequency 250 Hz and outputs 4 anode signals, dp signal and the select signal of the 4:1 mux. This module is used to refresh the led display after every 4 ms.

3 Design Decisions

We decided to not to pause the watch when the reset is used. To stop the watch when it is being reset you need to click on the stop button then click reset