

Statistical Device Simulation and Machine Learning of Process Variation Effects of Vertically Stacked Gate-All-Around Si Nanosheet CFETs

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Abstract—In this study, we report the process variation effect (PVE) including the work function fluctuation (WKF) on the DC/AC characteristic fluctuation of stacked gate-all-around silicon complementary field-effect transistors (CFETs). The PVE affects characteristic fluctuation significantly; in particular, for the variability of off-state current. Owing to the bottom channel of a fin-type, the P-FET suffers from the worst off-state current fluctuation (more than 200% variation) compared to the N-FET. The device variability induced by the WKF is marginal because of amorphous-type metal grains. As input features to an artificial neural network (ANN) model, low and high work function values, as well as parameters of PVE that have prevalent effects on CFET transfer characteristics are further considered and modeled. The estimated values of R²-score prove that the ANN model properly grasps information from the dataset successfully; thus, it can be used to model emerging CFETs for circuit simulation.

Index Terms—Complementary field effect transistors, gate-all-around, nanosheet, process variation effects, work function fluctuation, statistical device simulation, machine learning.

I. INTRODUCTION

LSI technologies with complementary field-effect transistors (CFETs) are quite fascinating due to their high area reduction [1]. Enhanced semiconductor technology nodes enable semiconductor devices to scale up to nanoscale regimes according to Moore's law [1], [2], [3]. Because of severe short channel effects (SCEs), transistors have evolved into three-dimensional

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(3-D) multi-gate structures from conventional two-dimensional (2-D) planar structures [4], [5]. Even though FinFETs have better gate controllability than conventional MOSFETs, their scaling is restricted by fin height and fin width [6], [7]. Due to their superior electrostatics and performance, gate-all-around (GAA) nanowire (NW) and nanosheet (NS) FETs are promising candidates for replacing FinFETs [8], [9]. By folding N-FETs and P-FETs on the same substrate, CFETs are further effective in reducing circuit layout area [10]. In addition, it offers the potential of providing a solution that extends beyond N2 technology [11]. Nevertheless, for highly scaled devices, even the smallest variation can significantly affect their characteristics [12]. Therefore, fluctuation cannot be ignored. Variations of this type are the main barrier to further scaling down of technology node. Device-to-device performance variations are primarily caused by process variations (PV) in sub-3-nm technology. Under PVs, it is a challenge to provide reliable IC design at advanced technology nodes. As compared to GAA NS metal oxide semiconductor field-effect transistors (MOSFETs), CFETs can reduce chip area by up to 50% [1], [13]. Thus, they are ideal for high-speed and low-power applications [14]. A further advantage of CFETs is their excellent performance characteristics, making them an attractive candidate for use in integrated circuits. In the fabrication process of high- κ -metal gate (HKMG) stacks, metal grains (MG) are challenging to grow during the nanometer scaling process [15]. The work function (WK) values of the amorphous MGs are random with respect to the small size of MGs [16]. The work-function variation, line edge roughness, gate edge roughness, and random dopant fluctuation (RDF) were demonstrated, and the comparative results between GAA NS MOSFET and CFET were also reported [12], [17].

Nanometer-level manufacturing processes are inevitably subject to intrinsic process fluctuations, such as the process variation effect (PVE) [17], [18], [19], [20], the work function fluctuation (WKF) [12], [16], [21], the RDF [15], [18], and interface trap fluctuations (ITF) [22], [23], [24]. Due to such process fluctuations, the DC characteristics have been subjected to serious variations resulting in severe effects on the designed circuit. As far as we know, the works explored with WKF and PVE are limited to planar MOSFETs, bulk FinFETs, GAA NW, and NS MOSFETs. It is insufficient to realize and benefit from the application of advanced technology nodes in which nanosheets occupy a large number of amorphous MGs and are sensitive to factors of PVE.

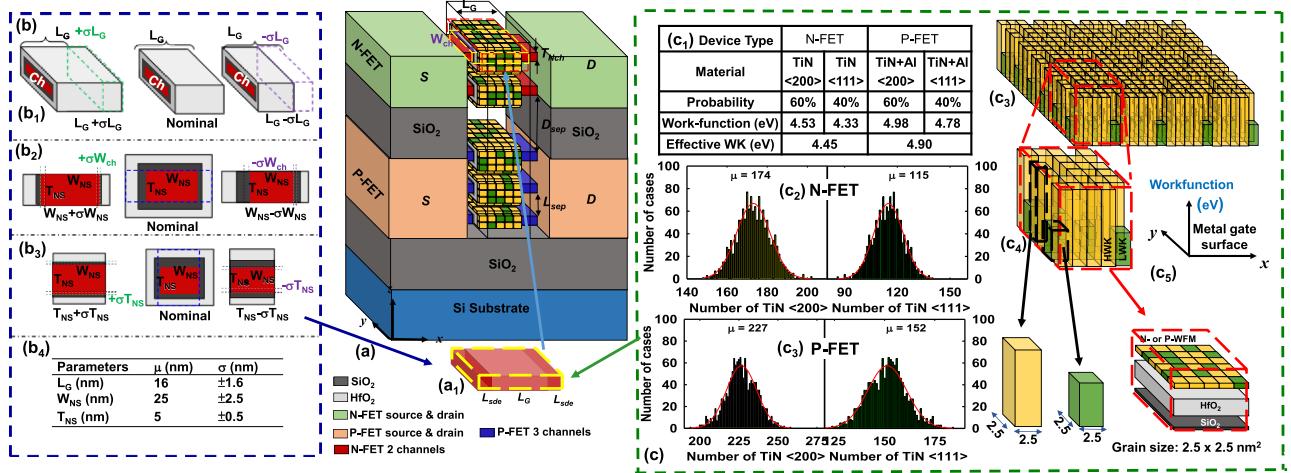


Fig. 1. (a) A schematic plot of the explored GAA Si NS CFET with totally random PVEs and amorphous-like MGs. (a₁) The schematic plot of PVE and WKF factors enter in to device. (b) The PVE including L_G , W_{NS} , T_{NS} is discussed. (b₁) L_G variation, (b₂) the W_{NS} variation, (b₃) the T_{NS} variation. (b₄) The value of the fluctuated geometrical parameters is in the range of 10% variation from its mean value. (c) The random MGs are generated in a large area; each amorphous MG is (2.5 nm^2). A plot of HKMG structure with the native oxides (SiO_2) around the silicon channel, where N-/P-work function of gate metal of each GAA channel is divided in to 144 amorphous MGs and the bottom channel of P-FET is with fin type whose grain is 90 metals. (c₁) For N-FET TiN is chosen in our simulation, where the orientation of TiN can be $<200>$ and $<111>$ with the probability of 60% and 40%, respectively. In addition, the N-FET work function of $\text{TiN} <200>$ and $<111>$ are 4.53 (high work function; HWK) and 4.33 eV (low work function; LWK), respectively, and the effective work function (EWK) is 4.45 eV. In constraint to N-FET, TiN doped with aluminum (Al) is chosen for P-FET. The P-FET work function $\text{TiN+Al} <200>$ HWK and $<111>$ LWK are 4.98 and 4.78 eV, respectively, and the EWK is 4.9 eV. The amorphous MGs are generated by using Gaussian distribution in a large plane; then, the distribution of each case will be assigned. (c₂)-(c₃) The Gaussian distribution of metal grains for both N-/P-FETs. The mean metal grain for N-/P-FET of HWK and LWK are 174, 115, 227, and 152, respectively.

It has been shown that the PVE and WKF mentioned above are related to the DC characteristics of current FinFET and GAA FETs, including threshold voltage (V_{th}), off-state current (I_{off}), subthreshold slope (SS), drain-induced barrier lowering (DIBL), and maximum transconductance ($g_{m,max}$). For identifying the comprehensive impacts of PVE and WKF on nanoscale devices, computer-generated modeling is the most feasible study than experimental investigation [25]. As far as the authors know, there is limited literature about the process variation of CFETs [12], [17], [19], [20]. However, as the semiconductor devices scaled to nanometer scale, the device physics becomes more complicated. Furthermore, a large number of sample devices are needed for analysis as fluctuations and variation sources are increases [26]. This requirement makes conventional device simulation tools less feasible because of their high computational cost [27]. This motivated researchers to explore other possible solutions which not only can improvise the computational time but also match the accuracy of the physics-based simulation tools. Some recent works have demonstrated that for semiconductor devices the machine learning (ML)-based artificial neural network (ANN) modeling method can provide high-accuracy models with a fast turnaround time [3], [28], [29]. For analyzing fluctuations in nanodevices, ANNs are proven superior in recent studies [30], [31]. Therefore, an ANN workflow that works efficiently to capture the variations in electrical characteristics induced by PVE and WKF will enable us to explore a novel paradigm in the device simulation domain.

In this paper, we for the first time estimate the DC/AC characteristics of 16-nm-gate HKMG CFETs in the presence of PVE and WKF. To determine the effect of fluctuations resulting from

the aforementioned random sources on the CFET characteristics, a 3-D statistical device simulation is performed intensively. To provide the best accuracy of simulation, the simulation has been experimentally validated. The major results show that both PVE and WKF affect the parameters of SCEs; nevertheless, the WKF with amorphous MG is found to bring less impact on device characteristic due to the screening effect of the inversion layer. The variability of I_{off} induced by PVE is large. Moreover, parameters of PVE as well as low and high work function values that have a predominant effect on CEFT transfer characteristics are also considered as input features to an ML-based ANN model.

The rest of the paper is organized as follows. Section II presents the structure of GAA Si NS CFETs with simulation settings, physical and electrical parameters of the nominal device, and random generation of PVE and WKF. In Section III, we demonstrate the results and discussions of DC and AC simulations, along with ANN model results. Finally, Section IV concludes the work of this article.

II. 3-D STATISTICAL DEVICE SIMULATION OF PVE AND WKF

The explored GAA Si NS CFET along with conventional CMOS devices are designed based on the projection of IRDS 2021 for high performance specification [25]. A 3-D schematic view of GAA Si NS CFET is shown in Fig. 1(a), where the bottom P-FET and top N-FET, the P-FET has two GAA and one fin-type channels, the N-FET has two GAA channels, in order to match the I_{on} of both devices. Fig. 2(a)–(b) are the plots of I_{off} versus I_{on} with respect to various factors of PVE; the

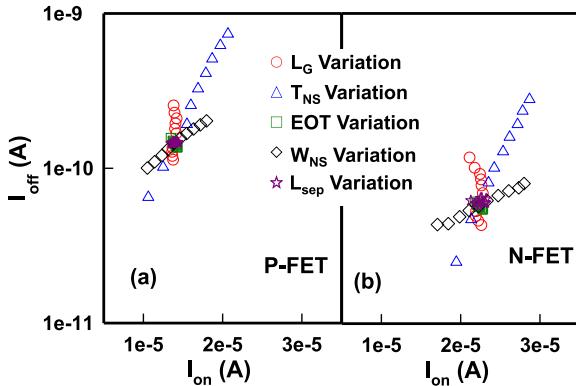


Fig. 2. Scatter plots of the off-current versus on-current for both N- and P-FETs of CFETs in relation to various PVE fluctuation factors. Among all factors, the characteristics of CFET are with the most severe fluctuations with respect to the nanosheet thickness and width of the nanosheet.

TABLE I
EXPLORED GAA Si NS CFET PHYSICAL PARAMETERS OF CALIBRATED DEVICE AND ACHIEVED CHARACTERISTICS AND SHORT CHANNEL EFFECTS OF NOMINAL DEVICES

Parameters	Value	
Channel doping (cm^{-3})	6×10^{17}	
Source and drain (S and D) doping (cm^{-3})	1×10^{20}	
S and D extension (S_{ext} and D_{ext}) doping (cm^{-3})	5×10^{18}	
S_{ext} and D_{ext} length (nm)	5	
Gate length (L_G) (nm)	16	
Inter-channel separation (L_{sep}) (nm)	10	
Inter-device separation (D_{sep}) (nm)	20	
Width of the nanosheet (W_{NS}) (nm)	16	
Nanosheet thickness (T_{NS}) (nm)	5	
Effective oxide thickness (EOT) (nm)	0.66	
Achieved Characteristics of Fresh Device		
Threshold voltage (V_{th}) (mV)	N-FET	265
	P-FET	-266
Off-state current (I_{off}) (A)	N-FET	3.5×10^{-11}
	P-FET	-4.1×10^{-11}
On-state current (I_{on}) (A)	N-FET	3.3×10^{-4}
	P-FET	-2×10^{-4}
Subthreshold slope (SS) (mV/dec)	N-FET	62
	P-FET	72
Drain-induced barrier lowering (DIBL) (mV/V)	N-FET	30
	P-FET	49

device characteristics are strongly affected by the NS thickness (T_{NS}), NS width (W_{NS}) and gate length (L_G), leading to sizeable dispersion than other factors. The T_{NS} has been observed to have a greater impact on I_{off} , and the W_{NS} to have a greater impact on I_{on} . Therefore, we further consider these three factors in order to determine PVE. We calibrated our device simulation with Intel measurement data in order to provide the highest level of accuracy [1]. In our earlier work, we have demonstrated the simulation calibration [3]. Table I lists the adopted device

parameters after a careful calibration with measured CFET characteristics and achieved characteristics of nominal device (i.e., without considering any PVE and WKF). The calibration parameters of mobility models are used in this simulation. In particular, the 3-D device simulation is achieved by solving the quantum-mechanically corrected drift-diffusion model in well-known Sentaurus TCAD tool [5], [32], [33]. Similarly, the device simulation of PVE and WKF is carried out using similar calibration methodologies and models. A total 1300 samples are randomly generated and simulated to examine the impact of PVE and WKF on the explored device. Fig. 1(a₁) shows schematic plot of random sources of PVE and WKF entering the device. Both N- and P-FETs of the GAA Si NS CFET are simulated simultaneously. This large-scale statistical device simulation is intensively performed to examine the impact of PVE and WKF on device characteristics.

A. Random Generation of PVE and WKF

For the CFET PVE, we randomly vary three major factors, which are T_{NS} , W_{NS} and L_G as part of the PVE simulation. A detailed description of parameter settings of PVE is provided in Fig. 1(b). It is not shown here, but the generation and distribution of random process variation parameters also follow a Gaussian distribution. As shown in Fig. 1(b₄) the list of these three factors of PVE, as well as their mean (μ) and standard deviation (σ), where the 10% variation considered for each factor from their μ value. Additionally, the adopted PVE and WKF methods have been demonstrated [15], [18] and 1300 samples have been generated randomly. To study the impact of WKF on CFETs, the amorphous-like TiN metal is composed with $2.5 \times 2.5 \text{ nm}^2$ MGs, as shown in Fig. 1(c). As listed in Fig. 1(c₁), the probability of $\text{TiN}_{<200>}$ and $\text{TiN}_{<111>}$ orientations with high work function (HWK) and low work function (LWK), respectively, for both N-/P-FETs are according to gate material properties; they are 60% and 40% respectively. The generation and of HWK and LWK of MGs follows the Gaussian distribution, where the average number of HWK and LWK are 174 and 115 for N-FET, and 227, 152 for P-FET, as shown in Fig. 1(b₂)–(b₃). In Fig. 1(c₂)–(c₃), the red curves show the Gaussian distribution of LWK and HWK for N-FETs and P-FETs, respectively.

III. RESULTS AND DISCUSSIONS

In this section, we first examine the characteristic fluctuation induced by PVE and WKF for both N-/P-FETs by assessing their transfer characteristics; then, we estimate the fluctuated magnitudes of V_{th} , I_{off} , I_{on} , SS, DIBL and $g_{\text{m,max}}$. As part of the AC characteristics, the gate capacitance (C_G) is considered as a result of the effects of PVE and WKF. The SCEs parameter fluctuations are evaluated using the ratio of standard deviation to mean value ($\sigma/\mu \times 100\%$) of each figure of merit (FoM). We do further model the transfer characteristics of the explored devices via the ML approach as well.

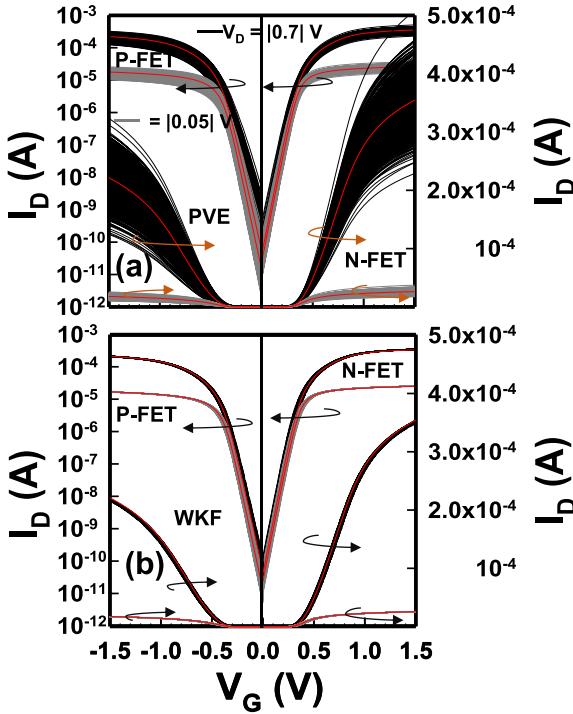


Fig. 3. (a)–(b) In both linear and log scales N-/P-FETs, the simulated PVE and WKF-induced I_D - V_G characteristic fluctuation in the linear and saturation regions.

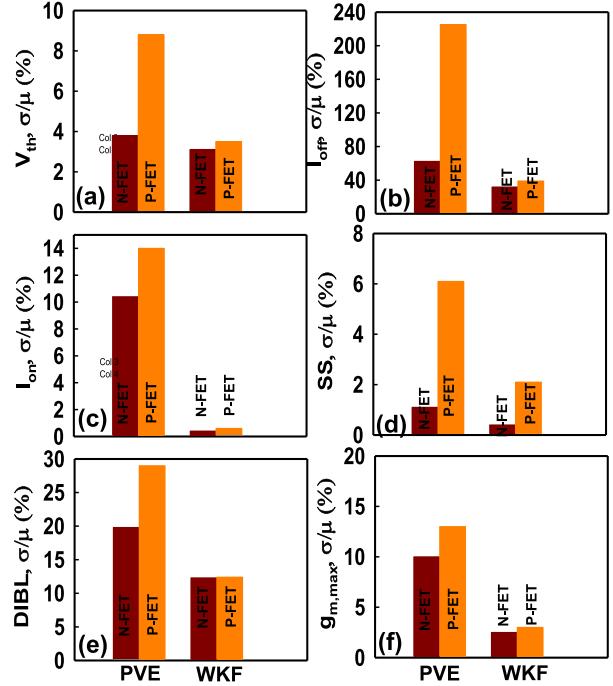


Fig. 4. (a)–(f) The statistical calculation ($\sigma/\mu \%$) of both N-/P-FETs for PVE and WKF-induced short channel effects in CFET devices. (a) V_{th} , (b) I_{off} , (c) I_{on} , (d) SS, (e) DIBL, and (f) $g_{m,max}$ variations.

A. DC Characteristic Fluctuation

Nominal devices are those that have not been impacted by PVE and WKF. Here, for all figures, the red curves indicate the nominal devices for both N-/P-FETs. For the explored GAA Si NS CFET in the linear and saturation regions, Fig. 3(a)–(b) show the simulated I_D - V_G characteristics induced by PVE and WKF, respectively. The fluctuation induced by PVE is significant, as compared to WKF. The factors of PVE appear to be more sensitive to device characteristics. The fluctuation at the off-state induced by PVE is relatively large, as shown in Fig. 3(a). In the studied GAA devices, the carrier's transport is governed by large GAA that controls the carrier's flow. Due to the fact that the plenty of carrier's transport is controlled by the GAA along the channel direction, it is possible to control the scattering of carrier by adjusting the effects of T_{NS} , W_{NS} , and L_G on the I_{off} . It is evident from the results of this study that the amorphous type MGs reduced the characteristic fluctuation. While the crystalline metal exhibits a large number of grain size, the adoption of amorphous metal has effectively reduced the grain size to less than 3 nm. Consequently, an increase in the quantity of amorphous MGs is observed. This rise in the number of amorphous MGs contributes to a reduction in characteristic fluctuation. Furthermore, the fluctuations of V_{th} , I_{off} , I_{on} , SS, DIBL and $g_{m,max}$ are discussed by using the statistical calculation ($\sigma/\mu \%$), as shown in Fig. 4(a)–(f). The P-FET has severe impact of variation compared to N-FET, due to the bottom fin type channel leakage. The PVE-induced variation is large for P-FETs, in particular, the I_{off} has more than 200% variation, as shown in

Fig. 4(b). The variability of the parameter of SCEs affected by WKF is insignificant for both N-/P-FETs. Especially, the WKF in I_{on} has almost zero variation.

B. AC Characteristic Fluctuation

One of the key AC characteristics is the device capacitance, in which the total gate capacitance (C_G) is directly extracted from the AC curves of N-/P-FETs. The C_G in CFETs is an important FoM that determines the device's switching speed, power consumption, and overall performance of the device. Additionally, it is influenced by the gate dielectric material, in particular, for HKMG devices. The PVE- and WKF-induced C_G - V_G characteristic fluctuations are shown in Fig. 5(a)–(b), respectively. It has been observed that the C_G fluctuations induced by PVE are significantly greater than those caused by WKF. There are almost negligible fluctuations of the estimated C_G induced by WKF in the saturation region. At zero gate bias, the accumulation layer screens the impact of WKF. The C_G fluctuations are minimal. During the on-state region the C_G achieves its upper limit due to the saturation of the maximal depletion region. As a result, the corresponding fluctuations in C_G are small. For the PVE-induced C_G fluctuation variations ($\sigma/\mu \%$) comparisons in the off- and on-state regions for N-/P-FETs are shown in Fig. 6(a)–(b). The comparison between PVE and WKF shows that PVE has significant variations on C_G for both N-/P-FETs. In addition, in the on-state region, for both the devices, the large C_G fluctuation has been observed; the

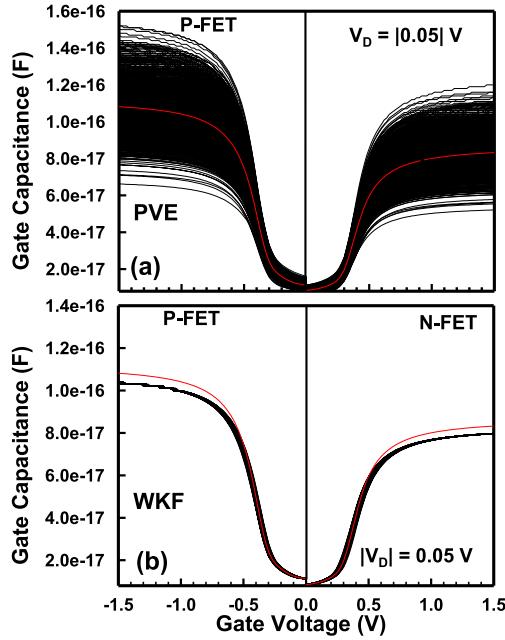


Fig. 5. Simulated C_G - V_G characteristic fluctuation induced by PVE and WKF of both N-FETs and P-FETs, where the red curve indicated the nominal device. (a) The fluctuations induced by PVE, (b) the fluctuation induced by WKF.

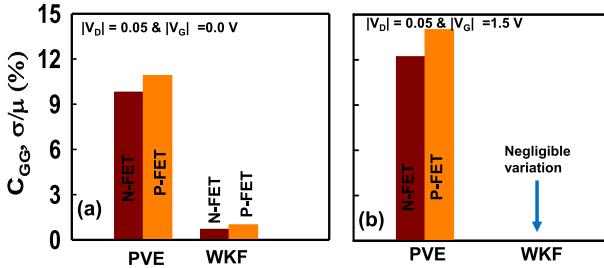


Fig. 6. Statistical calculation ($\sigma/\mu \%$) of PVE and WKF-induced gate capacitance of both N-FET and P-FET in CFET devices in the off-state and in the saturation region.

estimated values of ($\sigma/\mu \%$) are 12.8% and 14% for N-/P-FETs under the influence of PVE.

C. ANN Modeling of DC Transfer Characteristics

A highly accurate ANN model majorly depends on the number of available data that is used by the model to learn the pattern and to predict the output. To apply the ANN model, the database, of 1300 samples of N-FET and P-FET devices (for linear and saturation regions) for PVE and WKF each are generated for training and validation of the model. Fig. 7 represents the structure of the ANN to model the fluctuated characteristics of the transistor. In this work, to model PVE, the device parameters, that contribute the most to the variations, i.e., L_G , W_{NS} , and T_{NS} are used as inputs to estimate the variation. Similarly, for WKF the HWK and LWK patterns of WKs are used as inputs to the model and their variations on I_D - V_G characteristics are estimated. The inputs are preprocessed before

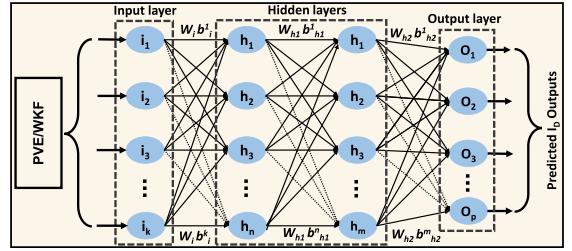


Fig. 7. Illustration of ANN model architecture for GAA Si NS CFET simulated dataset. The input layer is fed with PVE and WKF. Two hidden layers process the simulated data passed through the input layer. Lastly, one output layer accepts the data manipulated using biases and weights of hidden layers and then delivered it in the form of predicted current values (I_D).

TABLE II
COMPARISON OF THE R^2 -SCORE AND RMSE VALUES FOR I_D - V_G CHARACTERISTICS OBTAINED THROUGH TRAINING AND TESTING OF ANN MODEL FOR BOTH PVE AND WKF OF N-FET AND P-FET

Source	Device	$ V_D $ (V)	R^2 -score (Train)	R^2 -score (Test)	rmse (Train)	rmse (Test)
PVE	N-FET	0.05	0.9960	0.9913	6.47e-07	6.84e-07
	P-FET	0.05	0.9924	0.9878	2.24e-07	3.02e-07
	N-FET	0.7	0.9748	0.9465	7.66e-06	8.27e-06
	P-FET	0.7	0.9840	0.9796	2.13e-06	2.18e-06
WKF	N-FET	0.05	0.9970	0.9924	1.45e-07	2.46e-07
	P-FET	0.05	0.9909	0.9791	2.51e-07	4.96e-07
	N-FET	0.7	0.9886	0.9758	1.94e-06	2.87e-06
	P-FET	0.7	0.9835	0.9642	1.13e-06	1.85e-06

feeding into the model. The ANN model used for training has two hidden layers, hyperbolic tangent (\tanh) activation function, and adam optimizer using keras and tensorflow in backend with a learning rate of 0.001. All the model hyper-parameters are tuned and optimized iteratively during the training process.

Fig. 8 illustrates the simulated vs. ANN predicted electrical characteristics for N-FET and P-FET for training and validation results for PVE [Fig. 8(a)-(b)] and WKF [Fig. 8(c)-(d)] in linear and logarithmic scales. It can be noticed that the variation caused by WKF is comparatively much lesser than PVE. The ANN model, however, has the ability to accurately estimate the characteristics in both cases. ANN model performance is evaluated using R^2 -score and error is estimated using root mean square error (rmse). The R^2 -score is defined as

$$R^2\text{-Score} = 1 - \frac{\text{Residual sum of square}}{\text{A total sum of square}} = 1 - \frac{\sum_i^n (\text{Predicted}_i - \text{Actual}_i)^2}{\sum_i^n (\text{Average}_i - \text{Actual}_i)^2} \quad (1)$$

and the rmse is defined as

$$\text{rmse} = \sqrt{\frac{\sum_i^n (\text{Predicted}_i - \text{Actual}_i)^2}{N}} \quad (2)$$

The values for these quantitative measurement parameters are summarized in Table II which gives more intuitive results. On average, the R^2 -score of the ANN model is more than 98%

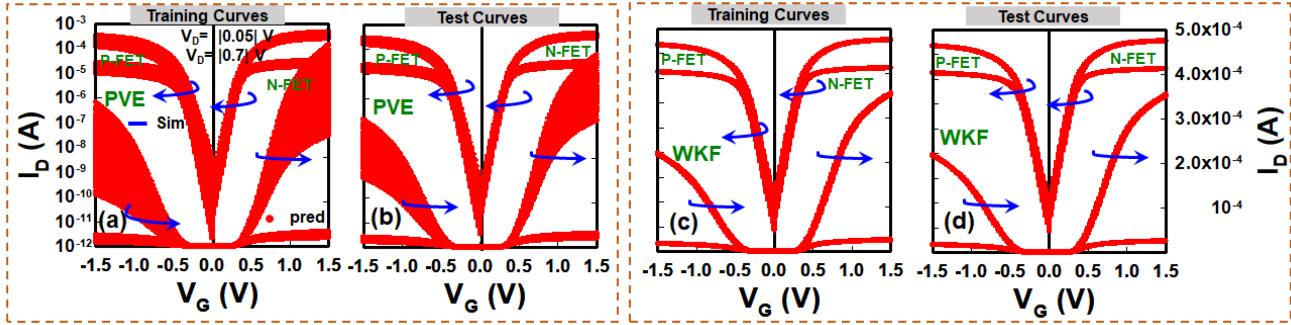


Fig. 8. Illustration of I_D - V_G curves obtained through the device simulation of GAA Si NS CFET (blue line) and from the predictive ANN model (red line). Each figure shows the linear as well as logarithmic I_D - V_G curves (a) represents the training of the ANN model based on the GAA Si NS CFET induced by PVE for N-and P-FETs. Similarly, (b) shows the testing of the ANN model for N-and P-FETs. (c) and (d) represent the training and testing of the ANN model based on GAA Si NS CFET induced by WKF, respectively. These I_D - V_G curves for both PVE and WKF for N-and P-FET depict the well-trained ANN model.

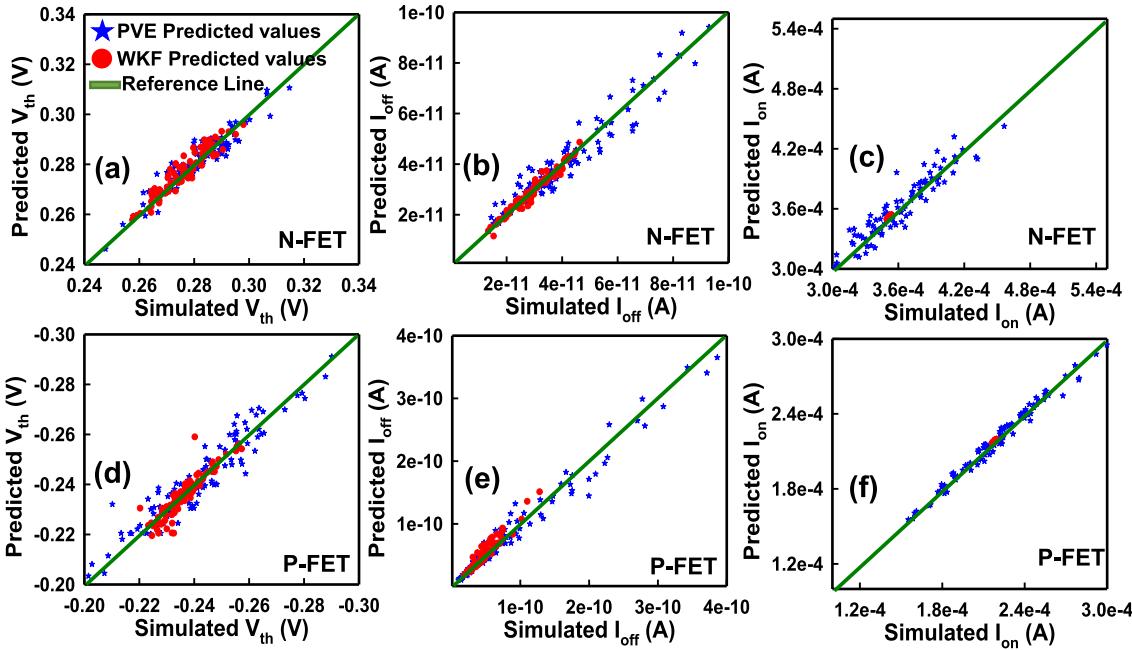


Fig. 9. Plot illustrates the linear relationship between the predicted and simulated values for N-FET and P-FET. (a) and (d) show the predicted and simulated V_{th} values for N-/P-FETs, respectively. For N-FET and P-FET, (b) and (e) represent the predicted and simulated I_{off} values, respectively, and (c) and (f) represent the predicted and simulated I_{on} values, respectively. A good agreement is observed between all of the electrical characteristics extracted from PVE- and WKF-induced simulated I_D - V_G curves as well as the predicted I_D - V_G curves.

for training and 97% for testing. Similarly, the small values of rmse ensure the excellent prediction performance of the ANN model. ANN models show an improved performance based on the smaller errors in the table. The test plots demonstrate that the trained model accurately predicted I_D - V_G characteristics. For test curves, the ANN model is also used to estimate the variability in V_{th} , I_{off} , and I_{on} caused by PVE and WKF. Fig. 9(a)–(f) illustrate the comparison between the predicted and the simulated I_D - V_G curves for N-FETs and P-FETs, respectively. According to the results, all FOMs are constrained toward the reference line (optimum line). According to the results, the ANN model is capable of making accurate predictions for a variety of FOMs. Furthermore, the computational cost for generating simulated data (1300 hours) is very high as compared to the ANN modeling (approximately 48 mins for training). Therefore, the

analysis of fluctuations using the ANN model can significantly improve the calculation efficiency with high accuracy compared to simulation results.

V. CONCLUSION

This work reported the impact of PVE and WKF on DC/AC characteristic fluctuations in GAA Si NS CFETs. In both PVE and WKF variations, P-FETs are affected more severely than N-FETs; however, variations of PVE are more pronounced than that of WKF. For the impact of PVE, T_{NS} , W_{NS} , and L_G cause more variations on DC characteristics. We observed that PVE shows large variations for both N- and P-FETs, whereas the impact of WKF on C_G is marginal, and it has almost zero in the saturation region. Furthermore, an ML-based ANN modeling

methodology was also developed to predict PVE and WKF variations. Samples of 1300 devices were simulated for every device and variations to train and test the ANN model. An accuracy of more than 98% was achieved in terms of R²-score. The ANN results indicates that the computational time was significantly reduced while maintaining high model accuracy. The well-trained ANN model can be incorporated into circuit simulation to assess the circuit performance of CFETs, not shown here. We are currently examining the effects of coupling capacitance on CFETs for high-speed circuits.

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