ECEN 5613 | **Embedded System Design** | **Fall 2021**

Lab #2 Signoff Sheet

You will need to obtain the signature of your instructor or TA on the following items in order to receive credit for your lab assignment. Signatures are due by **Friday, September 24, 2021 (Part 1 Elements) and Friday, October 1, 2021 (Part 2 Elements)**.

Print your name below, sign the honor code pledge, and then demonstrate your working hardware & firmware in order to obtain the necessary signatures.

Student Name: Dhiraj Bennadi

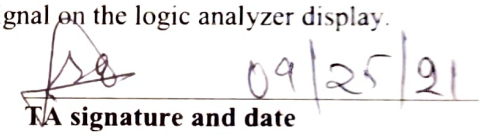
Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. **I have clearly acknowledged work that is not my own.**"

Student Signature: 

Signoff Checklist

Part 1 Required Elements

- [x] Schematic of acceptable quality, correct memory map, SPLD .PLD file
- [x] Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board
- [x] NVRAM (as EPROM substitute), decode logic, and LED functional
- [x] Understands device programmer.
- [x] Demonstrated ability to use logic analyzer to capture bus cycles and view fetches from NVRAM. Shows detailed knowledge of both state and timing modes. Captures latched address lines A[15:0], data lines D[7:0], ALE, /PSEN, and NVRAM chip select signal on the logic analyzer display.
- [x] Shows and discusses logic analyzer screen captures:
- [x] Assembly program and timer ISR functional:



09/25/21

TA signature and date

Part 2 Required and Supplemental Elements — did not do supplemental portion

- [x] AT89C51RC2, RS-232, and FLIP functional
- [x] 74LS374 debug port functional
- [x] Understands timing analysis, setup/hold/propagation
- [x] MSP432 code build process, LED program, version control

10/1/21

Instructor/TA Comments: ☐ ☐ ☐

TA signature and date

FOR INSTRUCTOR USE ONLY **Part 1 Elements**	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☑	☐	☐
Hardware physical implementation	☐	☐	☑	☐	☐
Part 1 Required Elements functionality	☐	☐	☑	☐	☐
Sign-off done without excessive retries		☐	☑		
Student understanding and skills	☐	☐	☑	☐	☐
Overall Demo Quality (Part 1 Elements)	☐	☐	☐ ✓	☐	☐

FOR INSTRUCTOR USE ONLY **Part 2 Elements**	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☐ ✓	☐	☐
Hardware physical implementation	☐	☐	☐ ✓	☐	☐
Part 2 Required Elements functionality	☐	☐	☑	☐	☐
Supplemental Elements functionality	☑	☐	☐	☐	☐
Sign-off done without excessive retries		☐	☐		
Student understanding and skills	☐	☐	☐ ✓	☐	☐
Overall Demo Quality (Part 2 Elements)	☐	☐	☐ ✓	☐	☐

NOTE: This signoff sheet should be the top/first sheet of your submission.

(+) Neat schematic, Headers in .ASM present
(-) Add comments to assembly code
~~/ Verify opcodes in state & timing modes~~
(-) T_{LPL} to be done. Will be added in report
(+) Good Understanding of Memory map, LED design

Part 2

→ Try and use clock dividers/prescalars to eliminate extra overhead in ISR for timer

→ Pull debouncing out of Port ISR to reduce overhead

→ Debug latch functional
→ Timing calculations verified
— Writes not restricted to 0000-7FFF H
/ To add screenshots of ISR debug values

Venkat 10/2/17