Electrical, Computer & Energy Engineering
UNIVERSITY OF COLORADO BOULDER

Embedded System Design Lab 1 Report

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Objective:

- Learn how to use an assembler and simulator. Start using the 8051 and ARM processors.
- Learn how to use the WinCUPL/WinSim design suite for the Atmel AT16V8C SPLD.
- Plan the layout of your development board and obtain your parts kit.
- Start learning schematic capture and gain skills in soldering. Build your basic hardware

Summary of Tasks:

1. Developed Assembly Language Program for Multiplication and WinCUPL code for Atmel AT16V8C SPLD chip to implement logic to drive the address lines of 80C51 microcontroller and verified on the Logic on WinSim and Logic Port.
2. Developed schematics for Reset Circuit, Oscillator circuit, Power On circuit, 80C51 Microcontroller, 74LS373 Address Latch, Atmel AT16V8C SPLD Chip.
3. Assembled the components on the PCB through soldering and wire wrapping techniques. Tested the hardware for various measurements to verify the working of the code and the connections of the components

Critical Readings

1. Voltage Readings

Sl.No	PCB Area	Value
1	Input of the Power Jack	9.16V
2	80C51 VCC-GND	4.97
3	SPLD VCC-GND	4.98V
4	74373 Address Latch	
5	Voltage Regulator Input	7.58V
6	Voltage Regulator Output	4.98V
7	Peak-Peak Voltage at 80C51 Top Side of PCB	279 – 330 mV
8	Peak-Peak Voltage at 80C51 Bottom Side of PCB	140 – 220 mV

2. Frequency Readings

Sl. No	Checkpoint	Value
1	ALE Pin	1.843 MHz
2	X1 Pin	11.11 Mhz

3. Timing Readings

Sl.No	Checkpoint	Value
1	Reset Circuit with reference to ALE Pin	120 ms

Visuals as measured on Oscilloscope

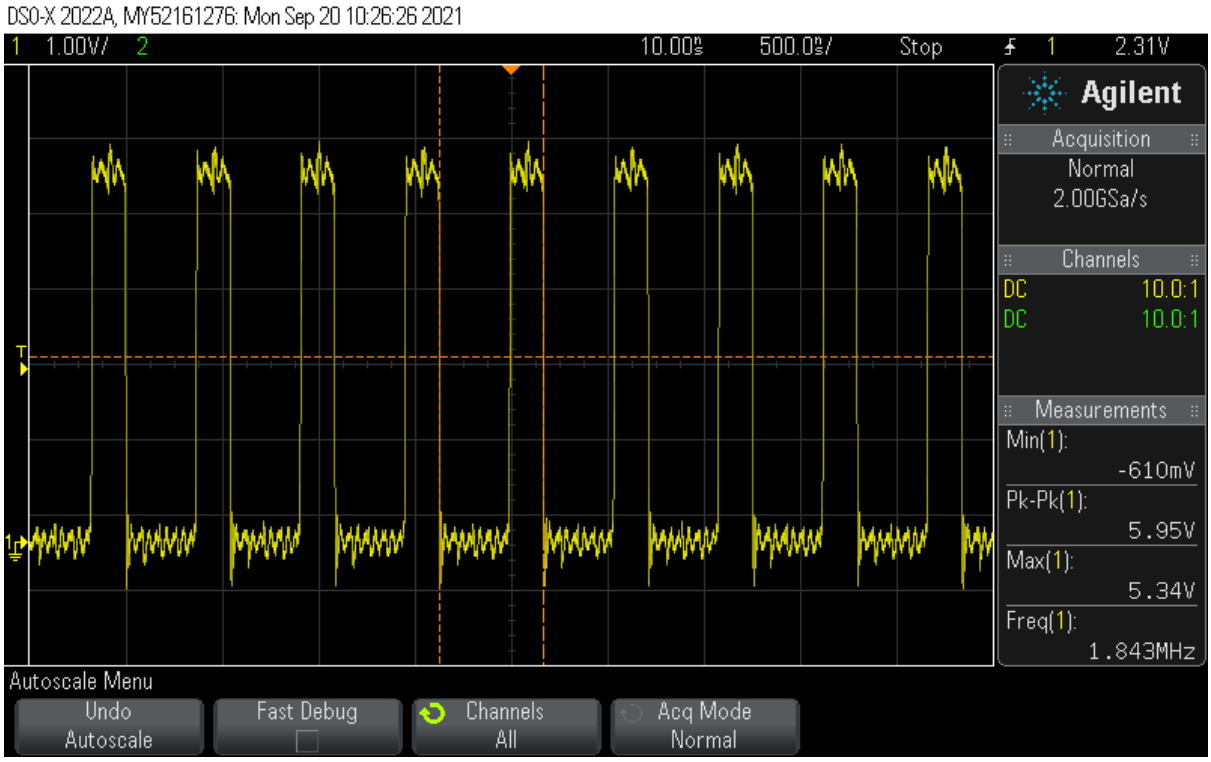

Figure 1 ALE Pin Reading

The Frequency of the ALE Pin is 1/6th of the Clock Frequency.

ALE Frequency = 1/6 * 11.11 Mhz

ALE Frequency = 1.851 Mhz

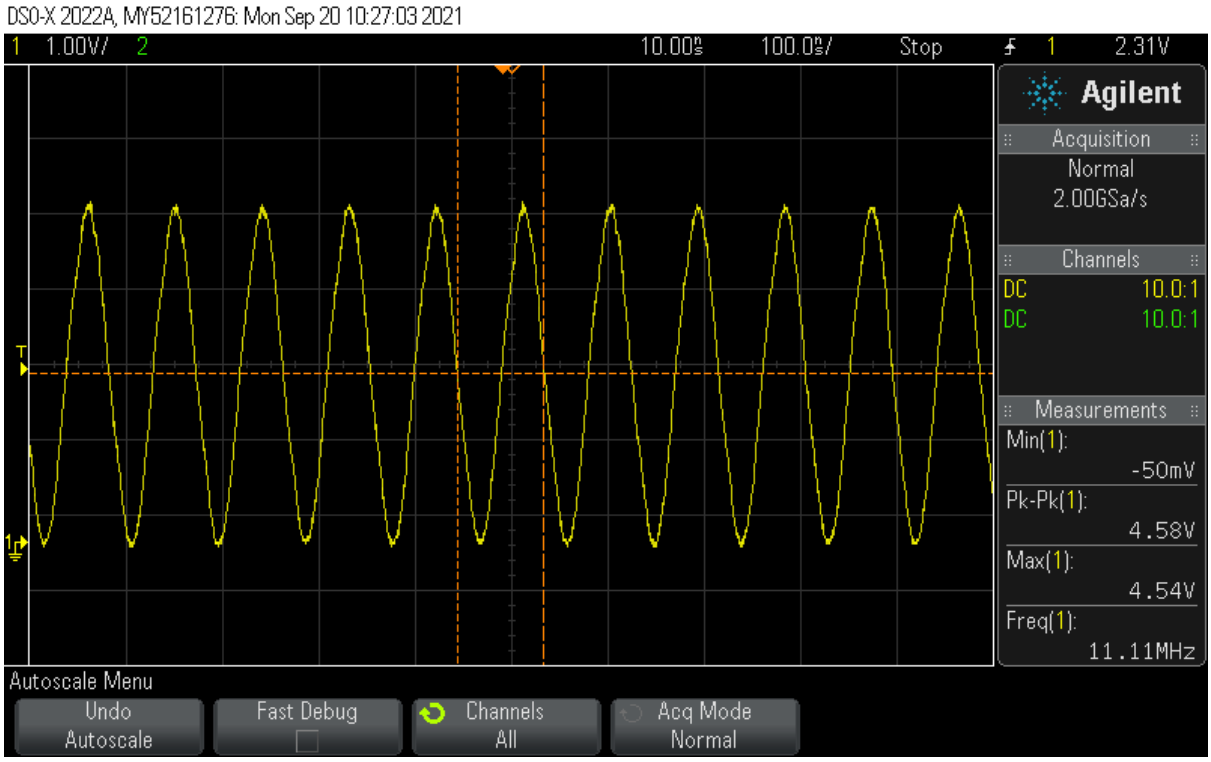

Figure 2 X2 Frequency

The measured value is across the X2 pin of the microcontroller. The oscillator circuit generates a theoretical frequency of 11.0592Mhz. The measured frequency is 11.11Mhz as shown in the above image.

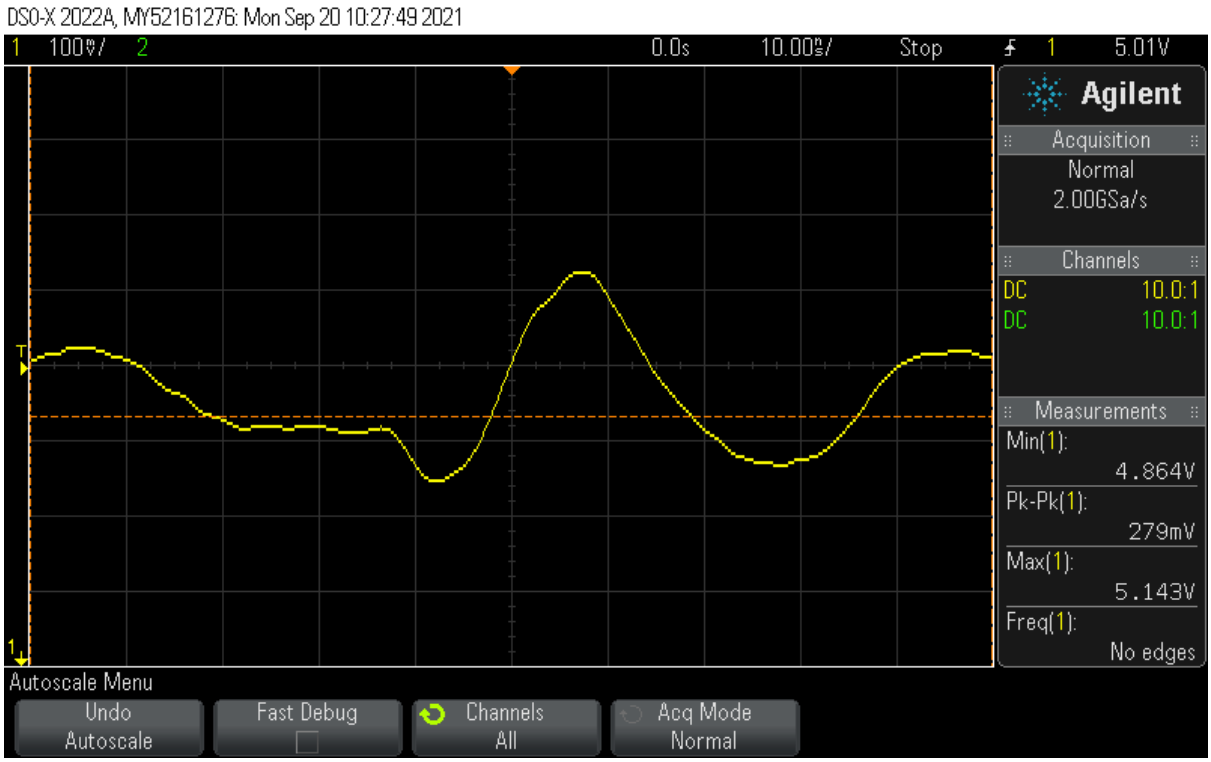

Figure 3 Peak-Peak Voltage at 80C51

The peak-peak Noise Voltage between Vcc and GND of the uC is 279 mV which is less than the 800 mV (Considered as a safe range for Noise)

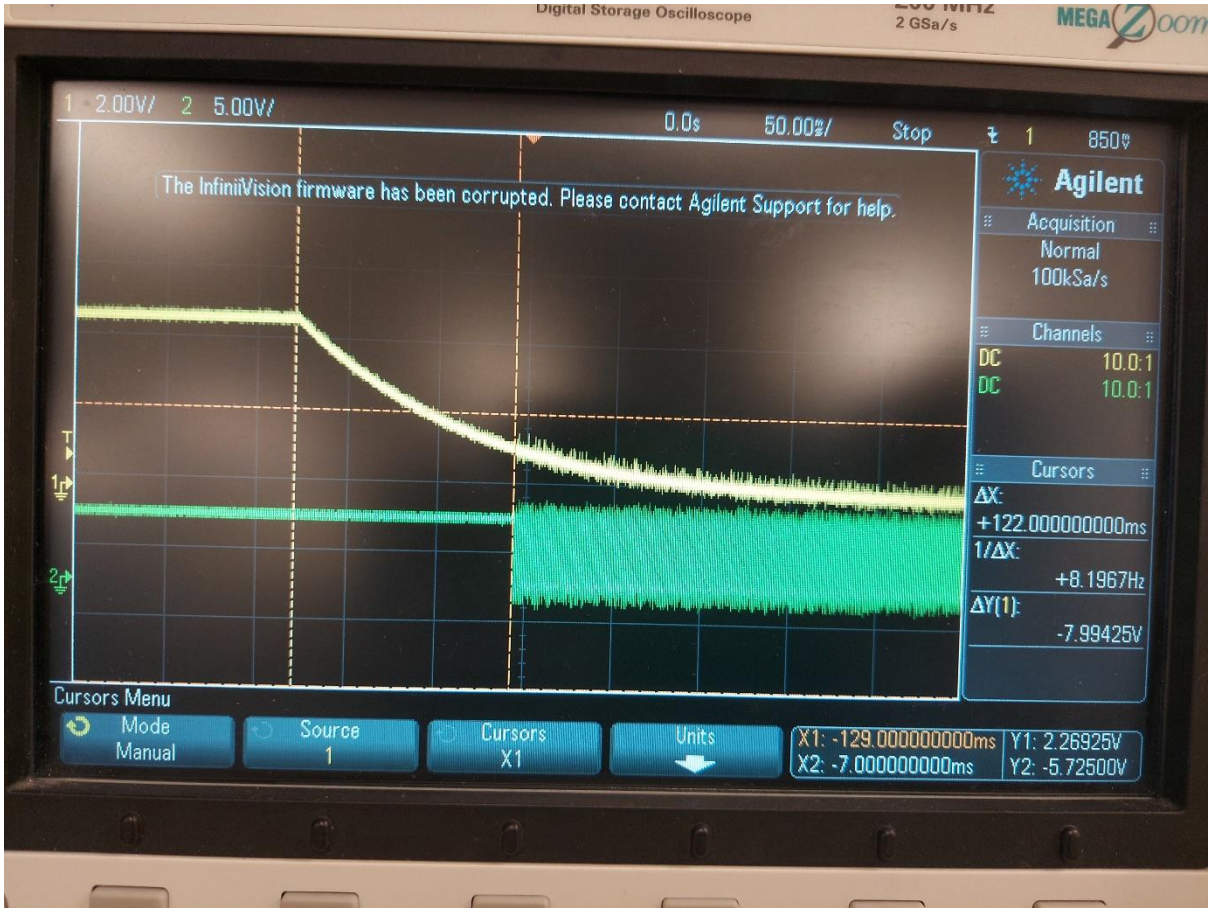

Figure 4 Duration of reset

The above image shows the readings across the Reset Circuitry and the ALE pin. The image shows the time period, the capacitor in the reset circuitry takes to discharge and the point at which uC boots up after the reset push button is released.

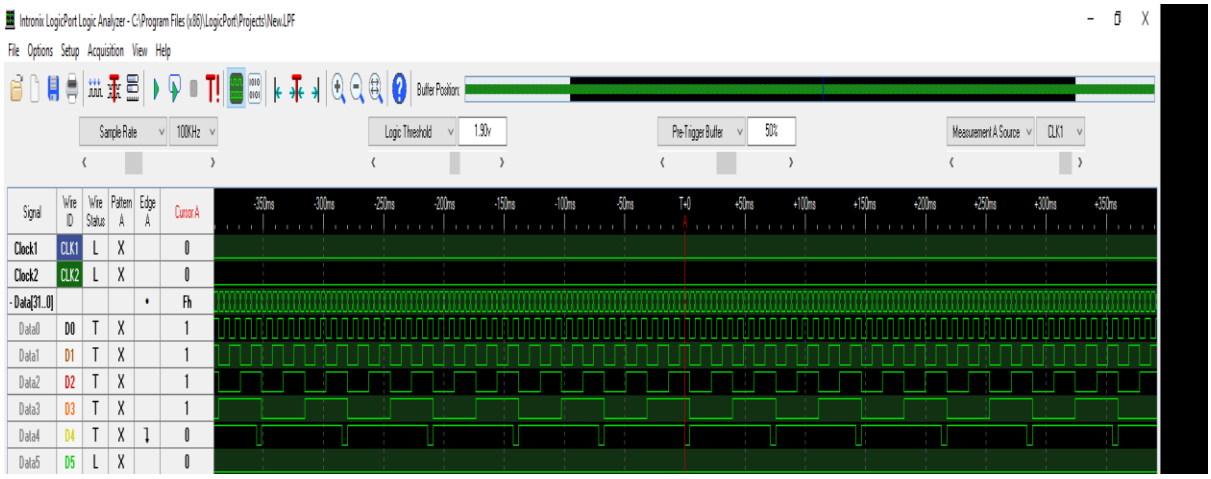

Figure 5 Logic Analyzer Output of CSPeripheral

The Lines D0, D1, D2, D3 correspond to Address Lines A12, A13, A14, A15 of the uC and Line D4 corresponds to CSPeripheral.
The logic implemented is CSPeripheral = !(A12 & A13 & A14 & A15)

The CSPeripheral has a duty cycle of 15/16 enabling the uC to address a memory of 4KB of external ROM or Data.

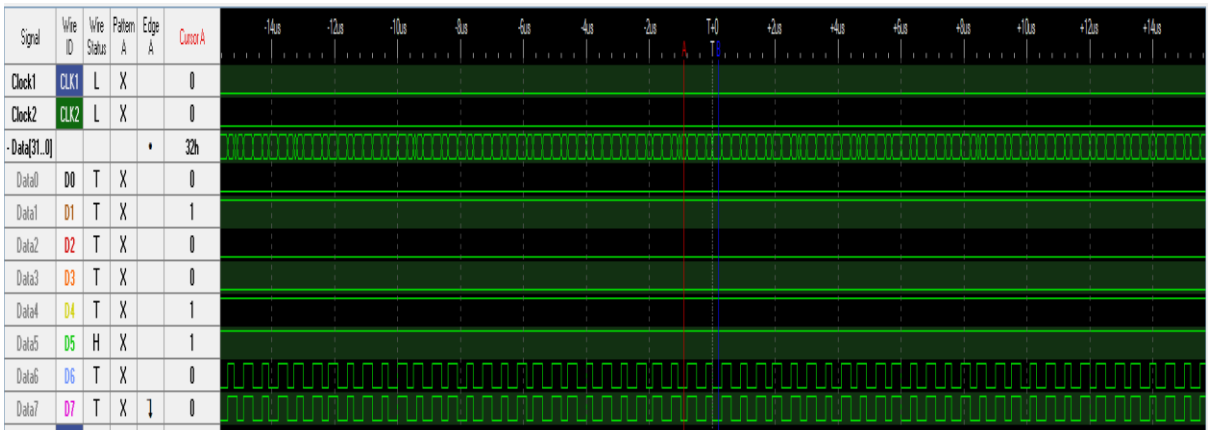

Figure 6 Logic Analyzer Output of Readn Pin

In Figure 6, the lines D5 and D6 correspond to RDn and PSENn, and line D7 corresponds to READn.

The logic implemented is READn = RDn & PSENn

This enables the uC to read data from the external memory only when the RDn and PSENn pins are active.

Key Learnings from TA Comments

1. Reduction of Assembly code size by using the MOV RAM_addr, Rn command
   This reduced the code size from 87 Bytes to 83 Bytes
2. Organized the Schematics by using Net Labels instead of Wires
3. Used Uniform Symbols into both the Schematics
4. Understood the variation of the Reset timing after the reset push button is released.