

# ECEN5730-PCB Board-2 Report

## Project Overview

### POR

1. Converting 5 V in to 3.3 V using LDO
2. Creating a clock signal of about 500 Hz and about 66% duty cycle
3. Driving four of the inputs of two hex inverters and use it to demonstrate good layout and bad layout
4. Adding a switch to selectively connect the 555 output to the various inputs of the good and bad layout hex inverters. When not connected, all the switching inputs to be tied HIGH so they do not switch.
5. Using red LEDs and about 50 ohm resistors as the load to three of the switching outputs of each hex inverter
6. Estimating the current expected to be drawn from the inverter for the LED and 50 ohm resistor load.
7. Connecting the output of the fourth switching inverter to a test point to act as a trigger for the scope
8. Setting up one output of each hex inverter as a quiet HIGH and one output as a quiet LOW
9. Engineering the layout on one side of the board with best design practices and the other side of the board with bad layout practices. In the bad layout, Decoupling capacitor to be moved away, remaining circuit would be identical to good layout.
10. There would be test points for:
  - a. The scope trigger output
  - b. The quiet high
  - c. The quiet low
  - d. The 555 output signal
  - e. The 3.3 V rail on the board
  - f. The 5 V rail on the board

## What it means to work:

### Power supply:

1. Check visually if LED for power is turned on
2. Measure the voltage of power rail on oscilloscope using 5V test point. Voltage should be around 5V.
3. Measure the voltage of power rail on oscilloscope using 3V3 test point. Voltage should be around 3.3V.

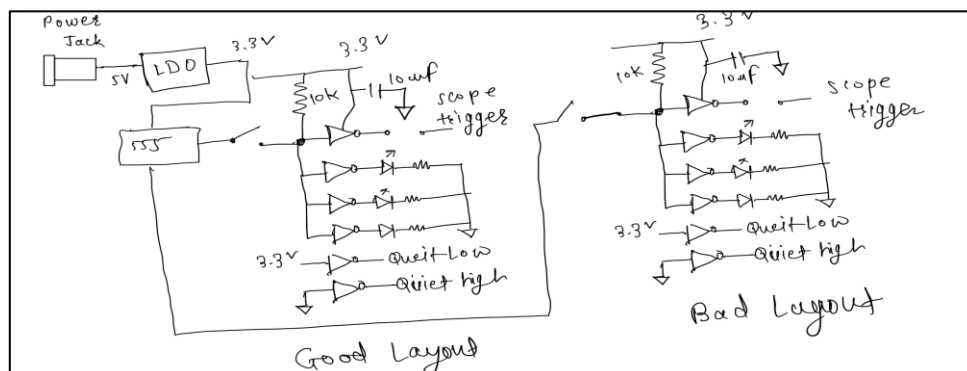
### 555 timer circuit:

1. Square wave should be visible on the oscilloscope when probed at 555 output test point.
2. Duty cycle of the square wave should be around 67%

### Hex Inverter:

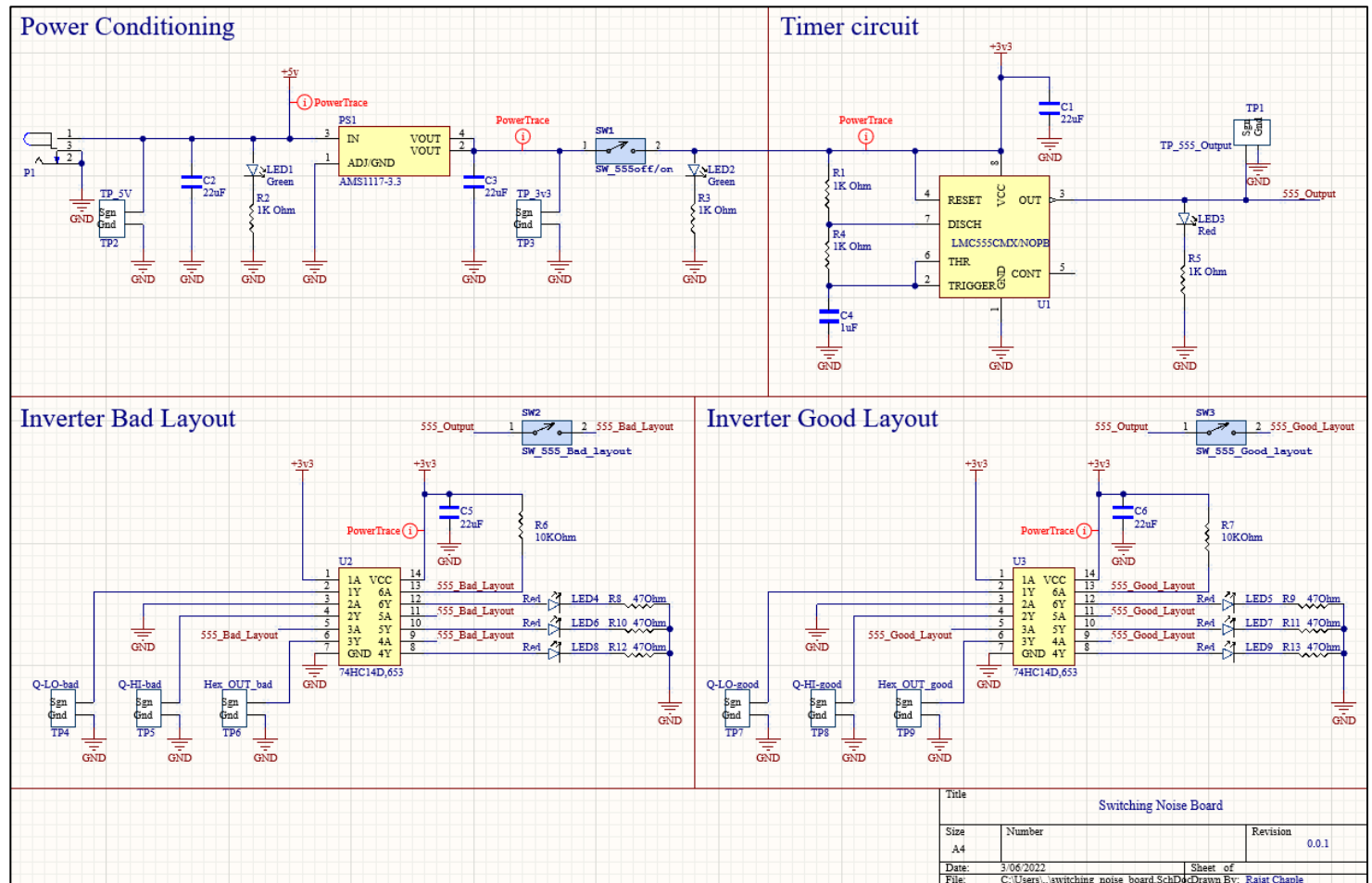
1. Inverted signal should be seen on one of the hex inverter outputs

## Sketch of the schematic:



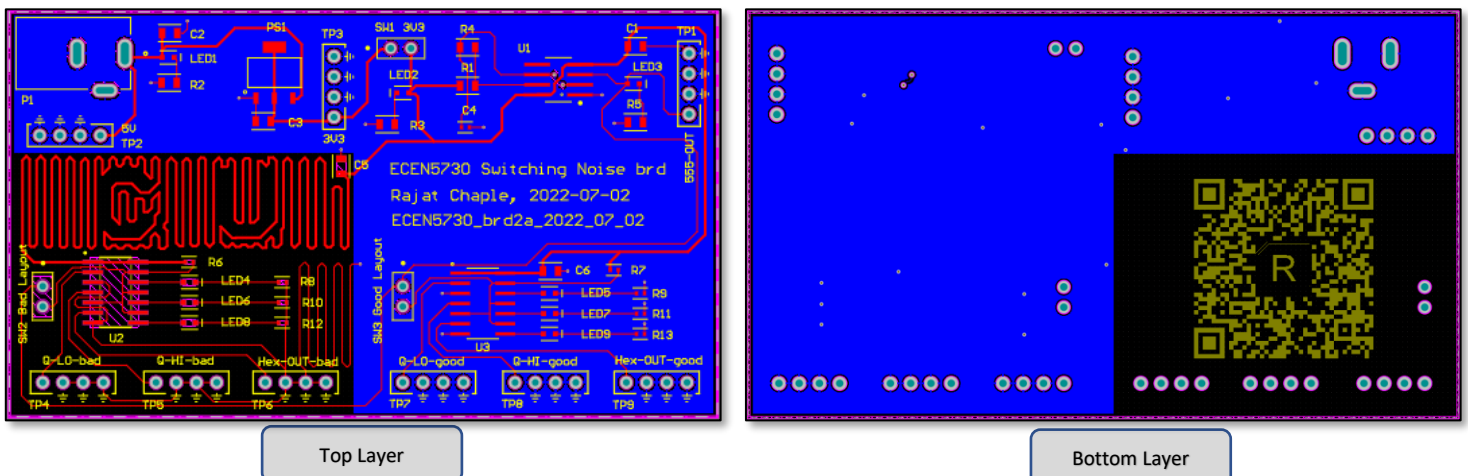
## Actual schematic capture from Altium designer

- Schematic was divided into functional sections: power conditioning, Timer circuit and Inverter Bad and Good Layouts.
- PowerTrace class was used to set 20 mils of power lines in layout
- Appropriate isolation switches, LEDs and test points were used at required locations.



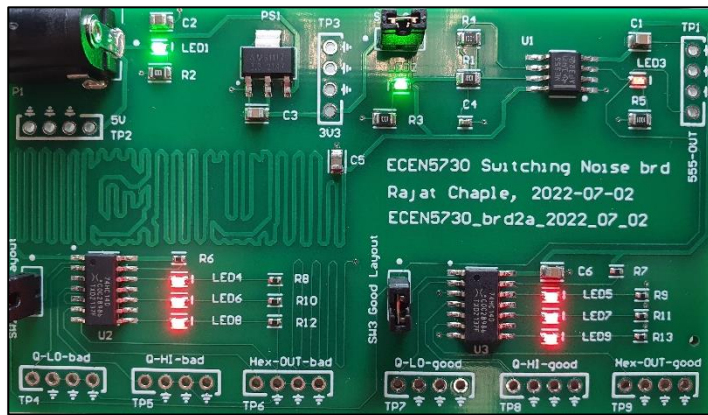
## Board layout from Altium designer

- Appropriate design rules were set before starting the layout. E.g. via diameter, Thermal relief.
- Name, board ID was used as board identification

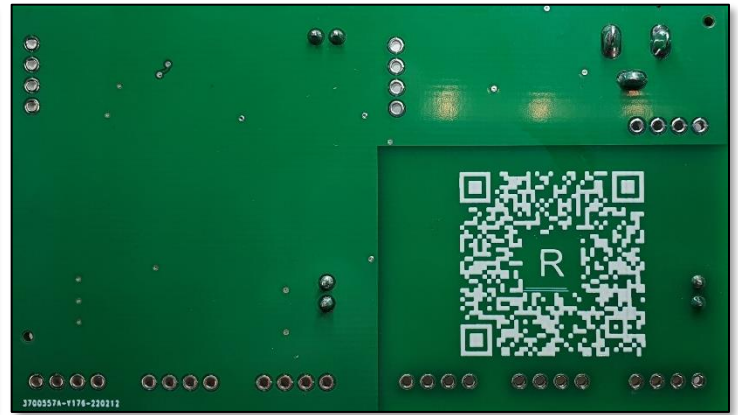


## Assembled board

- Board was powered ON using 5v adapter
- In bad design layout, longer trace was used for the decoupling capacitor to keep it away from the IC. Also, continuous return plane was not used for bad layout.



Top Layer



Bottom Layer

## What worked

### Your definition of what it means to work

For this lab, these are the criteria:

#### Power supply:

1. Check visually if LED for power is turned on
2. Measure the voltage of power rail on oscilloscope using 5V test point. Voltage should be around 5V.
3. Measure the voltage of power rail on oscilloscope using 3V3 test point. Voltage should be around 3.3V.
4. There should be a synchronous switching noise

#### 555-timer circuit:

1. Square wave should be visible on the oscilloscope when probed at 555 output test point.
2. Duty cycle of the square wave should be around 67%

#### Hex Inverter:

2. Inverted signal should be seen on one of the hex inverter outputs
3. Also, monitor for the switching noise on the Q -Hi and Q-Lo signals. There should be a difference in good and bad layouts

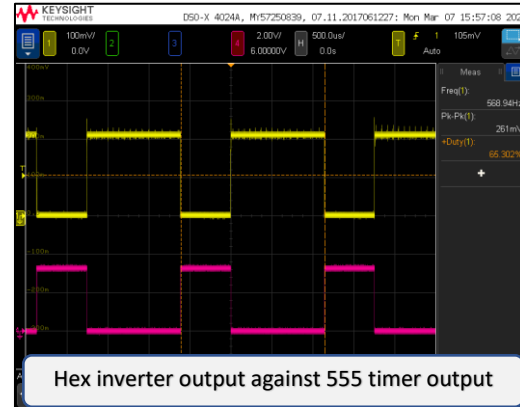
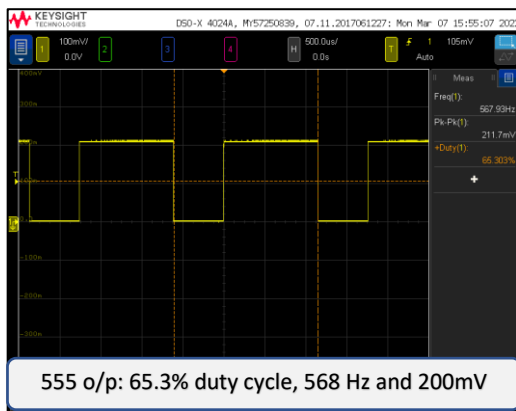
### Your expectations for any performance features

- Switching noise on bad layout
  - There would be switching noise because of
    - ◆ Decoupling capacitor away from the IC
    - ◆ Non-continuous return plane
  - This noise would be negligible on the good layout part

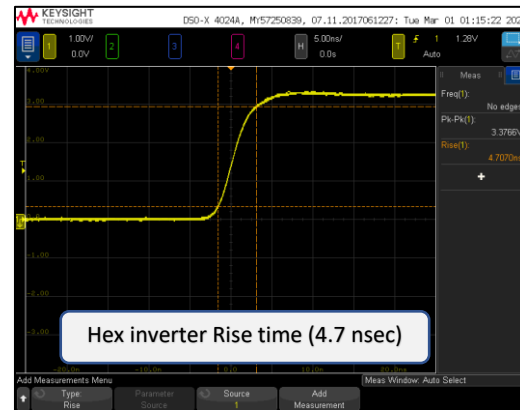
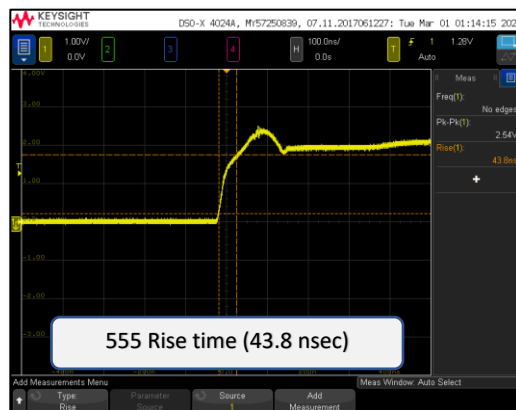
## What you actually measured to verify your board “worked”

- Measurement screenshots

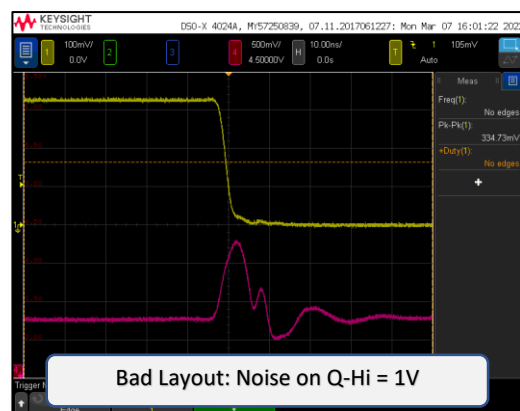
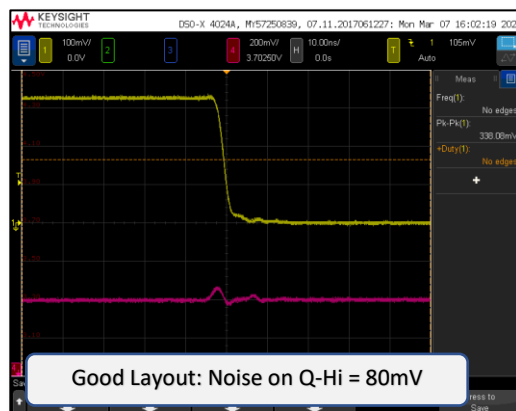
### a. 555 timer and Hex inverter output



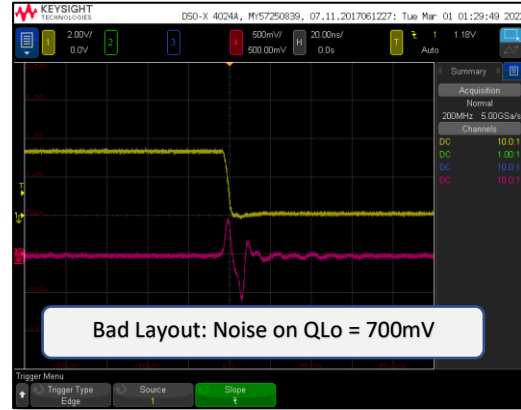
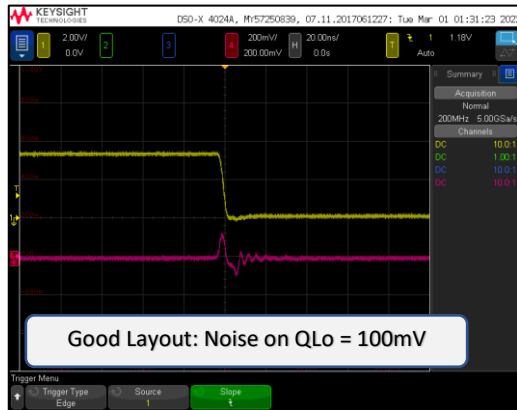
### b. comparison of rise time of hex-scope-trigger and 555 timer output



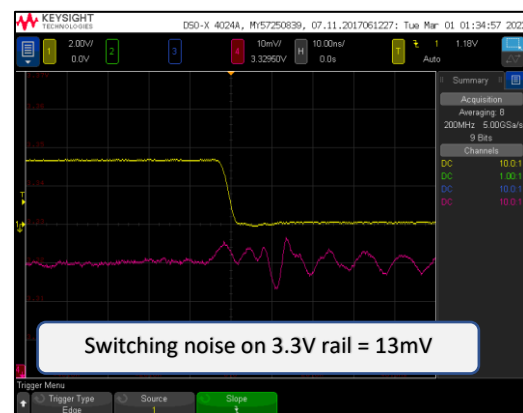
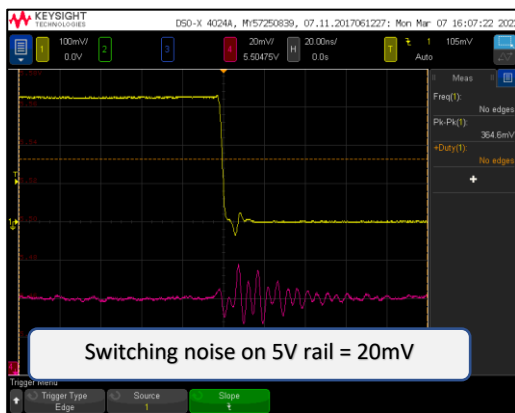
### c. Q hi outputs on good and bad layouts



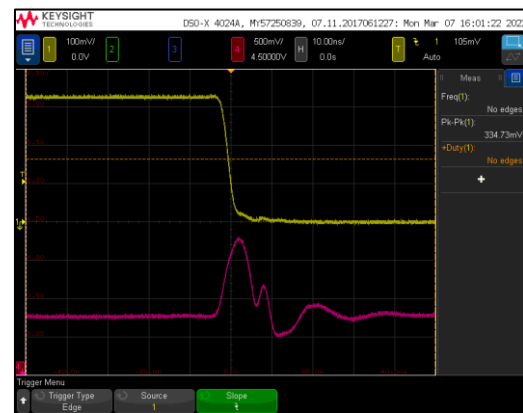
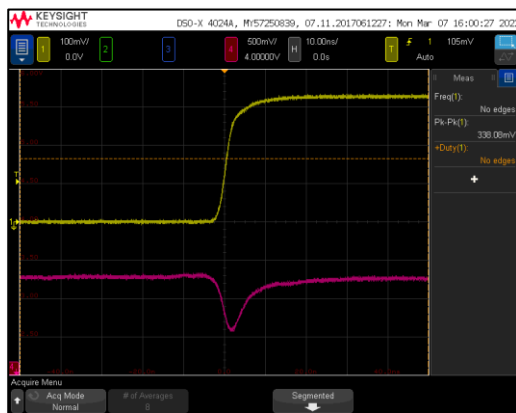
d. Q Lo outputs on good and bad layouts



f. Switching noise on power rails



e. Direction of switching noise



Apart from above measurements, LEDs were also monitored to see if that functional block is working.

## Your analysis of the measurements

### Duty Cycle

$$\begin{aligned} \text{Duty Cycle} &= \frac{\text{Time High}}{\text{Time Period}} \\ &= \frac{0.693 * (R_2 + R_3) * C_3}{0.693 * (R_2 + 2 * R_3) * C_3} \\ &= \frac{2}{3} \\ &= 66.67\% \end{aligned}$$

Above theoretical value roughly matches with the measured value

### Rise Time

- Measured rise time for 555 timer output is 43.8 nsec, whereas for Hex inverter output it is just 4.7 nsec.
- Lower the rise time higher the chances of switching noise due to  $L \frac{di}{dt}$  component.

### Q-Hi outputs on good and bad layouts

- Noise on Q-Hi pin on good layout is around 80mV. Whereas, it is around 1V on bad layout
- The measure contributing factor for this difference is
  - Proximity of decoupling capacitor
  - Continuous return plane
- Ideally the position of decoupling capacitor should be closest to the IC.

### Q-Lo outputs on good and bad layouts

- Noise on Q-Hi pin on good layout is around 100mV. Whereas it is around 700mV on bad layout
- The measure contributing factor for this difference is
  - Proximity of decoupling capacitor
  - Continuous return plane

### Noise on power rail

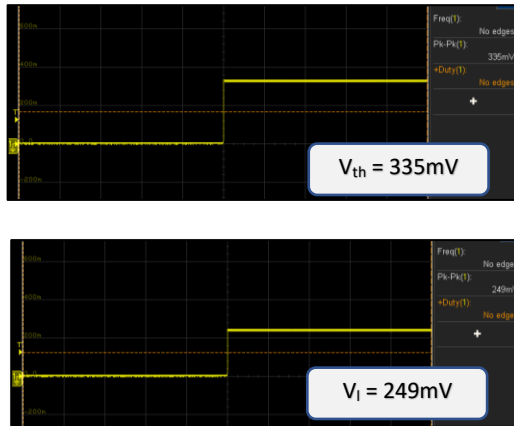
- Synchronous switching noise on 5v power rail is about 20mV and that about 3.3v power rail is 13mV.
- Power rail noise can be reduced by using decoupling capacitor in the close proximity of the IC.

### Frequency

$$\begin{aligned} \text{Frequency} &= \frac{\text{Time High}}{\text{Time Period}} \\ &= \frac{1.44}{(R_2 + 2 * R_3) * C_3} \\ &= \frac{1.44 * 1000}{3} \\ &= 480 \text{ Hz} \end{aligned}$$

Calculated value of 480 Hz is not matching with the measured value 568 Hz. Possible reason could be the wrong capacitor value on board affecting the R-R-C combination.

## Thevenin output resistance for Hex Inverter



$$\begin{aligned}V_{th} &= 335 \text{ mV} \\V_{load} &= 249 \text{ mV} \\R_L &= 47 \Omega \\ \text{Calculating for } R_{th}, \\ R_{th} &= R_L \left( \frac{v_{th} - v_{load}}{v_{load}} \right) \\ &= 47 \left( \frac{335 - 249}{249} \right) \\ &= 16 \Omega\end{aligned}$$

Calculated value of 480 Hz is not matching with the measured value 568 Hz. Possible reason could be the wrong capacitor value on board affecting the R-R-C combination.

## Demonstration of best design practices and best measurement practices

Best design practices include:

- Isolation of circuits using jumper switches
- Continuous return plane for the signals with good layout
- Also, non-continuous return plane for the bad layout design (study purpose)
- Decoupling capacitor close to the IC in good layout
- Labels for the components and test points.
- Name and Board Identification text on the top layer

Best measurement practices include:

- Spring tip of the probe is used to reduce mutual inductance and hence the crosstalk while measurement
- Probe was used in 10x mode and was compensated before taking the measurements.

## What did not work

- Frequency calculated and frequency measured did not match

## Analysis of your project:

### What worked and you did well and want to do in future designs

Power supply:

1. Power LED turned on
2. Voltage measured on power rail comes around 5v
3. Voltage measured across 3.3V test point comes around 3.3 V
4. Synchronous noise observed on power rail due to bad layout design practices

555 timer circuit:

1. Square wave is visible with duty cycle of 65%
2. This 555 timer output is then fed in to hex inverter

## Hex Inverter

1. Good Layout
  - a. Significantly low noise observed on Q-Hi line 80mV
  - b. Significantly low noise observed on Q-Lo line 100mV
2. Bad Layout
  - a. Significantly high noise observed on Q-Hi line 1V
  - b. Significantly high noise observed on Q-Lo line 700mV

This board was built to understand Good and Bad design practices. Following things were done right during this process,

- Continuous return plane for Good layout
- Decoupling capacitor in the close proximity of the IC in the good layout
- 6 mil trace for signals and 20 mil trace for powerlines
- Isolation switches used to isolate the power supply and 555 timer.
- Labels for the test points, components and board ID (name and description) text would be included in future designs as well
- Test points at appropriate points to measure important signals.

What did not work, and you will want to do differently in future designs.

- It worked as per requirement except the frequency which is off compared to theoretical value.
- Also, there is a chance of formation of antenna due to the kind of trace drawn for the placement of decoupling capacitor in bad layout.

Were there any hard errors- why did they go wrong

- No hard errors

Were there any soft errors that you would like to do differently next time?

- There could be an incorrect C4 capacitor value causing it to give incorrect frequency but correct duty cycle.
- Critical parts like this could be changed to 1206 in future as these could be hand-assembled.