Rajath Ramana

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SUMMARY

MS student in Electrical Engineering at the University of Pennsylvania with hands-on experience in RTL design & verification, accelerator microarchitectures, and SoC-level hardware from prior work at Qualcomm. Skilled in Verilog, C/Python, and hardware performance/area analysis. Excited to apply this background to innovative hardware design and verification across ASIC, FPGA, and SoC platforms.

EDUCATION

University of Pennsylvania, Philadelphia | PA, USA Aug 2025 – Dec 2026
Master of Science in Electrical Engineering

Advanced Computer Architecture, Chips Design & Measurement, SoC Architecture, GPGPU Architecture/Programming

National Institute of Technology, Tiruchirapalli | TN, India July 2019 – May 2023
Bachelor of Technology in Electrical and Electronics Engineering *GPA: 3.89 (9.01/10.0)*

VLSI Fundamentals & Digital Electronics, Microprocessors & Microcontrollers, Embedded Systems, Analog Electronics

EXPERIENCE

Qualcomm Hyderabad, India
RTL Design Engineer *July 2023 – August 2025*

- Led RTL design for CMSR & TCSR IP's from spec to tape-out, delivering into high-volume XR/MSM SoCs.
- Architected centralized MEMRED & MEMACC fuse distribution for Qualcomm SoC's, eliminating **60K retention flops**, improving speed, performance and efficiency by almost **20%** compared to legacy implementations.
- Automated SoC integration flows using Python & Tcl, reducing integration time & human errors across tape-outs.
- Resolved Lint & CDC issues across **50 plus SoC cores**, preventing synthesis failures & ensuring timing closure.
- Executed post-code-freeze ECOs to resolve **30 plus** RTL & gate-level issues across the SoC during MTO / BTO phases; collaborated with synth, DV & PD teams to ensure ECO convergence, logic equivalance & sign-off readiness.

VLSI Laboratory, NIT-T Tiruchirappalli, India
Verification & FPGA Design Intern *Jan 2022 – May 2022*

- Prototyped FPGA encryption accelerators on Spartan-6, delivering **15–20x** faster throughput than software.
- Built RTL testbenches, achieving **85%** functional coverage using directed/random tests & golden-model checks.
- Verified FPGA system stability on hardware, confirming clean clock/reset sequencing and consistent I/O timing.

PROJECTS

- **High-Throughput Heterogeneous Compression Engine (ARM + NEON + FPGA)**
- Engineered a real-time compression pipeline targeting **400 Mb/s** on Ultra96 SoC, analyzing bottlenecks and parallelism.
- Partitioned compute across ARM cores, NEON intrinsics, and FPGA fabric to eliminate key stalls in the pipeline.
- Verified end-to-end correctness using custom RTL testbenches, OpenCL host/device integration, and Ethernet streaming.

- **Hardware Cryptographic Accelerator for Secure Smart Metering (Bachelor Thesis)**
- Designed Verilog RTL for AES-GCM, SHA-256, and ECDSA/ECDH blocks, optimizing datapaths & modular arithmetic.
- Analyzed cycle behavior of GHASH, SHA scheduling, and ECC scalar operations to guide small architectural refinements.
- Validated on Basys-3 with 100% match to software golden models and NIT-T smart-meter field data.

- **CUDA-Accelerated Sparse Kernel Optimization**
- Developed optimized CSR SpMM kernels with warp specialization & vectorized memory paths for higher throughput.
- Profiled GPU execution behavior, observing a 12% drop in warp divergence after reorganizing access patterns.
- Benchmarked against PyTorch sparse ops, identifying utilization limits driven by cache locality and SM occupancy.

SKILLS

- **Hardware/Design:** RTL Design & Verification, ASIC/SoC/FPGA Microarchitecture, CDC/RDC, PPA Analysis
- **Languages/OS Tools** : Verilog/VHDL, SystemVerilog (SV/UVM), C/C++, Python, Tcl, Perl, Make, Linux, CUDA
- **EDA Tools:** Xilinx Vivado, Synopsys VCS, Cadence Virtuoso, ModelSim, Spyglass CDC/PLDRC, Vitis HLS, Verdi