
UNIVERSITY OF ROCHESTER
ECE -200

LAB-3

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Abstract Summary:

The lab requires us to create an ALU unit and a Register Unit. Implementing this lab would require us to design an ALU module, a Register module and a ALU control module to control the function of ALU.

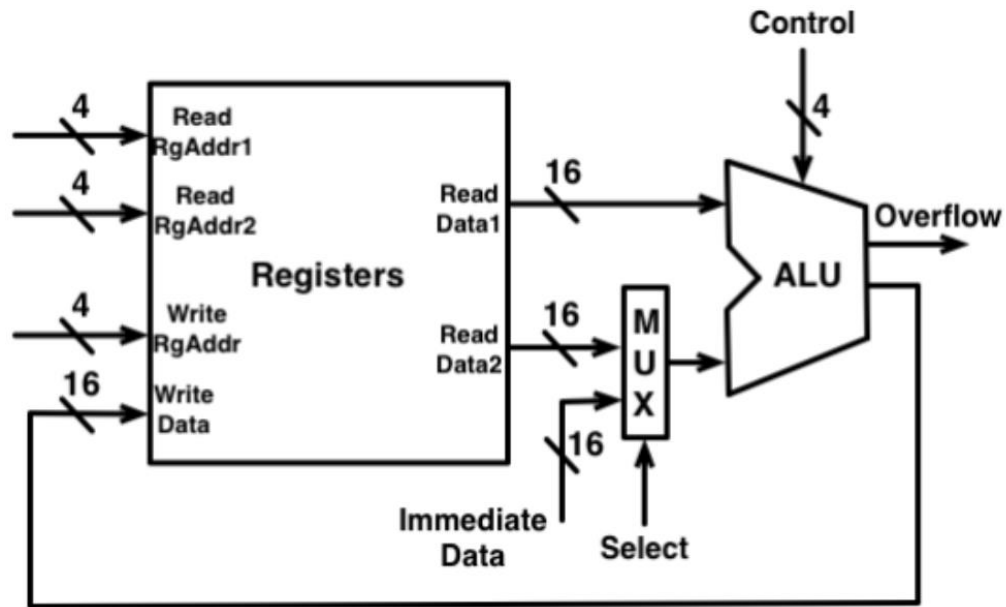
Introduction:

An ALU (Arithmetic Logic Unit) is a combination if many modules like Adder, AND & OR module which indeed are made of logic gates. The purpose of ALU is to perform calculations based on the instruction code or also called OP Code. The output will depend on the input and the instruction given to the ALU.

ALU Controls	Functions
0000	AND
0001	OR
0010	ADD
0110	SUB
0111	SLT
1100	NOR

Design Approach:

The Registers take 2, 4 bit input and a 4 bit destination register. Then a 16bit instruction is sent to the ALU which processes the input and write the 16bit data to the destination register.



Comments:

Through this lab, we were able to implement an ALU and register file using Verilog in Modelsim. I had a little trouble with making the test bench properly but when assigning the values manually to the inputs through model sim, the result came out as expected. The only problem that could surf up is the writing back of data to memory register.