UNIVERSITY OF ROCHESTER

ECE -200

LAB-2

Rajat Kuthiala

Abstract Summary:

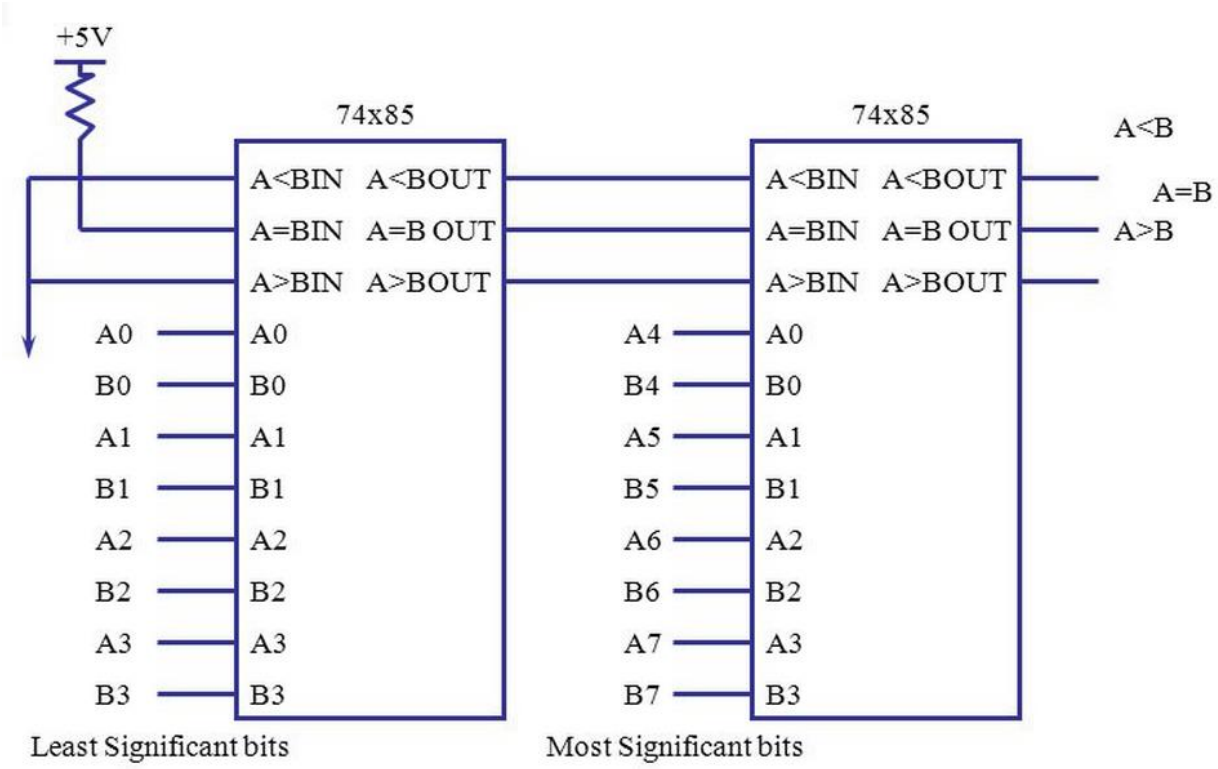
Through this lab we were able to learn about modelsim and Verilog. The lab required us to build a comparator which compared 2- 8 bit numbers and compare their value with each other.

Introduction:

-Part 2: 8-bit comparator that takes two 8-bit binary values (A and B) as inputs. Output is 1, if A is greater than B; output is 0, if A is equal to B; and output is 2, if A is smaller than B.

Design Approach:

The design was pretty straightforward by comparing the A_n bit with B_n bit.



Comments:

Through this lab we were able to simulate ALU on modelsim and observe the result and got hands on experience with Verilog. The results were obtained by simulating the model in Modelsim and the output were obtained as per expectations.