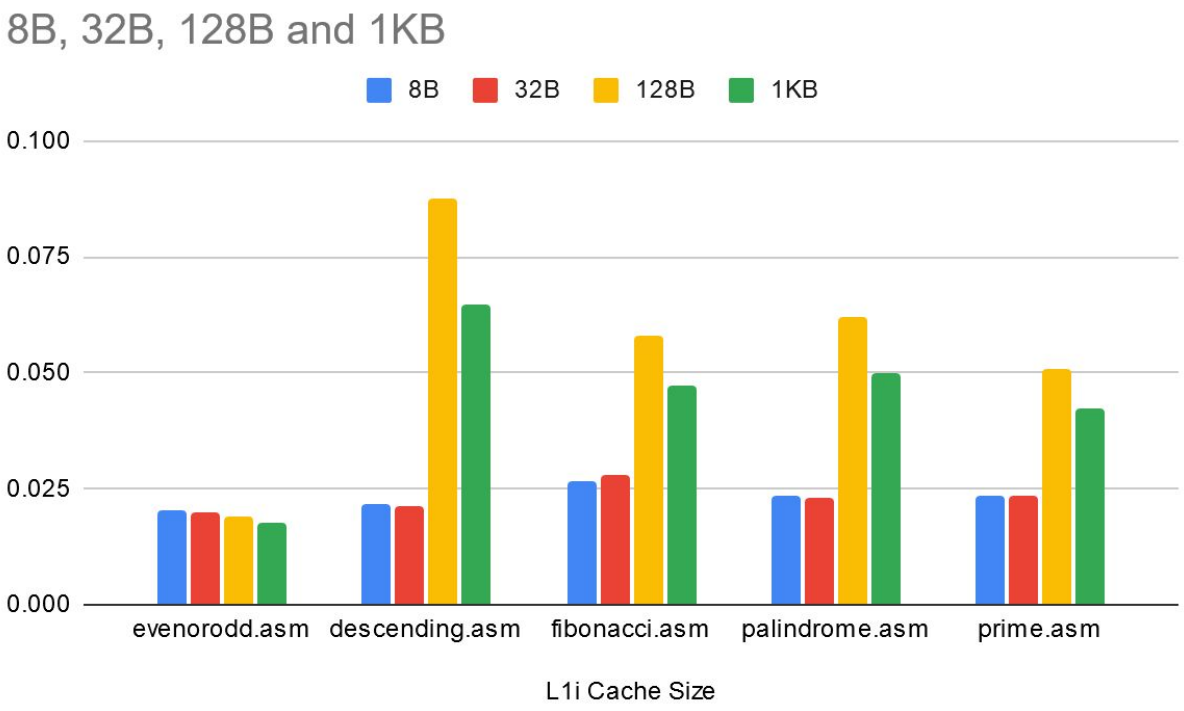
ASSIGNMENT 6 REPORT

L1D Cache Size = 1KB

L1i Cache Size	evenorodd.asm	descending.asm	fibonacci.asm	palindrome.asm	prime.asm
8B	0.02023121387	0.02155029192	0.026736691	0.02344877344	0.02341920
32B	0.01983002832	0.02109567399	0.028133634	0.02291152626	0.02341920
128B	0.01907356948	0.08749277317	0.058181818	0.06208213944	0.05076141
1KB	0.01772151898	0.06481084939	0.047197640	0.04973221117	0.04219409



Analysis:

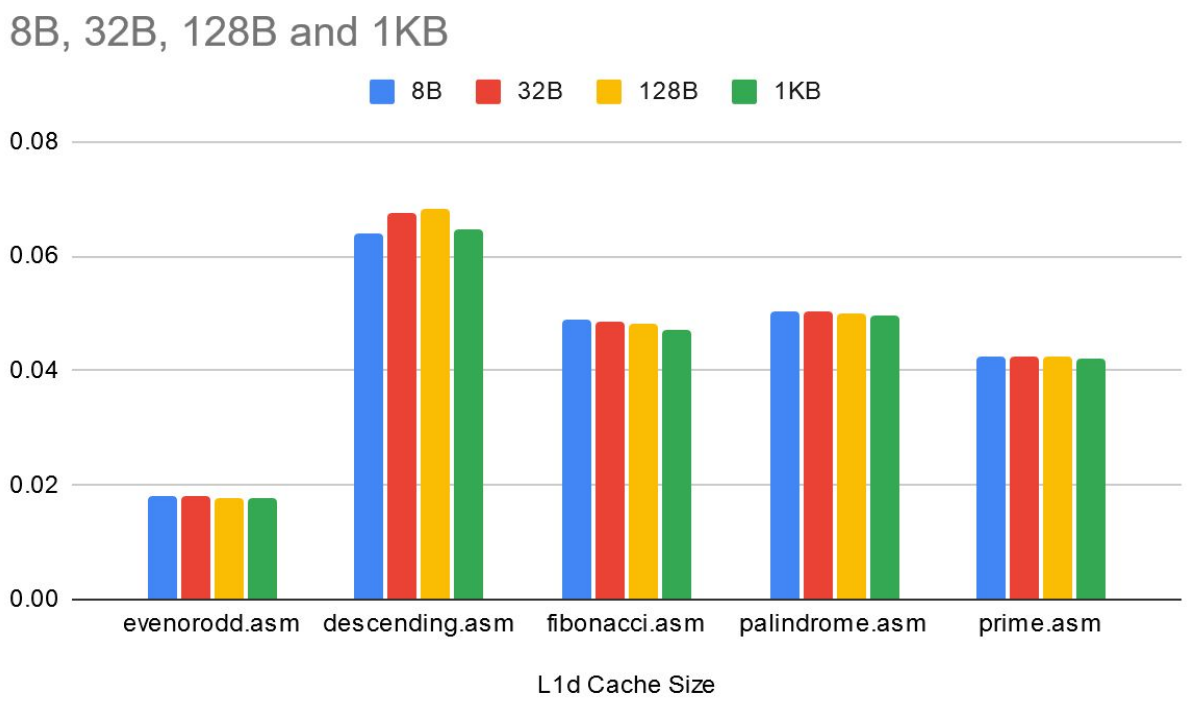
Increasing cache has 2 effects: higher hit ratio, higher latency. We kind of want to goto some kind of maxima in between. For small codes such as evenorodd.asm size of cache has very small effect on hit ratio, that makes the trades between hit ratio and latency very expensive that what happened here increasing size for evenorodd.asm led to decrement in overall throughput. Whereas for longer code such as other increment cache size till 128B was good tradeoff after that increasing cache size resulted in decrease in performance due to relatively more increase in latency.

ASSIGNMENT 6 REPORT

L1i Cache Size = 1KB

L1d Cache Size	evenorodd.asm	descending.asm	fibonacci.asm	palindrome.asm	prime.asm
8B	0.0180412371134021	0.0639256547451422	0.0487804878048781	0.0502706883217324	0.0425079702444208
32B	0.0179948586118252	0.0676501266577261	0.0485478977026441	0.0501930501930502	0.0424628450106157
128B	0.0179028132992327	0.0682809445029328	0.0480893087161872	0.0500384911470362	0.0423728813559322
1KB	0.0177215189873418	0.0648108493932905	0.0471976401179941	0.0497322111706197	0.0421940928270042

Ana



Analysis

As there not much memory access operation involved except the descending,asm. So increase in cache size has very less effect on overall throughput. Similar reasoning can be provided as provided for evenorodd.asm in the previous section for codes with less number of memory access events. In descending.asm the number of memory accesses are low to have any major effect in performance but are available to show changes in performance and tradeoff between latency and cache hit ratio.