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10CS46

Fourth Semester B.E. Degree Examination, Dec.2014/Jan. 2015
Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the basic operational concepts between the processor and the memory. **(08 Marks)**
b. How to measure the performance of the computer? Explain. **(06 Marks)**
c. Write a note on byte addressability, big-endian and little – endian assignment. **(06 Marks)**

2 a. What is an addressing mode? Explain any four types of addressing modes, with example. **(08 Marks)**
b. With example, explain subroutine stack frame. **(06 Marks)**
c. Explain how to encode the instructions into 32 – bit words. **(06 Marks)**

3 a. What is an interrupt? With example illustrate the concept of interrupts. **(06 Marks)**
b. Explain in detail, the situations where a number of devices capable of initiating interrupts are connected to the processor? How to resolve the problems? **(08 Marks)**
c. Explain the two approaches for bus arbitration. **(06 Marks)**

4 a. Describe how a read operation is performed on a PCI bus. **(10 Marks)**
b. List the sequence of events that takes place when a processor sends a commands to the SCSI controller. **(10 Marks)**

PART – B

5 a. Discuss the internal organization of a 2M × 8 asynchronous DRAM chip. **(10 Marks)**
b. Describe the different mapping functions in cache. **(10 Marks)**

6 a. Write the logic diagram of 4 – bit carry look ahead adder. Explain the operation. **(06 Marks)**
b. Perform multiplication for –13 and + 9 using Booth's algorithm. **(06 Marks)**
c. Write the circuit arrangement for binary division. Perform the restoring division for the given binary numbers 1000 ÷ 11, show all the cycles. **(08 Marks)**

7 a. Explain the three – bus organization of the processor. **(08 Marks)**
b. Discuss the organization of hardwired control unit. **(08 Marks)**
c. Write the micro-routine for the instruction Add – (Rsrc), Rdst. **(04 Marks)**

8 a. With a neat diagram, explain the organization of a shared memory multiprocessor. **(08 Marks)**
b. What is hardware multithreading? Explain the three approaches to hardware multithreading. **(08 Marks)**
c. Explain : i) SISD ii) MIMD iii) SIMD and iv) SPMD. **(04 Marks)**

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.