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06CS46

Fourth Semester B.E. Degree Examination, Dec. 2013/Jan. 2014
Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With a general block diagram, explain the functions of each of the processor registers. **(08 Marks)**

b. Highlighting important technological features and advances, explain the evolution of computer over different generations. **(08 Marks)**

c. With suitable example, explain how performance is measured using SPEC rating and give its significance. **(04 Marks)**

2 a. Convert the following pair of decimal numbers into 5 bit singed 2's complement binary numbers and perform operations indicated. Also state if overflow occurs.
i) – 10 and – 13 (addition) ii) – 14 and 11 (subtraction) iii) – 3 and – 8 (addition)
iv) – 10and – 13 (subtraction) **(08 Marks)**

b. Given the following instruction, rewrite using only direct, indirect and immediate addressing modes to achieve the same effect : move 123 (R_1, R_2), (R_3, R_4). **(05 Marks)**

c. What is a stack frame? Explain its use in subroutines. **(07 Marks)**

3 a. What is an interrupt? Explain its concepts and the hardware used to realize it. **(06 Marks)**

b. What is the necessity of DMA? Explain the two modes in which DMA interface operates to transfer data. **(06 Marks)**

c. Explain the bus arbitration approaches with the help of neat sketches. **(08 Marks)**

4 a. Explain the combined input/output interface circuit, with help of a neat logic block diagram. **(10 Marks)**

b. With respect to USB, discuss the USB architecture, addressing and protocol adopted. **(10 Marks)**

PART – B

5 a. With a block diagram, explain the organization of 8 M × 32 memory using 512 K × 8 memory chips. **(10 Marks)**

b. Explain the working of a dynamic memory cell. **(05 Marks)**

c. What is memory interleaving? Explain. **(04 Marks)**

d. Calculate the average access time experienced by a processor if cache hit rate is 0.88, miss penalty is 0.015 milliseconds and cache access time is 10 micros seconds. **(04 Marks)**

6 a. Explain how virtual memory address translation based on fixed - length pages is organized and achieved. **(08 Marks)**

b. Explain the design of a 4 – bit carry – lookahead adder. **(08 Marks)**

c. Write a note on optical technology used in CD systems. **(04 Marks)**

7 a. Draw the circuit diagram for binary division. Explain the non – restoring division algorithm, with suitable example. **(10 Marks)**

b. Explain the IEEE standard for floating point number representation. **(10 Marks)**

8 a. Mention and explain the control sequences for execution of an unconditional branch instruction. **(10 Marks)**

b. With a block diagram, explain the basic organization of a micro-programmed control unit. **(10 Marks)**