



01 : 57 : 08



Exit

**Choose the correct option**

Q80 / 80

Full form of CPI

**OPTIONS**

cycle per instruction

clock per instruction

count per instruction

cycle per implementation

**SKIP****SUBMIT ANSWER**



01 : 57 : 12



Exit

**Choose the correct option**

Q78 / 80

MIMD stands for

**OPTIONS**

Multiple instruction memory data

Multiple instruction multiple data

memory instruction multiple data

Multiple information memory data

**SKIP****SUBMIT ANSWER**



01 : 57 : 10



Exit

**Choose the correct option**

Q79 / 80

ADD R1,R2,R3 belongs to which addressing mode?

**OPTIONS**

Immediate Addressing

Direct addressing

Register

**SKIP****SUBMIT ANSWER**



01 : 57 : 14



Exit

**Choose the correct option**

Q77 / 80

Each digit position of a binary number has a \_\_ in power of \_\_

**OPTIONS**

weight,2

sign,4

sign,2

**SKIP****SUBMIT ANSWER**



01 : 57 : 16



Exit

**Choose the correct option**

Q76 / 80

Pipeline implementation of CISC architecture is

**OPTIONS**

complex

simple

**SKIP****SUBMIT ANSWER**



01 : 57 : 18



Exit

**Choose the correct option**

Q75 / 80

The average time required to reach a storage location in memory and obtain its contents is called

**OPTIONS**

Access time

Latency time

Turnaround time

Response time

**SKIP****SUBMIT ANSWER**



01 : 57 : 20



Exit

**Choose the correct option**

Q74 / 80

ADD R1,2106H belongs to which addressing mode?

**OPTIONS**

Immediate Addressing

Direct addressing

Register

**SKIP****SUBMIT ANSWER**



01 : 57 : 24



Exit

**Choose the correct option**

Q73 / 80

Logic gates with a set of input and outputs, is arrangement of\_\_\_\_\_.

**OPTIONS**

Logic Circuits

Computational circuit

Design Circuits

Registers

**SKIP****SUBMIT ANSWER**



01 : 57 : 28



Exit

**Choose the correct option**

Q72 / 80

Consider the following statements: (i) RISC architecture increases number of instructions per program. (ii) RISC architecture increases CPI and clock cycle time. Which of the following is correct?

**OPTIONS**

Only (ii) is true

Only (i) is true

Both (i) and (ii) are true

Both (i) and (ii) are false

**SKIP****SUBMIT ANSWER**



01 : 57 : 30



Exit

**Choose the correct option**

Q71 / 80

On which of the following does CPI depend on?

**OPTIONS**

Complier

Instruction set Architecture

CPU organization

All of these

**SKIP****SUBMIT ANSWER**



01 : 57 : 32



Exit

**Choose the correct option**

Q70 / 80

Which of the following is the most widely used alphanumeric code for computer input and output?

**OPTIONS**

ASCII

Gray

Parity

EBCDIC

**SKIP****SUBMIT ANSWER**



01 : 57 : 34



Exit

**Choose the correct option**

Q69 / 80

The instruction contains a field that holds the memory address, which in turn holds the memory address of the operand. Identify the addressing mode

**OPTIONS**

Immediate Addressing

Direct addressing

Indirect

**SKIP****SUBMIT ANSWER**



01 : 57 : 36



Exit

**Choose the correct option**

Q68 / 80

In MIPS 32 which of the following register is missing?

**OPTIONS**

PC

IP

SP

**SKIP****SUBMIT ANSWER**



01 : 57 : 38



Exit

**Choose the correct option**

Q67 / 80

For the instruction STORE R1,35(R2) what will be effective address of the memory operand if R2 is 200 (in decimal)?

**OPTIONS**

165

35

200

235

**SKIP****SUBMIT ANSWER**



01 : 57 : 40



Exit

**Choose the correct option**

Q66 / 80

Floating point representation is used to store

**OPTIONS**

Whole numbers

Boolean values

Real integers

Integers

**SKIP****SUBMIT ANSWER**



01 : 57 : 42



Exit

**Choose the correct option**

Q65 / 80

\_\_\_ defines the number of cycles between an instruction producing a result and another instruction using it.

**OPTIONS**

Latency

Interval

**SKIP****SUBMIT ANSWER**



01 : 57 : 43



Exit

**Choose the correct option**

Q64 / 80

Superscalar machines can result in CPI

**OPTIONS**

greater than 1

less than 1

less than 0

**SKIP****SUBMIT ANSWER**



01 : 57 : 45



Exit

**Choose the correct option**

Q63 / 80

A full subtracter circuit requires \_\_\_\_\_.

**OPTIONS**

two inputs and three outputs

two inputs and two outputs

three inputs and one output

three inputs and two outputs

**SKIP****SUBMIT ANSWER**



01 : 57 : 47



Exit

**Choose the correct option**

Q62 / 80

A vector processor is characterised by

**OPTIONS**

No loop overhead.

good speedup when we carry out similar operations on vectors.

The number of instructions gets reduced.

All of these

**SKIP****SUBMIT ANSWER**



01 : 57 : 49



Exit

**Choose the correct option**

Q61 / 80

In a tightly coupled multiprocessor all the processors have access to a common shared memory.

**OPTIONS**

true

false

**SKIP****SUBMIT ANSWER**



01 : 57 : 51



Exit

**Choose the correct option**

Q60 / 80

Which one out of the Following is characterised by multiple ALU and registers?

**OPTIONS****Single core architecture****Multicore architecture****SKIP****SUBMIT ANSWER**



01 : 57 : 53



Exit

**Choose the correct option**

Q59 / 80

The radix of a number system defines

**OPTIONS**

total digits in a system

maximum value

minimum value

**SKIP****SUBMIT ANSWER**



01 : 57 : 55



Exit

**Choose the correct option**

Q58 / 80

CCT can be reduced by

**OPTIONS**

increasing the number of pipeline stages.

reducing the number of pipeline stages.

removing the number of pipeline stages.

**SKIP****SUBMIT ANSWER**



01 : 57 : 58



Exit

**Choose the correct option**

Q57 / 80

VLIW stands for

**OPTIONS**

Very Long Instruction Word

Viscous Long Instruction Word

**SKIP****SUBMIT ANSWER**



01 : 58 : 00



Exit

**Choose the correct option**

Q56 / 80

Digital representations of numerical values of quantities may BEST be described as having characteristics:

**OPTIONS**

that vary constantly over a continuous range of values.

that are difficult to interpret because they are continuously changing.

that vary in constant and direct proportion to the values they represent.

that vary in discrete steps in proportion to the values they represent.

**SKIP****SUBMIT ANSWER**



01 : 58 : 02



Exit

**Choose the correct option**

Q55 / 80

The instruction in different stages of the pipeline do not interfere with one another, the

**OPTIONS**

pipeline stacks

pipe stage

pipeline registers

processor cycle

**SKIP****SUBMIT ANSWER**



01 : 58 : 04



Exit

**Choose the correct option**

Q54 / 80

When the compiler attempts to schedule instructions to avoid the hazard is known as

**OPTIONS**

Static scheduling

Compiler

Dynamic scheduling

Both a and b

**SKIP****SUBMIT ANSWER**



01 : 58 : 07



Exit

**Choose the correct option**

Q53 / 80

Indicating which of the four steps the instruction is in, is provided by

**OPTIONS**

instruction id

instruction set

instruction decoding

instruction status

**SKIP****SUBMIT ANSWER**



01 : 58 : 09



Exit

**Choose the correct option**

Q52 / 80

The instruction following the branch is always executed before the PC is modified to perform the branch is known as

**OPTIONS**

branch hazard

delayed branch

structural hazard

data hazard

**SKIP****SUBMIT ANSWER**



01 : 58 : 11



Exit

**Choose the correct option**

Q51 / 80

If the stages are perfectly balanced, then the time per instruction on the pipelined processor, is equal to

**OPTIONS**

time per instruction on unpipelined machine\*  
no of piped stages

time per instruction on unpipelined machine/  
no of piped stages

time per instruction on unpipelined machine  
+ no of piped stages

time per instruction on unpipelined machine -  
no of piped stages

**SKIP****SUBMIT ANSWER**



01 : 58 : 13



Exit

**Choose the correct option**

Q50 / 80

Which of the following is true about DMA?

**OPTIONS**

The DMA controller acts as a processor for DMA transfers and overlooks the entire process.

DMA is an approach of performing data transfers in bulk between memory and the external device without the intervention of the processor.

The DMA controller has 3 registers.

All of the above

**SKIP****SUBMIT ANSWER**



01 : 58 : 15



Exit

**Choose the correct option**

Q49 / 80

Components that provide internal storage to the CPU  
are \_\_\_\_\_

**OPTIONS**

Program Counters

Registers

Controllers

Internal chips

**SKIP****SUBMIT ANSWER**



01 : 58 : 17



Exit

**Choose the correct option**

Q48 / 80

In \_\_\_\_\_ mode, the I/O module and main memory exchange data directly, without processor involvement

**OPTIONS**

DMA

Programmed I/O

Interrupt-driven I/O

All the above

**SKIP****SUBMIT ANSWER**



01 : 58 : 19



Exit

**Choose the correct option**

Q47 / 80

Which of the following is used to hold running program instructions?

**OPTIONS**

Virtual Storage

Primary Storage

Internal Storage

Minor Devices

**SKIP****SUBMIT ANSWER**



01 : 58 : 22



Exit

**Choose the correct option**

Q46 / 80

Which of the following are not true for DMA data transfer?

**OPTIONS**

CPU puts all its memory bus lines in high impedance state before data transfer can begin.

Data are transferred directly between the memory and the peripheral without CPU intervention

It is more suitable for devices where the data transfer rates can vary widely

None of the above.

**SKIP****SUBMIT ANSWER**



01 : 58 : 23



Exit

**Choose the correct option**

Q45 / 80

Pipelining increases the CPU instruction

**OPTIONS**

Through put

Size

Cycle rate

Time

**SKIP****SUBMIT ANSWER**



01 : 58 : 25



Exit

**Choose the correct option**

Q44 / 80

With the help of \_\_\_\_\_, the fetch and execution cycles are interleaved.

**OPTIONS**

Clock

Modification in processor architecture

Special Unit

Control Unit

**SKIP****SUBMIT ANSWER**



01 : 58 : 27



Exit

**Choose the correct option**

Q43 / 80

The set of instructions examined as candidates for potential execution is called the

**OPTIONS**

Register

Frame

Window

Blocked

**SKIP****SUBMIT ANSWER**



01 : 58 : 29



Exit

**Choose the correct option**

Q42 / 80

Every time during execution time if the event occurs at the same place with the same data and memory allocation is known as

**OPTIONS**

Synchronous

Asynchronous

Delayed

Stalled

**SKIP****SUBMIT ANSWER**



01 : 58 : 29



Exit

**Choose the correct option**

Q42 / 80

Every time during execution time if the event occurs at the same place with the same data and memory allocation is known as

**OPTIONS**

Synchronous

Asynchronous

Delayed

Stalled

**SKIP****SUBMIT ANSWER**



01 : 58 : 31



Exit

**Choose the correct option**

Q41 / 80

Code containing redundant loads, stores, and other operations that might be eliminated by an optimizer, is

**OPTIONS**

Unoptimized clock

Optimized clock

Optimized code

Unoptimized code

**SKIP****SUBMIT ANSWER**



01 : 58 : 33



Exit

**Choose the correct option**

Q40 / 80

If a unit completes its task before the allotted time period, then

**OPTIONS**

Its time gets reallocated to a different task

It'll perform some other task in the remaining time

It'll remain idle for the remaining time

None of the above

**SKIP****SUBMIT ANSWER**



01 : 58 : 37



Exit

**Choose the correct option**

Q39 / 80

The process of letting an instruction move from decode stage into the execution stage of this pipeline is usually called

**OPTIONS**

Instruction issue

Cancellation

Nullifying

Branch prediction

**SKIP****SUBMIT ANSWER**



01 : 58 : 39



Exit

**Choose the correct option**

Q38 / 80

Pipeline overhead arises from the combination of pipeline register delay and \_\_\_\_.

**OPTIONS**

Clock cycle

Hit rate

Cycle rate

Clock skew

**SKIP****SUBMIT ANSWER**



01 : 58 : 42



Exit

**Choose the correct option**

Q37 / 80

The process contends for the usage of the hardware  
and might enter into a \_\_\_\_.

**OPTIONS**

Stall state

Hazard state

Deadlock state

None of the above

**SKIP****SUBMIT ANSWER**



01 : 58 : 44



Exit

**Choose the correct option**

Q36 / 80

How many types of pipeline exists?

**OPTIONS**

3

2

4

5

**SKIP****SUBMIT ANSWER**



01 : 58 : 45



Exit

**Choose the correct option**

Q35 / 80

The sum value in Full adder is characterized by the equation

**OPTIONS****S=A XOR B XOR C****S= A AND B AND C****S=A OR B OR C****SKIP****SUBMIT ANSWER**



01 : 58 : 47



Exit

**Choose the correct option**

Q34 / 80

If we multiply 4 bit by 4 bit number the resultant will be \_\_\_ bits

**OPTIONS**

8

16

4

24

**SKIP****SUBMIT ANSWER**



01 : 58 : 49



Exit

**Choose the correct option**

Q33 / 80

Convert hex 777 to decimal

**OPTIONS**

1920

1911

5911

1919

**SKIP****SUBMIT ANSWER**



01 : 58 : 51



Exit

**Choose the correct option**

Q32 / 80

ALU is responsible to perform operations like

**OPTIONS**

Both Arithmatical and Logical Operations

Logical Operations

Addition

Data transfer

**SKIP****SUBMIT ANSWER**



01 : 58 : 53



Exit

**Choose the correct option**

Q31 / 80

Processors are only used for execution of programs

**OPTIONS**

true

false

**SKIP****SUBMIT ANSWER**



01 : 58 : 55



Exit

**Choose the correct option**

Q30 / 80

Which of the following is not a valid register Name?

**OPTIONS****General Purpose Registers****Address Register****Status Register****SKIP****SUBMIT ANSWER**



01 : 58 : 57



Exit

**Choose the correct option**

Q29 / 80

Storage which stores or retains data after power off is called

**OPTIONS**

Non-volatile storage

Volatile storage

Sequential storage

Direct storage

**SKIP****SUBMIT ANSWER**



01 : 59 : 01



Exit

**Choose the correct option**

Q28 / 80

Highly encoded schemes that use compact codes to specify a small number of functions in each micro instruction is \_\_\_\_\_

**OPTIONS**

Vertical Organisation

Horizontal Organisation

Diagnol Organisation

None of the mentioned

**SKIP****SUBMIT ANSWER**



01 : 59 : 03



Exit

**Choose the correct option**

Q27 / 80

Which of the following approaches can be used for reducing cache miss rate?

**OPTIONS**

Use larger cache

Use larger block size

Use higher associativity

All of Above

**SKIP****SUBMIT ANSWER**



01 : 59 : 05



Exit

**Choose the correct option**

Q26 / 80

To read the control words sequentially \_\_\_\_\_ is used.

**OPTIONS**

IR

PC

UPC

None of the mentioned

**SKIP****SUBMIT ANSWER**



01 : 59 : 07



Exit

**Choose the correct option**

Q25 / 80

In micro-programmed approach, the signals are generated by \_\_\_\_\_

**OPTIONS**

System programs

Machine instructions

Utility tools

None of the mentioned

**SKIP****SUBMIT ANSWER**



01 : 59 : 09



Exit

**Choose the correct option**

Q24 / 80

A sequence of control words corresponding to a control sequence is called \_\_\_\_\_

**OPTIONS**

Micro function

Micro routine

Micro procedure

None of the mentioned

**SKIP****SUBMIT ANSWER**



01 : 59 : 09



Exit

**Choose the correct option**

Q24 / 80

A sequence of control words corresponding to a control sequence is called \_\_\_\_\_

**OPTIONS**

Micro function

Micro routine

Micro procedure

None of the mentioned

**SKIP****SUBMIT ANSWER**



01 : 59 : 11



Exit

**Choose the correct option**

Q23 / 80

Which of the following statement(s) is/are true for fetching a word from memory?

**OPTIONS**

The information to be fetched, must be an instruction/operand.

The word can be directly loaded to general purpose registers from memory

The word can be directly transferred to ALU for further operation

all of these

**SKIP****SUBMIT ANSWER**



01 : 59 : 13



Exit

**Choose the correct option**

Q22 / 80

Consider the following set of micro-operations for a single bus architecture machine: Step Action T1: PCout, MARin, Read, Select4, Add, Zin T2: Zout, PCin, Yin, WMFC T3: MDRout, IRin T4: R3out, Yin, SelectY T5: R4out, ADD, Zin T6: Zout, R3in, End The micro-operation corresponds to which instruction?

**OPTIONS**

ADD R3, Y

ADD Y, R4

ADD R3, R4

MOVE R3, R4

**SKIP****SUBMIT ANSWER**



01 : 59 : 15



Exit

**Choose the correct option**

Q21 / 80

In a three BUS architecture, how many input and output ports are there?

**OPTIONS**

1 output and 2 input

2 output and 2 input

2 output and 1 input

1 output and 1 input

**SKIP****SUBMIT ANSWER**



01 : 59 : 17



Exit

**Choose the correct option**

Q20 / 80

Which of the following statements is/are true with respect to Amdahl's law?

**OPTIONS**

It provides a measure to compare execution time of two machines

It express the law of diminishing returns

None of these

All of these

**SKIP****SUBMIT ANSWER**



01 : 59 : 19



Exit

**Choose the correct option**

Q19 / 80

If the instruction size of a machine is 64 bit long, which has a byte addressable memory then to point to the next instruction the PC value should be incremented by \_\_\_\_?

**OPTIONS**

8

4

2

16

**SKIP****SUBMIT ANSWER**



01 : 59 : 24



Exit

**Choose the correct option**

Q18 / 80

Consider the following statement: (i) Program Counter holds address of the memory location containing the next instruction to be executed (ii) Instruction Register contains the next instruction to be executed. Which of the following is correct?

**OPTIONS****Only (ii) is true****Only (i) is true****Both (i) and (ii) are true****Both (i) and (ii) are false****SKIP****SUBMIT ANSWER**



01 : 59 : 26



Exit

**Choose the correct option**

Q17 / 80

A word whose individual bits represent a control signal is \_\_\_\_\_

**OPTIONS**

Control word

Command word

Co-ordination word

Generation word

**SKIP****SUBMIT ANSWER**



01 : 59 : 28



Exit

**Choose the correct option**

Q16 / 80

Consider the following statements: (i) MIPS rating is used to compare performance of two processors. (ii) Higher MIPS rating indicates better performance. Which of the following is correct?

**OPTIONS**

Only (ii) is true

Only (i) is true

Both (i) and (ii) are true

Both (i) and (ii) are false

**SKIP****SUBMIT ANSWER**



01 : 59 : 30



Exit

**Choose the correct option**

Q15 / 80

What does the hardwired control generator consist of?

**OPTIONS**

Condition codes

Decoder/encoder

Control step counter

All of the mentioned

**SKIP****SUBMIT ANSWER**



01 : 59 : 32



Exit

**Choose the correct option**

Q14 / 80

Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

**OPTIONS**

B

A

Both take the same time

INSUFFICIENT INFORMATION

**SKIP****SUBMIT ANSWER**



01 : 59 : 34



Exit

**Choose the correct option**

Q13 / 80

Consider a program with 50 million instructions, a machine requires 25 milliseconds to execute this program. What will be the MIPS rating of the machine?

**OPTIONS**

200

20

2000

20000

**SKIP****SUBMIT ANSWER**



01 : 59 : 35



Exit

**Choose the correct option**

Q12 / 80

CISC stands for \_\_\_\_\_

**OPTIONS**

Computer Integrated Sequential Compiler

Complete Instruction Sequential Compilation

Complex Instruction Set Computer

Complex Instruction Sequential Compilation

**SKIP****SUBMIT ANSWER**



01 : 59 : 36



Exit

**Choose the correct option**

Q11 / 80

The ultimate goal of a compiler is to \_\_\_\_\_

**OPTIONS**

Reduce the size of the object code

Reduce the clock cycles for a programming task

Be versatile

Be able to detect even the smallest of errors

**SKIP****SUBMIT ANSWER**



01 : 59 : 38



Exit

**Choose the correct option**

Q10 / 80

For a byte addressable computer which has 4 Gigabytes of memory. If each word in the computer is 64 bit. Then how many bits are needed to address a single word.

**OPTIONS**

30

29

31

32

**SKIP****SUBMIT ANSWER**



01 : 59 : 40



Exit

**Choose the correct option**

Q9 / 80

What is the largest number that can be represented using 10-bit 2's complement representation -----?

**OPTIONS**

535

215

511

239

**SKIP****SUBMIT ANSWER**



01 : 59 : 41



Exit

**Choose the correct option**

Q8 / 80

Computer has a built-in system clock that emits millions of regularly spaced electric pulses per \_\_\_\_\_ called clock cycles.

**OPTIONS**

millisecond

second

microsecond

minute

**SKIP****SUBMIT ANSWER**



01 : 59 : 43



Exit

**Choose the correct option**

Q7 / 80

Program counter is a register that

**OPTIONS**

Points to the current instruction that is being executed.

Counts the total number of instructions present in a program.

Points to the next instruction that is to be executed.

Stores the data of the current instruction that is being executed.

**SKIP****SUBMIT ANSWER**



01 : 59 : 45



Exit

**Choose the correct option**

Q6 / 80

A circuitry that processes that responds to and processes the basic instructions that are required to drive a computer system is \_\_\_\_\_

**OPTIONS**

ALU

Memory

CU

Processor

**SKIP****SUBMIT ANSWER**



01 : 59 : 49



Exit

**Choose the correct option**

Q5 / 80

Consider the instruction XOR R3, R2. If register R1 and R2 contains value 09H and 47H respectively. What will be the value R3 after executing the instruction?

**OPTIONS**

5E

4E

2E

3E

**SKIP****SUBMIT ANSWER**



01 : 59 : 51



Exit

**Choose the correct option**

Q4 / 80

Opcode indicates the operations to be performed

**OPTIONS**

true

false

**SKIP****SUBMIT ANSWER**



01 : 59 : 53



Exit

**Choose the correct option**

Q3 / 80

Which of the following addressing modes does not require any memory access for fetching the operands?

**OPTIONS**

Immediate Addressing

Direct addressing

Register Indirect

**SKIP****SUBMIT ANSWER**



01 : 59 : 55



Exit

**Choose the correct option**

Q2 / 80

The main virtue for using single Bus structure is

**OPTIONS**

Cost effective connectivity and speed

Fast data transfers

Cost effective connectivity and ease of attaching peripheral devices

None of the mentioned

**SKIP****SUBMIT ANSWER**



01 : 59 : 59



Exit

**Choose the correct option**

Q1 / 80

Radix of Hexadecimal number system is

**OPTIONS**

4

8

2

16

**SKIP****SUBMIT ANSWER**