8085 Microprocessor –

→ 8085 microprocessor is an 8-bit microprocessor designed by Intel in 1977 using NMOS (N-channel metal oxide semiconductor) technology.

→ It has following configuration –

(i) 8-bit data bus.
(ii) 16-bit address bus.
(iii) A 16-bit program counter.
(iv) A 16-bit stack pointer.
(v) Six 8-bit registers arranged in pairs – BC, DE, HL.
(vi) Requires +5V supply to operate at 3.2 MHZ single phase clock.

Pin Diagram -

Left Pins		Right Pins	
X₁	1	40	Vcc
X₂	2	39	HOLD
RESET OUT	3	38	HLDA
SOD	4	37	CLK (OUT)
SID	5	36	RESET IN'
TRAP	6	35	READY
RST 7.5	7	34	IO/M'
RST 6.5	8	33	S₁
RST 5.5	9	32	RD'
INTR	10	31	WR'
INTA'	11	30	ALE
AD₀	12	29	S₀
AD₁	13	28	A₁₅
AD₂	14	27	A₁₄
AD₃	15	26	A₁₃
AD₄	16	25	A₁₂
AD₅	17	24	A₁₁
AD₆	18	23	A₁₀
AD₇	19	22	A₉
Vss	20	21	A₈

8085 A

$A_0 - A_{15}$ are address bus. They are unidirectional.

ALE stands for Address latch Enable Signal. It enables the lower 8-bits of the address.

IO/M signals are input/output or

memory signals.

Block Diagram —

D_0 — $\overline{MEMR}$
D_0 — $\overline{MEMW}$
D_0 — $\overline{IOR}$
D_0 — $\overline{IOW}$

Read Write Memory

A_{15}

A_8

ALE

AD_7

AD_0

$\overline{IO/M}$
$\overline{RD}$
$\overline{WR}$

Microprocessor

Data 30H

0
1
1
0
1
0

$\overline{MEMR}$
$\overline{MEMW}$

A_7
Address
A_0

75H

D_7

$1 \to 0$

A_7

A_0

MUX

to 30H Memory

D_0

75H
↓
Data

INTR INTA RST 5.5 RST 6.5
Interrupt Control   Serial I/O Control
                SID SOD
        TRAP RST 7.5

Accumulator   Temp. Reg.   Multiplexer
   (8)   (8)   Temp Reg   Temp Reg
                              B   C
              Flag   Reg   Reg
              Flip Flop   D   E
                    (5)   Reg   Reg
                         Instruction   H   L
                         Register   Reg   Reg
                                        Stack Pointer
              ALU   Instruction   Program Counter
              (8)   Decoder
                        and   Increment/Decrement
                        Machine   Address Latch
                        Cycle
                        Encoding

                                     Register
                                     Array

Power   Address   Data/Address
Supply   +5V   Buffer   Buffer
          GND

X₁   CLK Timing And Control
X₂   GEN Control Status DMA Reset
CLK   RD WR ALE S S HOLD Reset   A₁₅-A₈   AD₇-AD₀
OUT READY   Address Bus Address/Data
             IO/M HLDA Reset Out   Bus