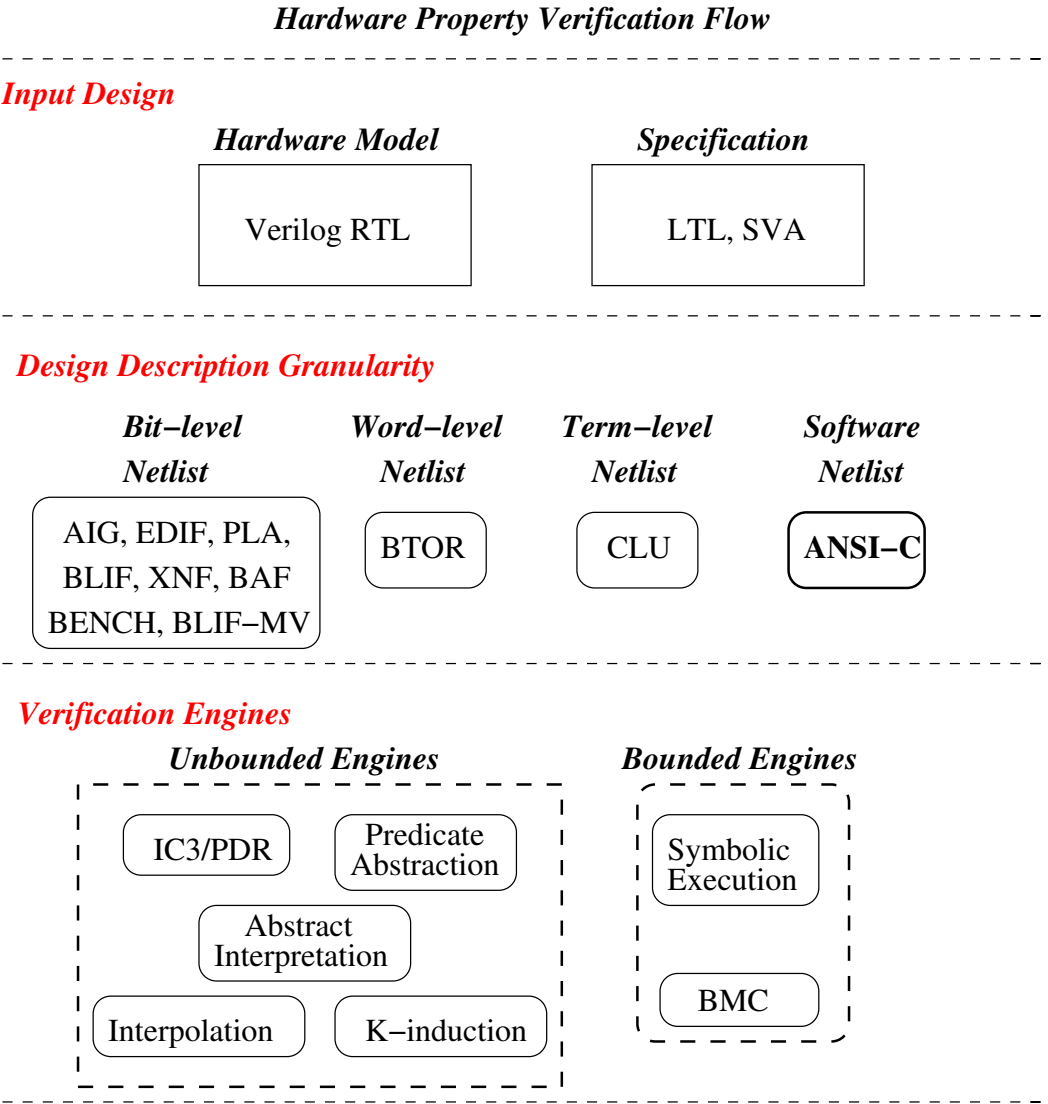
Hardware Property Verification Flow
Input Design
Hardware Model
Verilog RTL
Specification
LTL, SVA
Design Description Granularity
Bit−level Netlist
AIG, EDIF, PLA, BLIF, XNF, BAF BENCH, BLIF−MV
Word−level Netlist
BTOR
Term−level Netlist
CLU
Software Netlist
ANSI−C
Verification Engines
Unbounded Engines
IC3/PDR
Predicate Abstraction
Abstract Interpretation
Interpolation
K−induction
Bounded Engines
Symbolic Execution
BMC