UNIT 4
Analog and Digital Electronics

Sequential Circuit

Synchronous Counter

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The procedure to design a synchronous counter is listed here.

- Obtain the truth table of the logic sequence for intended counter to be designed. Alternatively obtain the state diagram of the counter.
- Determine the number and type of flip-flop to be used.
- From the excitation table of the flip-flop, determine the next state logic.
- From the output state, use Karnaugh map for simplification to derive the circuit output functions and the flip-flop output functions.
- Draw the logic circuit diagram.

Excitation Table of FFs

Q_t	Q_{t+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q_t	Q_{t+1}	**D**
0	0	0
0	1	1
1	0	0
1	1	1

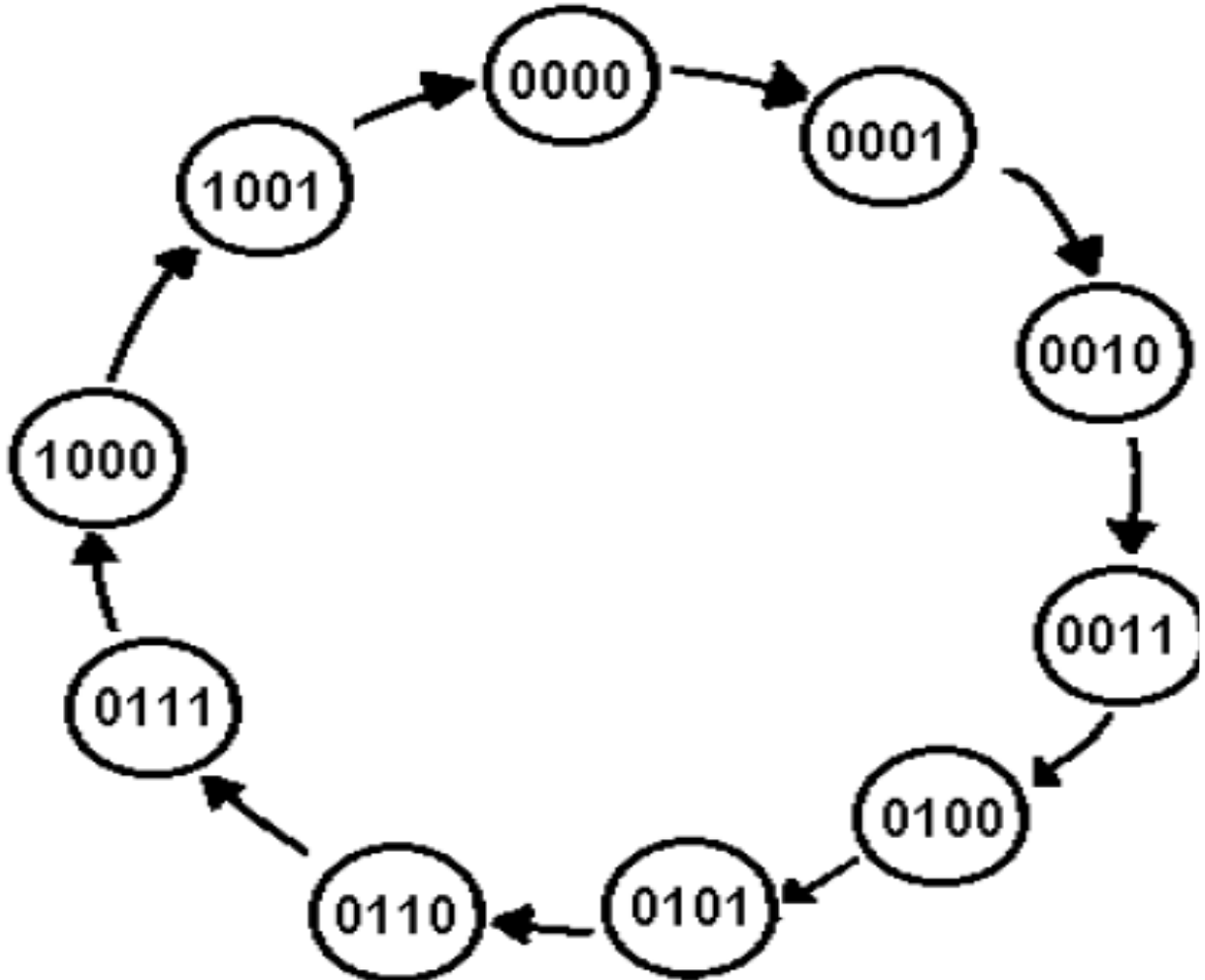
Figure 9.7: Characteristic table of SR and D flip-flop

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_t	Q_{t+1}	**T**
0	0	0
0	1	1
1	0	1
1	1	0

Synchronous Decade Counter Using JK Flip-Flop

State Diagram

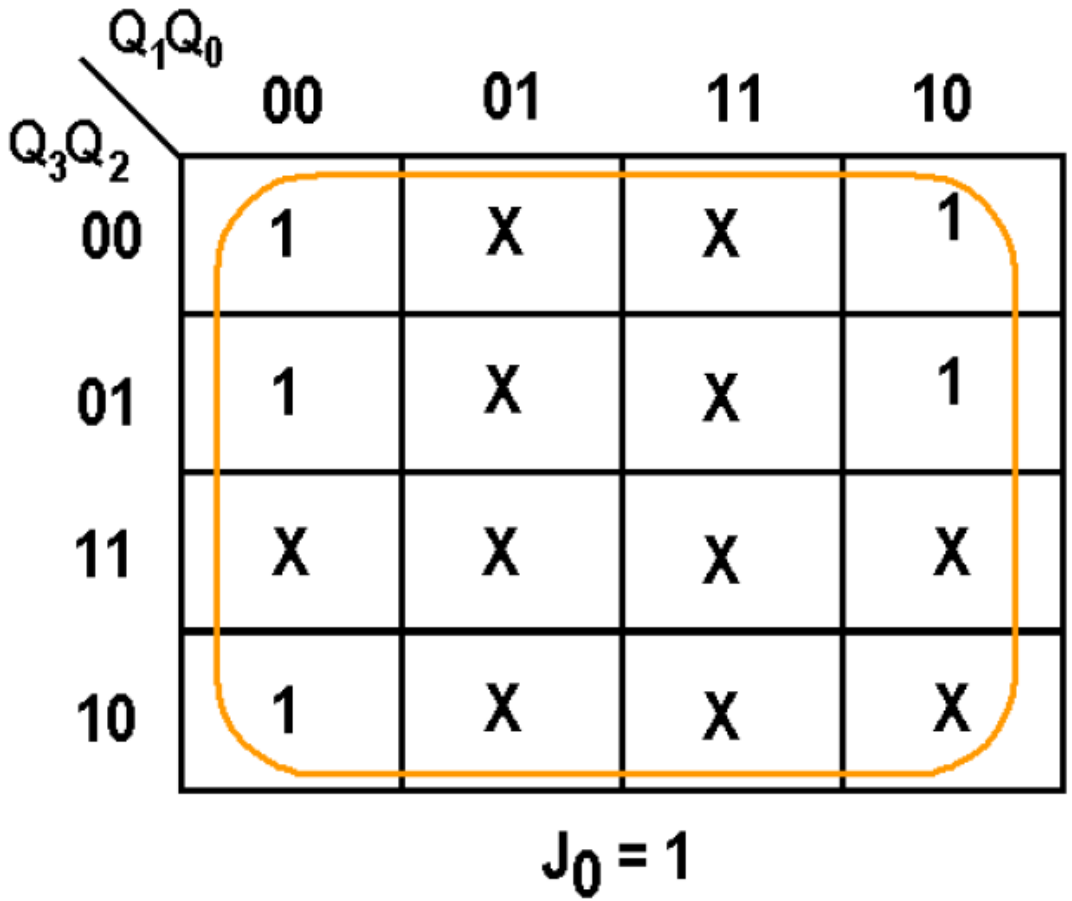


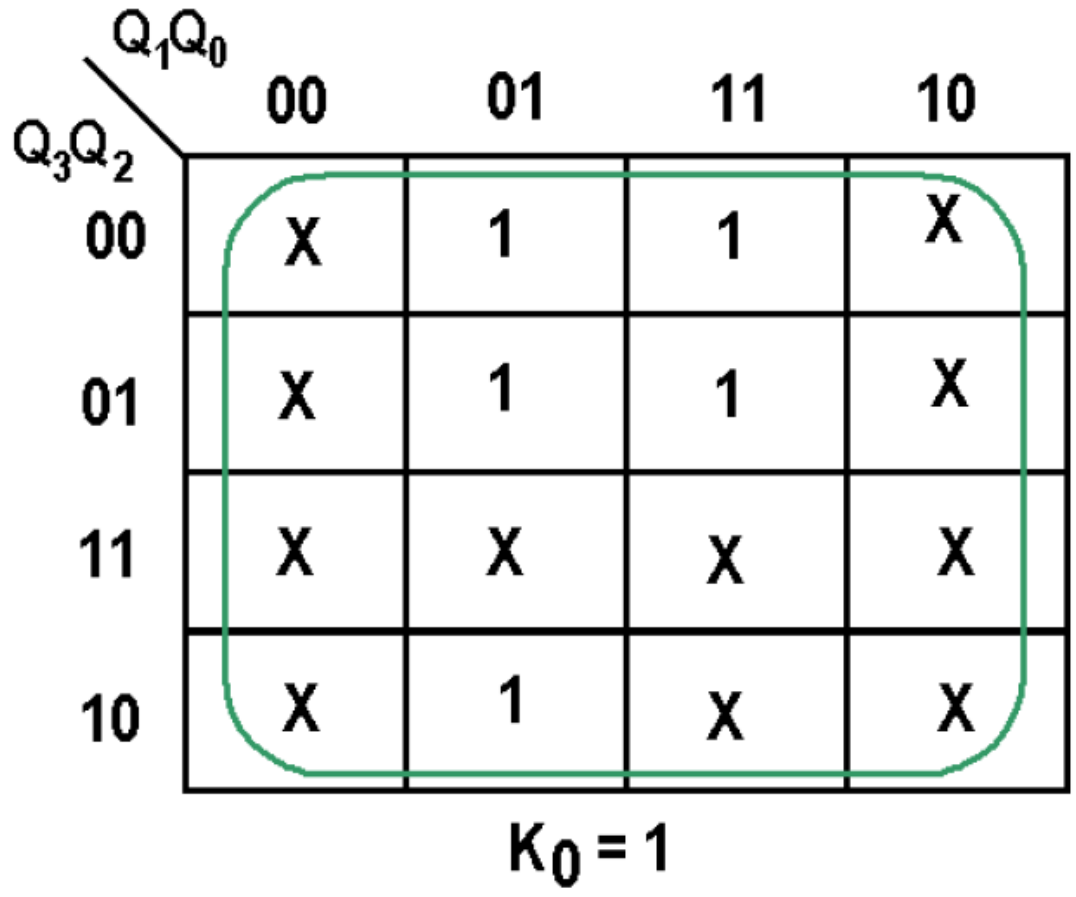
Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Truth Table

Present State				Next State				Output							
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

K map for J0 & K0





Q_3Q_2 \ Q_1Q_0	00	01	11	10
00		1	X	X
01		1	X	X
11	X	X	X	X
10			X	X

$J_1 = \overline{Q}_3 Q_0$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	1	
01	X	X	1	
11	X	X	X	X
10	X	X	X	X

$K_1 = \overline{Q}_3 Q_0$

Figure 9.12: Karnaugh maps of J_1 and K_1

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00			1	
01	X	X	X	X
11	X	X	X	X
10			X	X

$J_2 = Q_1 Q_0$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	X	X
01			1	
11	X	X	X	X
10			X	X

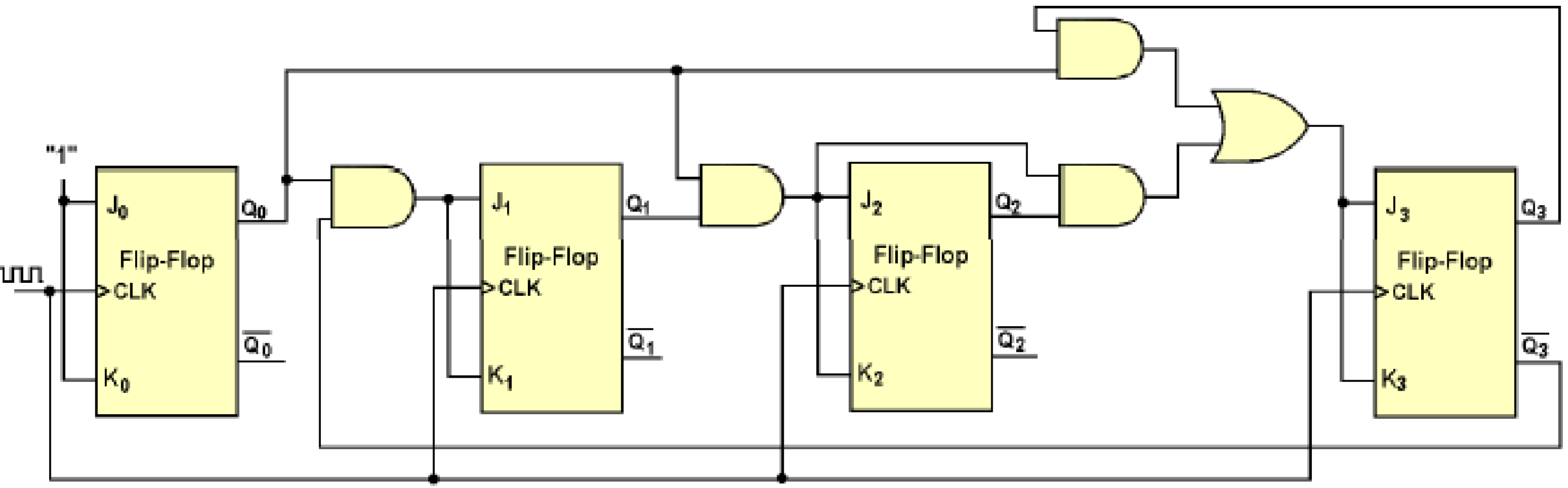
$K_2 = Q_1 Q_0$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00				
01			1	
11	X	X	X	X
10	X	X	X	X

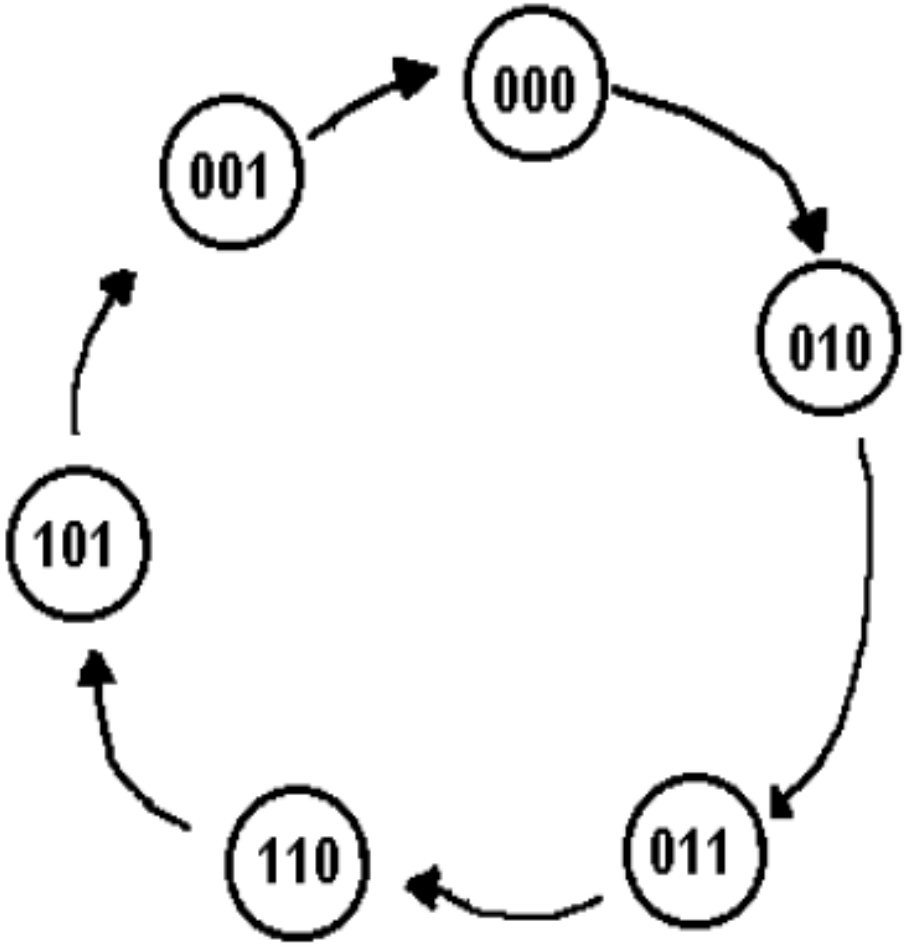
$$J_3 = Q_3 Q_0 + Q_2 Q_1 Q_0$$

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10		1	X	X

$$K_3 = Q_3 Q_0 + Q_2 Q_1 Q_0$$



Design of a Synchronous Modulus-Six Counter Using SR Flip-Flop



Q_t	Q_{t+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

[Present State			Next State			Output					
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	R_2	S_2	R_1	S_1	R_0	S_0
0	0	0	0	1	0	0	X	1	0	0	X
0	1	0	0	1	1	0	X	X	0	1	0
0	1	1	1	1	0	1	0	X	0	0	1
1	1	0	1	0	1	X	0	0	1	1	0
1	0	1	0	0	1	0	1	0	X	X	0
0	0	1	0	0	0	0	X	0	X	0	1

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	0	1
1	X	X	X	1

$R_0 = Q_1 \cdot \overline{Q_0}$

Q_2 \ Q_1Q_0	00	01	11	10
0	X	1	1	0
1	X	0	X	0

$S_0 = \overline{Q_2} \cdot Q_0$

Figure 9.19: Karnaugh maps of R_0 and S_0

Q_2 \ Q_1Q_0	00	01	11	10
0	1	0	X	X
1	X	0	X	0

$R_1 = \overline{Q_1} \cdot \overline{Q_0}$

Q_2 \ Q_1Q_0	00	01	11	10
0	0	X	0	0
1	X	X	X	1

$S_1 = Q_2$

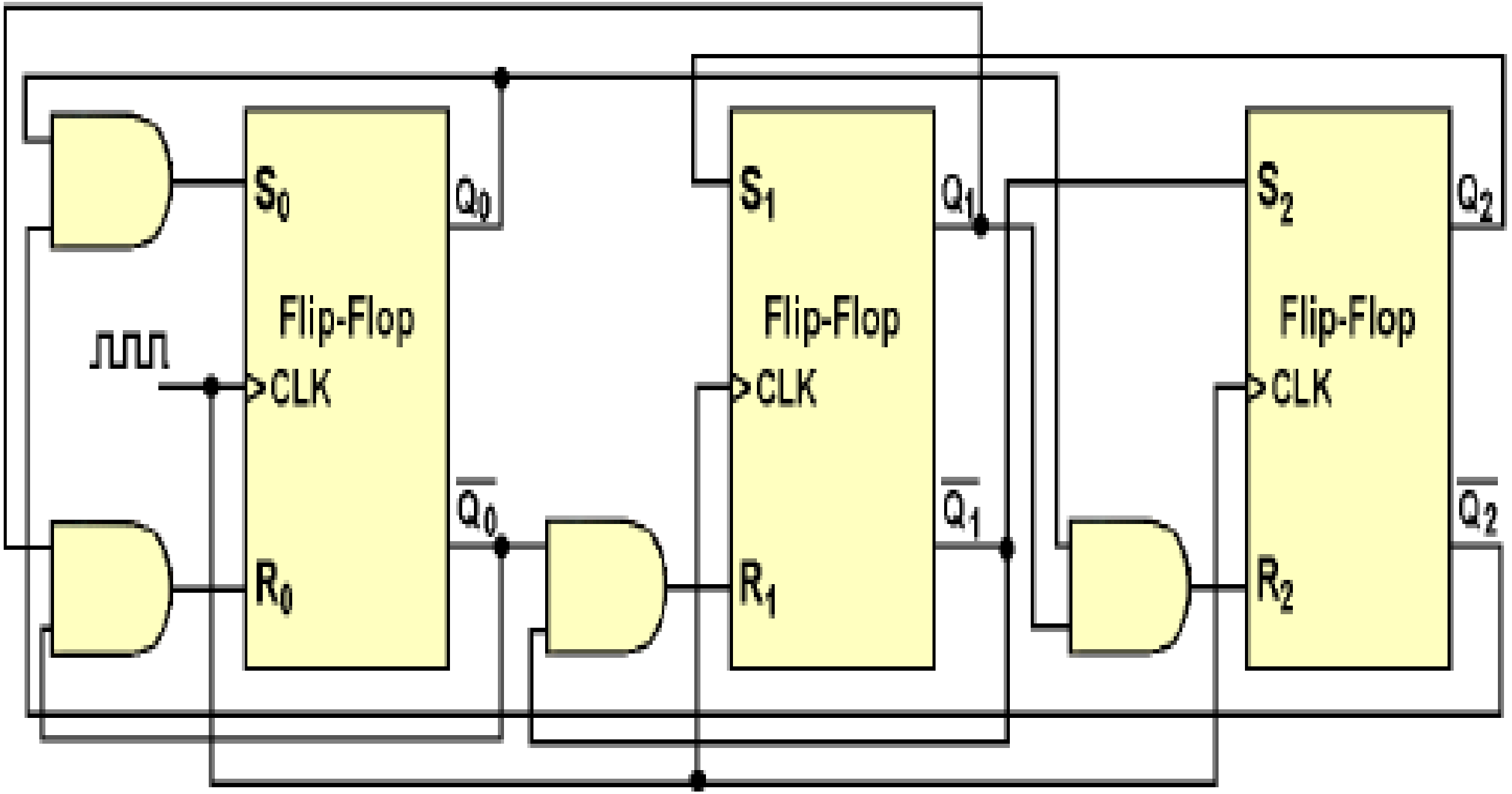
Figure 9.20: Karnaugh maps of R_1 and S_1

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	1	0
1	X	0	X	X

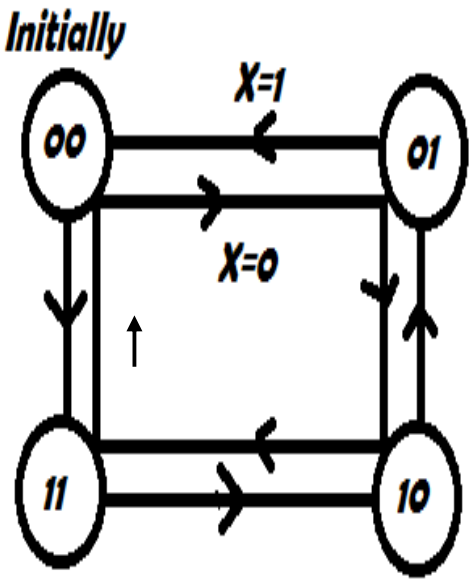
$R_2 = Q_1 \cdot Q_0$

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	0	X
1	X	1	X	0

$S_2 = \overline{Q_1}$


S0
Q0
Flip-Flop
CLK
Q̄0
R0
S1
Q1
Flip-Flop
CLK
Q̄1
R1
S2
Q2
Flip-Flop
CLK
Q̄2
R2

Binary Up-Down Counters using D FF



If control input
X=0 counter act as
UP Counter

If the control input
X=1 counter act as
Down counter

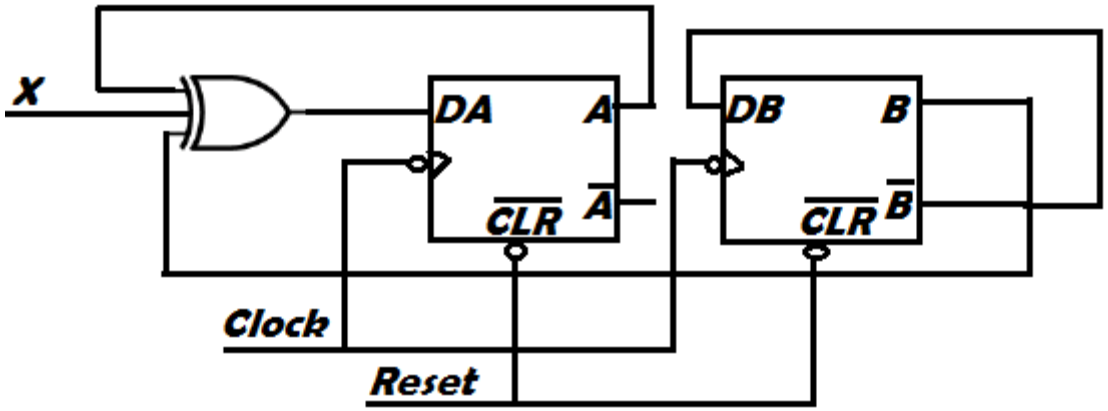
X	A	B	An+1	Bn+1	DA	DB
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

Q_t	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

D_B

X \ AB	00	01	11	10
0	1	0	0	1
1	1	0	0	1

$D_B = \overline{B}$



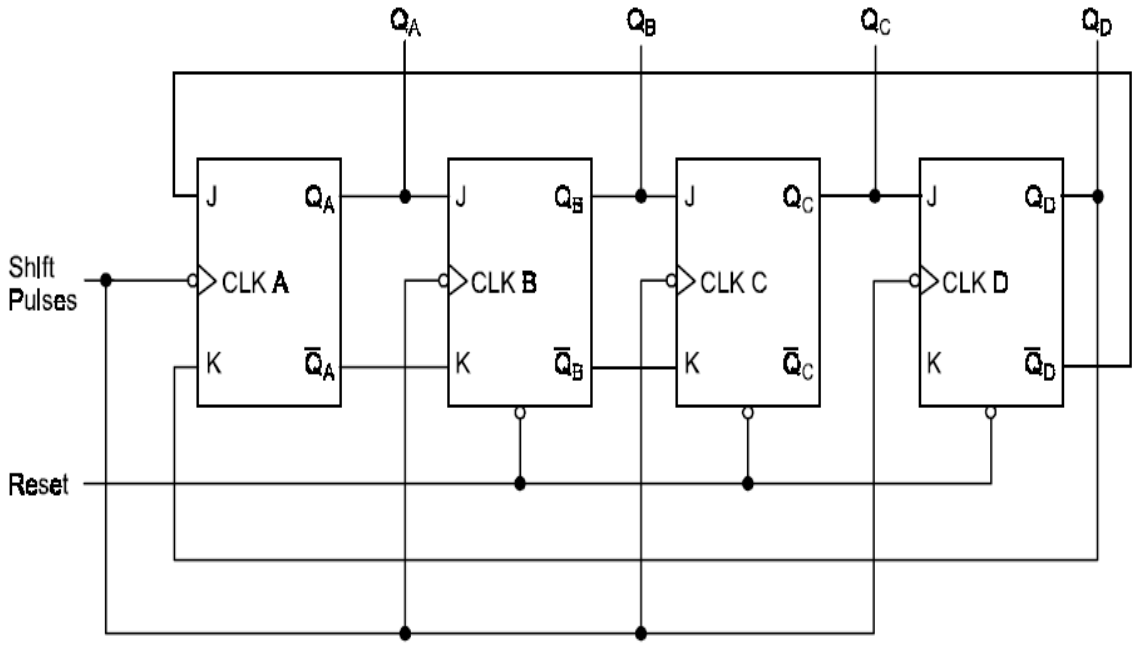
D_A

X \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$D_A = \overline{X}(\overline{A}B + A\overline{B}) + X(\overline{A}\overline{B} + AB)$

$= X \oplus A \oplus B$

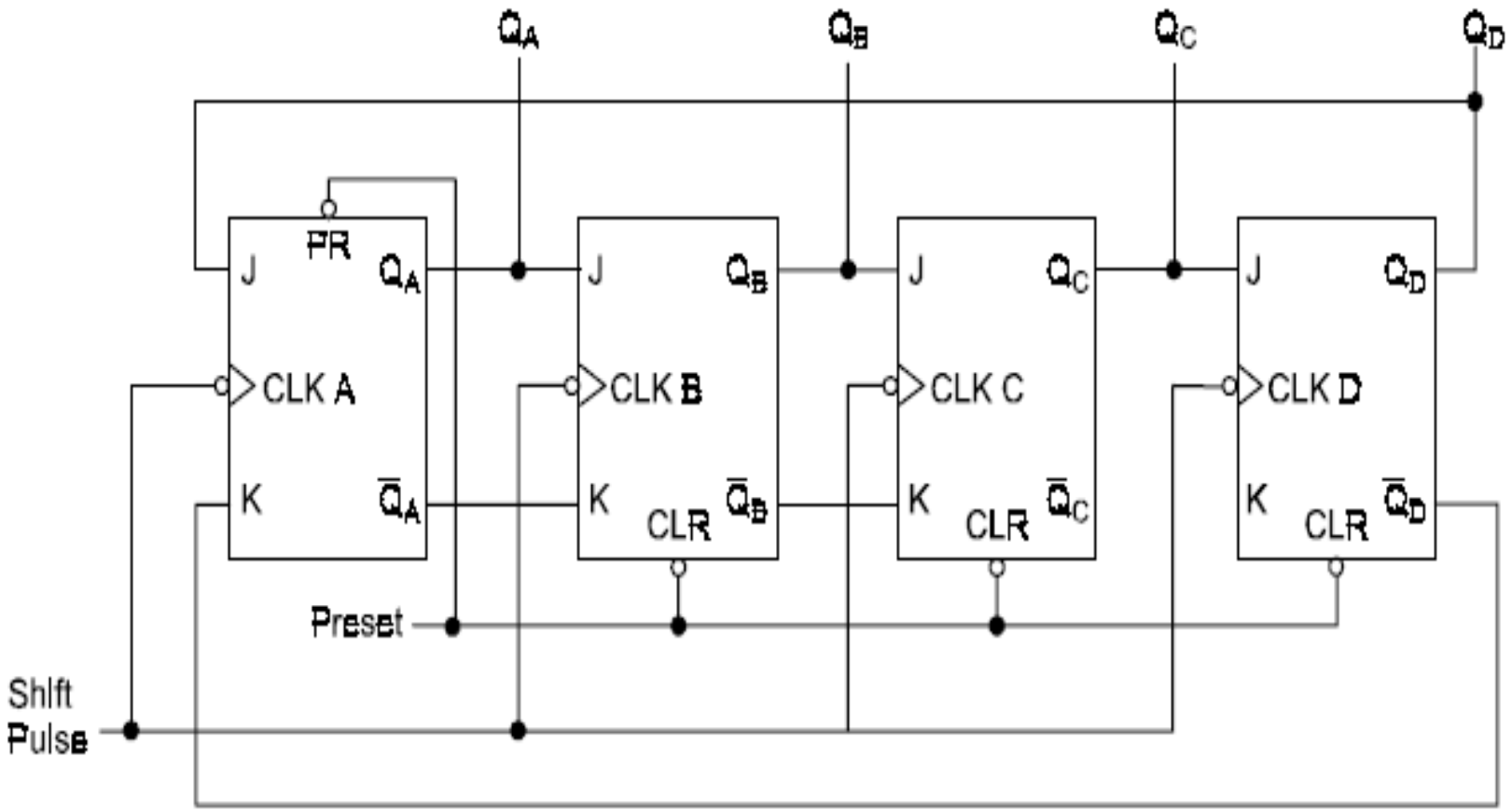
Johnson counter



State	Q_D	Q_C	Q_B	Q_A	*Binary equivalent*	*Output decoding*
1	0	0	0	0	0	$\bar{A}\bar{D}$
2	0	0	0	1	1	$A\bar{B}$
3	0	0	1	1	3	$B\bar{C}$
4	0	1	1	1	7	$C\bar{D}$
5	1	1	1	1	15	AD
6	1	1	1	0	14	$\bar{A}B$
7	1	1	0	0	12	$\bar{B}C$
8	1	0	0	0	8	$\bar{C}D$

Ring counter

Pre-set used to insert 1 in FF A at the same time all the FF reset to 0 then simply act shift register at each clock edge.



States	Counter output			
	Q_A	Q_B	Q_C	Q_D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0

UNIT 4 END