

ADE- UNIT IV

Combination Circuits

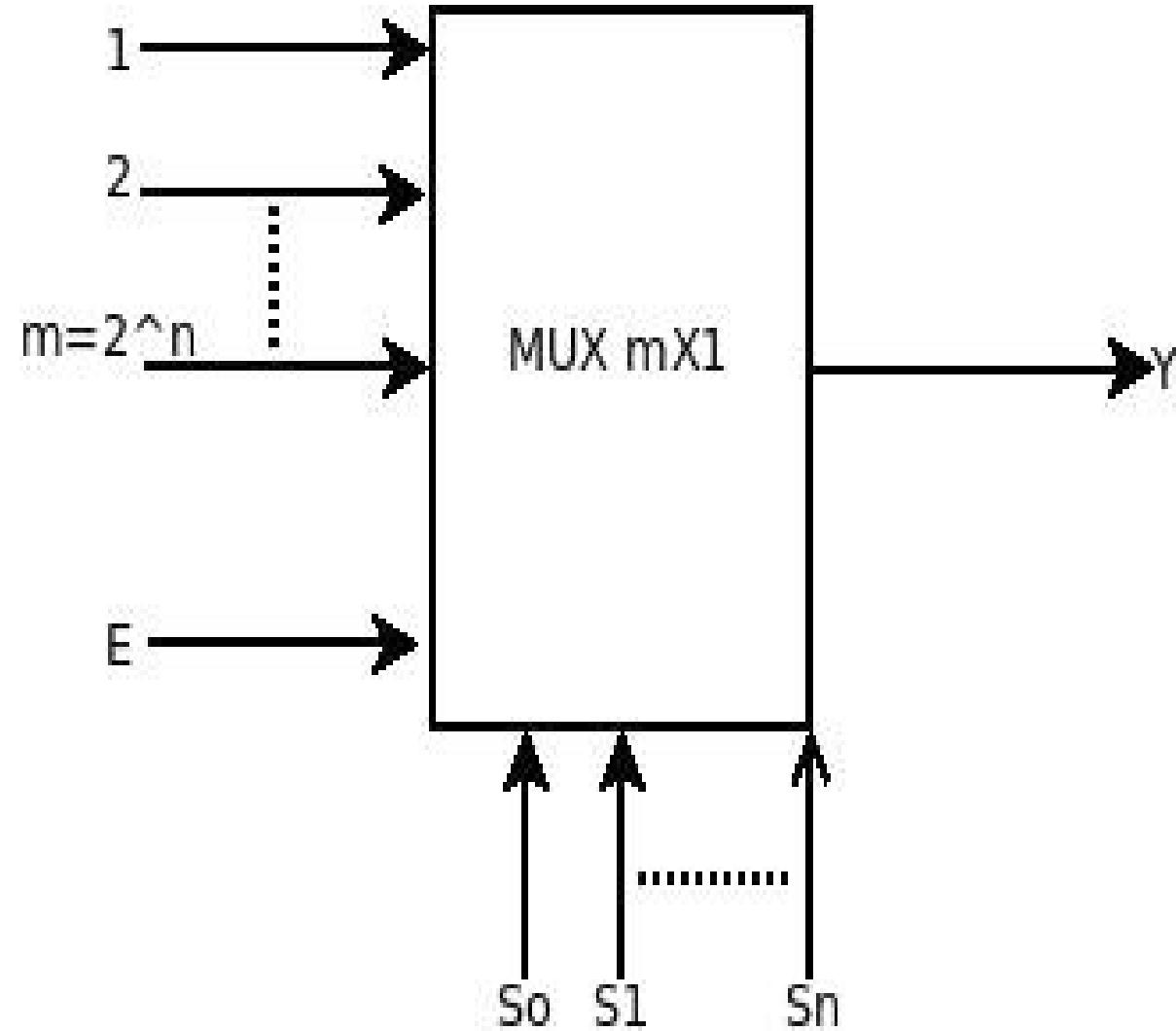
Topics

1. Multiplexer
2. Demultiplexer
3. Encoder
4. Decoder

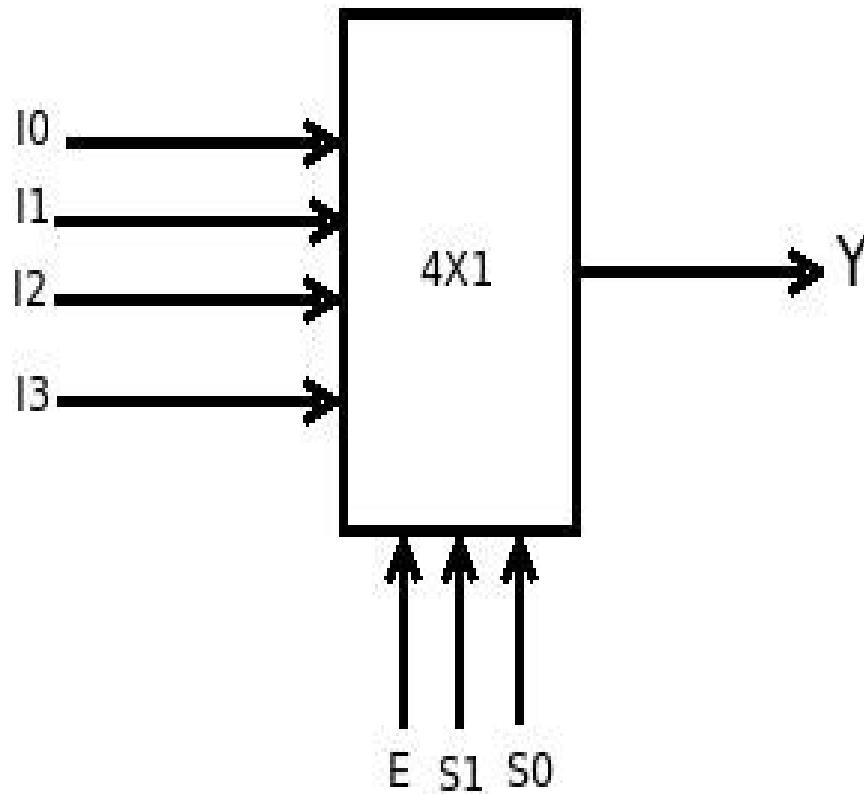
Intoduction and implementation ,Tree &
Logical circuit implementation

Multiplexer

- Electronic device consist of
- 2^m input terminals
- One output output terminals
- M numbers of selection line



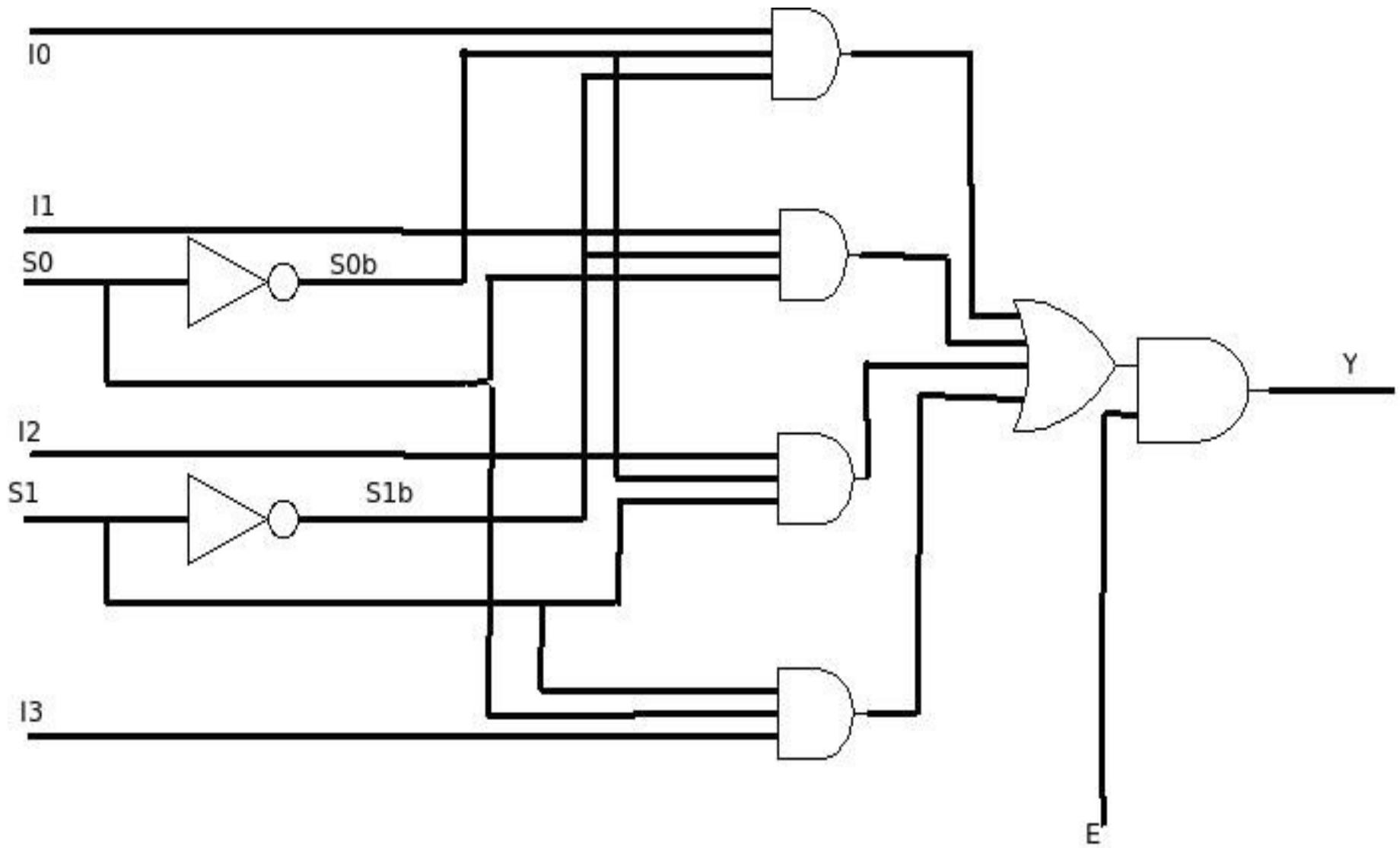
MUX 4X1



E	S1	S0	Y
1	0	0	I0
1	0	1	I1
1	1	0	I2
1	1	1	I3
0	X	X	0

$$Y = E(S1b S0b I0 + S1b S0 I1 + S1 S0b I2 + S0 S1 I3)$$

Logical Implementation



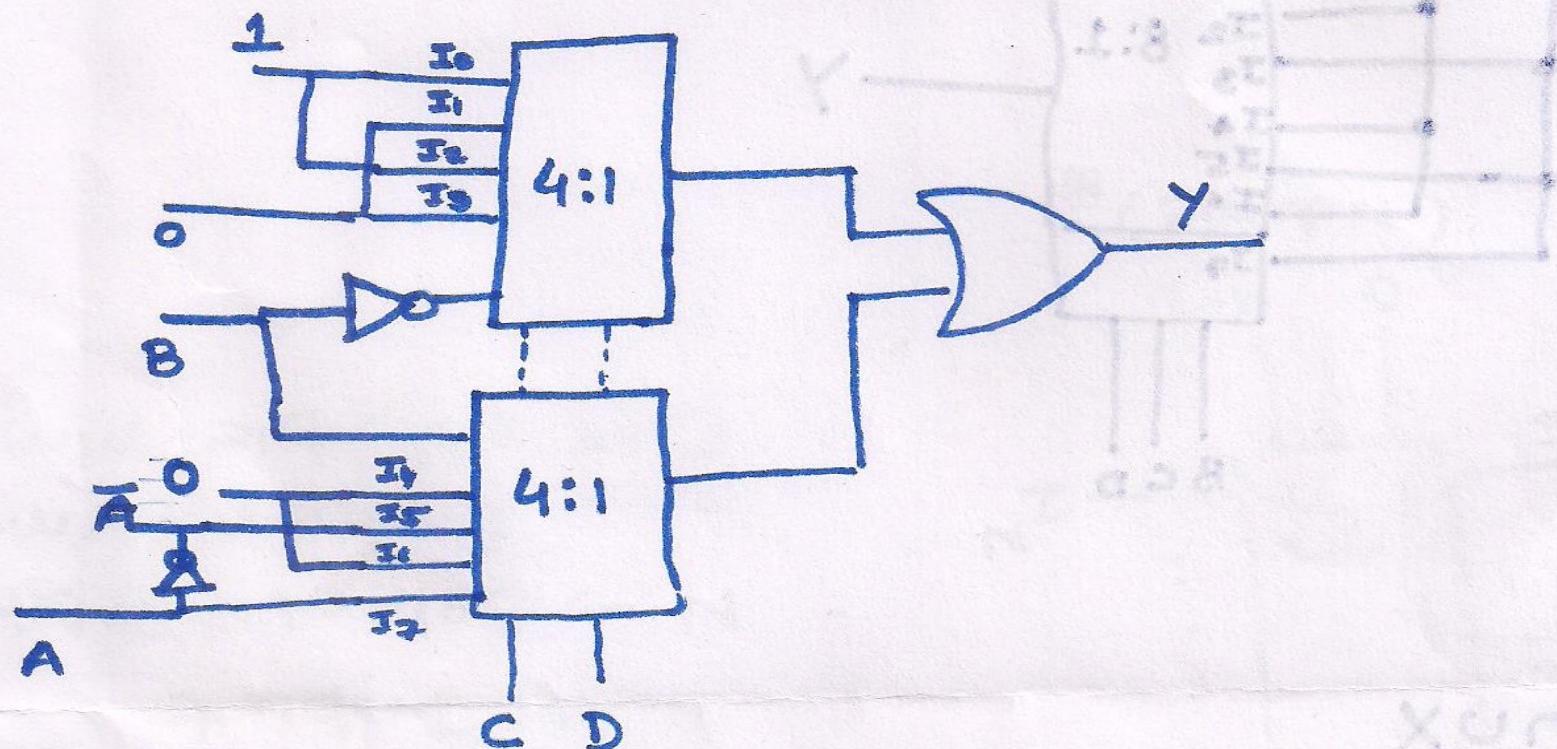
①

Implement the function using 4:1 mux

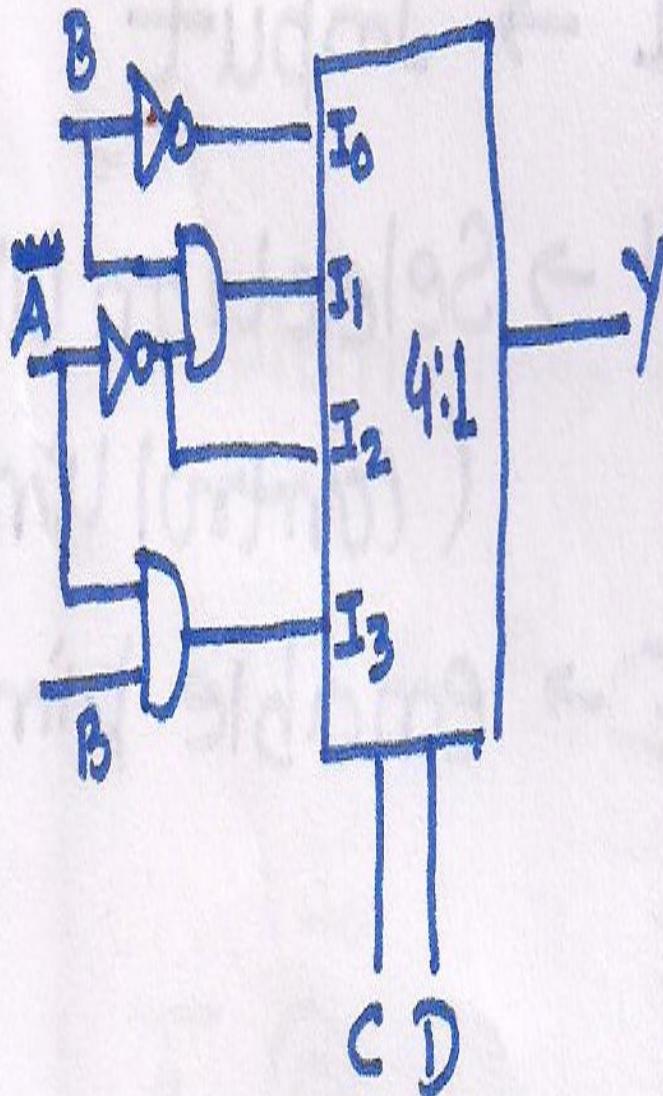
$$F(A, B, C, D) = \sum(0, 2, 5, 8, 10, 15)$$

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	
\bar{A}	0	1	2	3	4	5	6	7	
A	8	9	10	11	12	13	14	15	

1	0	1	0	0	\bar{A}	0	A	
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② 2nd way

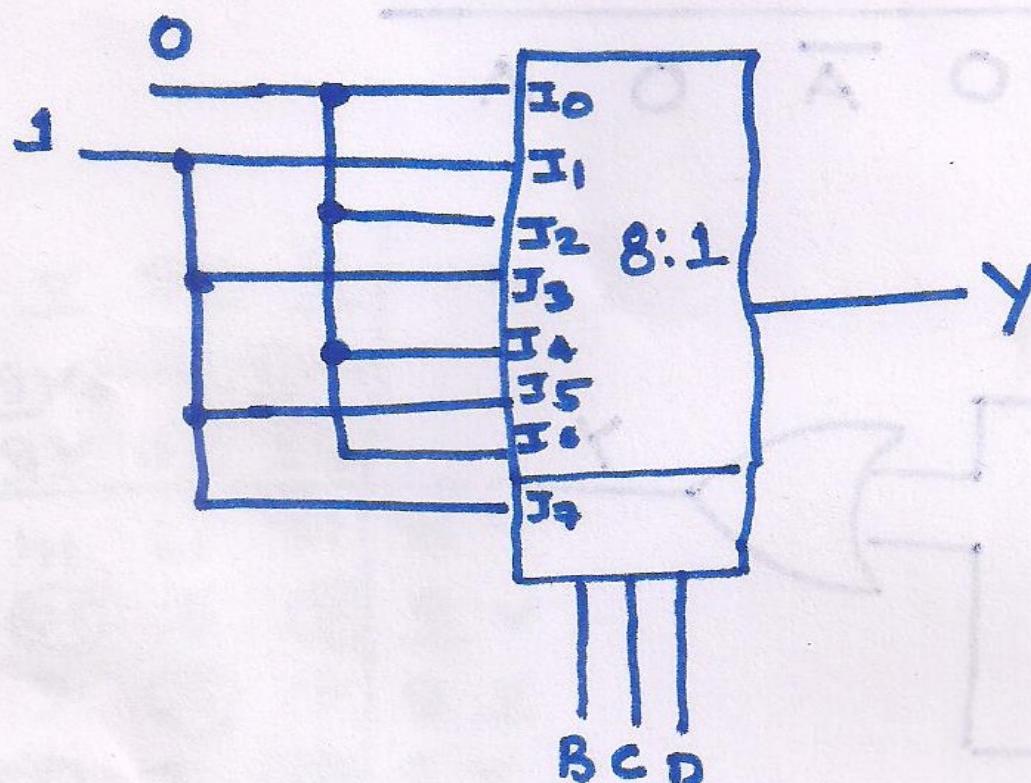


$\bar{A} \bar{B}$	0	1	2	3
$\bar{A} B$	4	5	6	7
$A \bar{B}$	8	9	10	11
$A B$	12	13	14	15
$\bar{B} \bar{A}$	$\bar{A} B$	$\bar{A} \bar{B}$	$A B$	
$+ A \bar{B}$		$+ A \bar{B}$		
$= \bar{B}$	$\bar{A} B$	\bar{A}	$A B$	

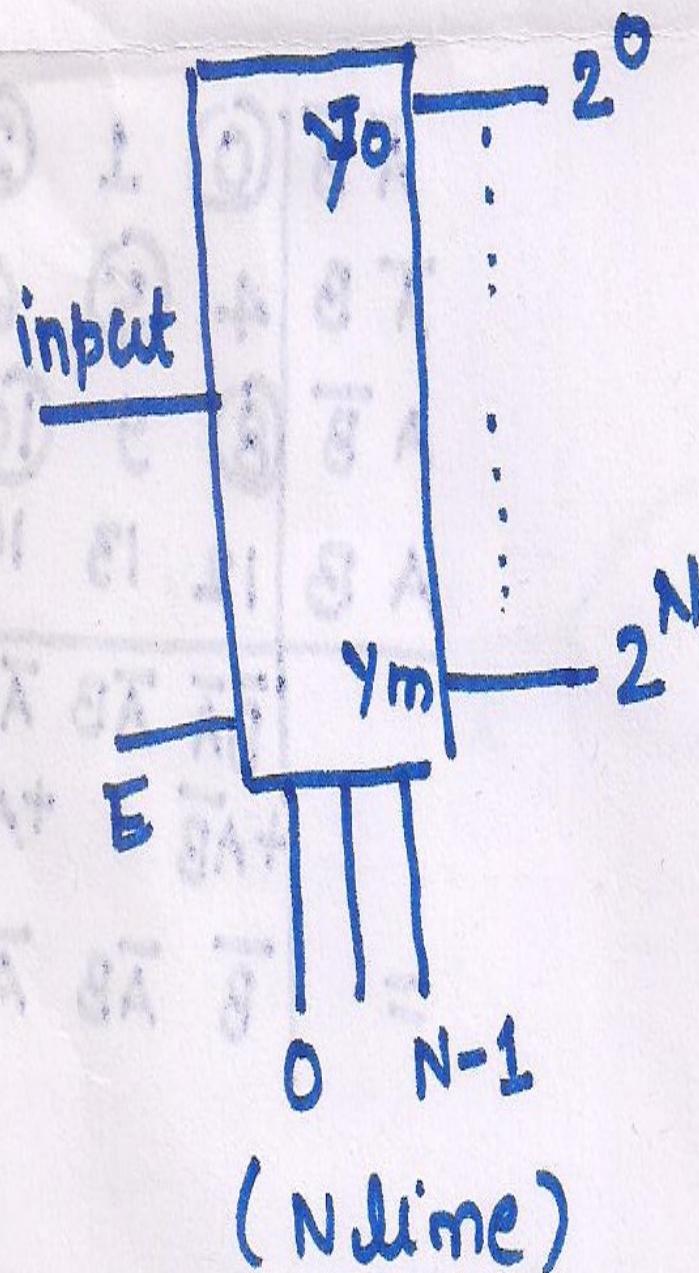
③

6 $\pi(0, 2, 4, 6, 8, 10, 12, 14)$ (8:1) ^{max}

	I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇
A	0	①	2	③	4	⑤	6	⑦
A	8	⑨	10	⑪	12	⑬	14	⑮

| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |


③ DEMUX



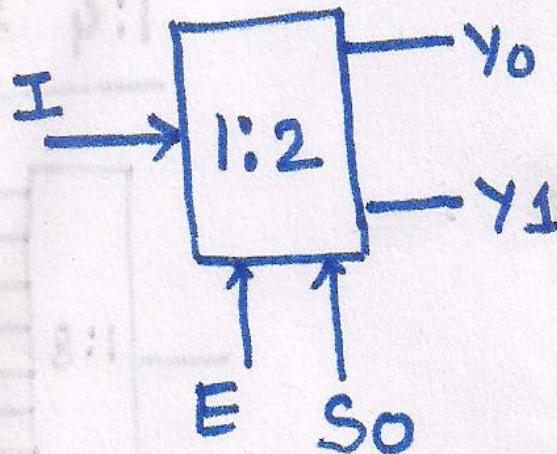
$2^N \rightarrow$ output

1 → Input

N → Selection Line
(control line)

E → enable pin

1:2 Demux



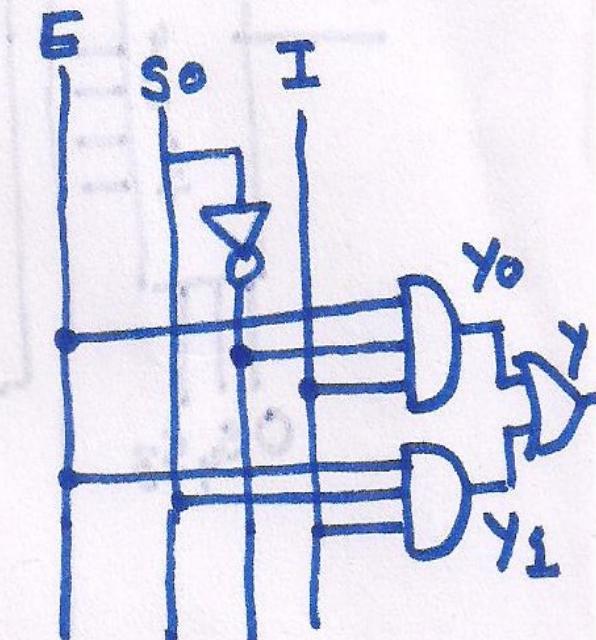
E	I	S_0	Y_1	Y_0
0	X	X	0	0
1	0	0	0	0
1	1	0	0	1
1	0	1	0	0
1	1	1	1	0

S_0	I	0	1
0	0	0	1
1	1		

$Y_0 = \bar{S}_0 I$

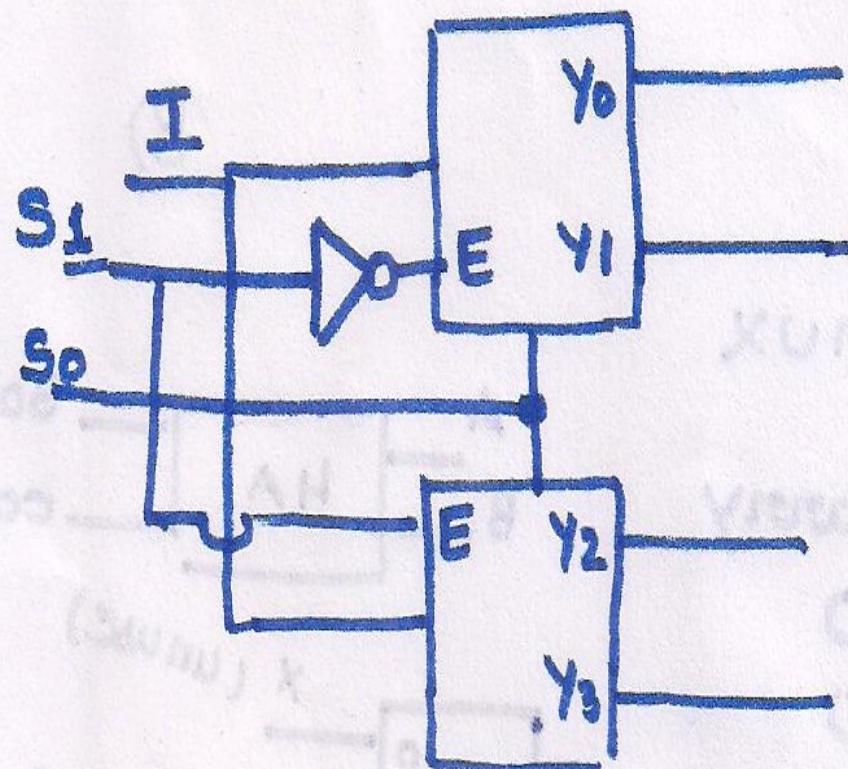
S_0	I	0	1
0	0	0	1
1	1		

$Y_1 = S_0 I$



DEMUX TREE

1:4 using 1:2

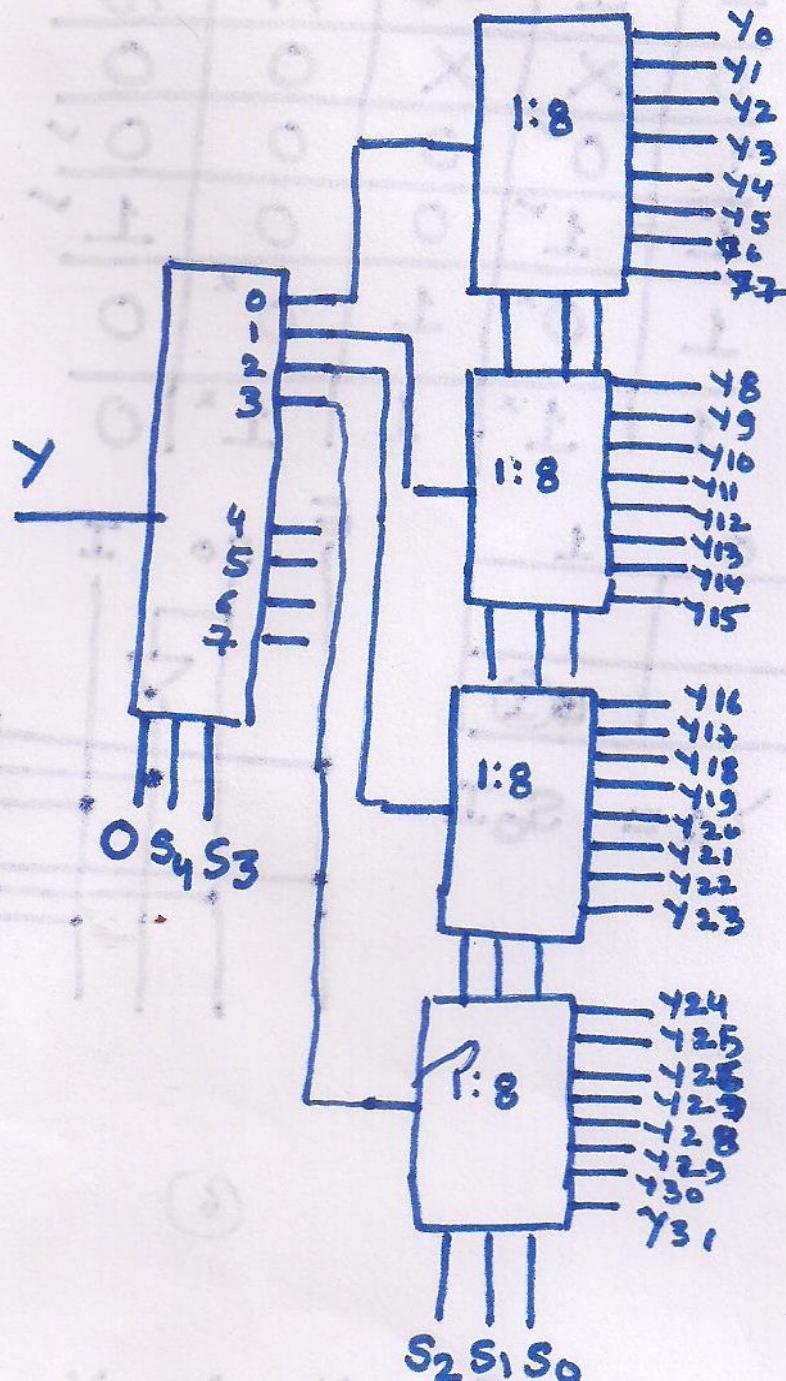


S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

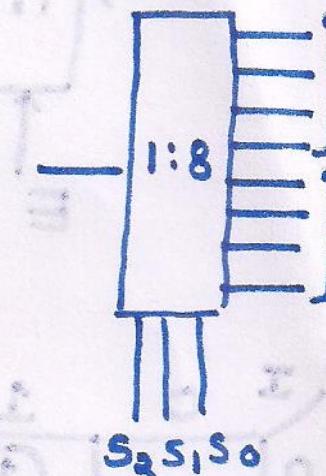
a:- Implement 1:8 using 1:4

Q:- 1:32 Using 1:8

(7)



1:4 from 1:8



$S_2 \ S_1 \ S_0$	$Y_7 \ Y_6 \ Y_5 \ Y_4 \ Y_3 \ Y_2 \ Y_1 \ Y_0$
0 0 0	0 0 0 0 0 0 0 1
0 0 1	0 0 0 0 0 0 0 0
0 1 0	0 0 0 0 0 0 1 0
0 1 1	0 0 0 0 0 1 0 0
1 0 0	0 0 0 0 1 0 0 0
1 0 1	0 0 0 1 0 0 0 0
1 1 0	0 0 1 0 0 0 0 0

Q:- compare mux & DEMUX

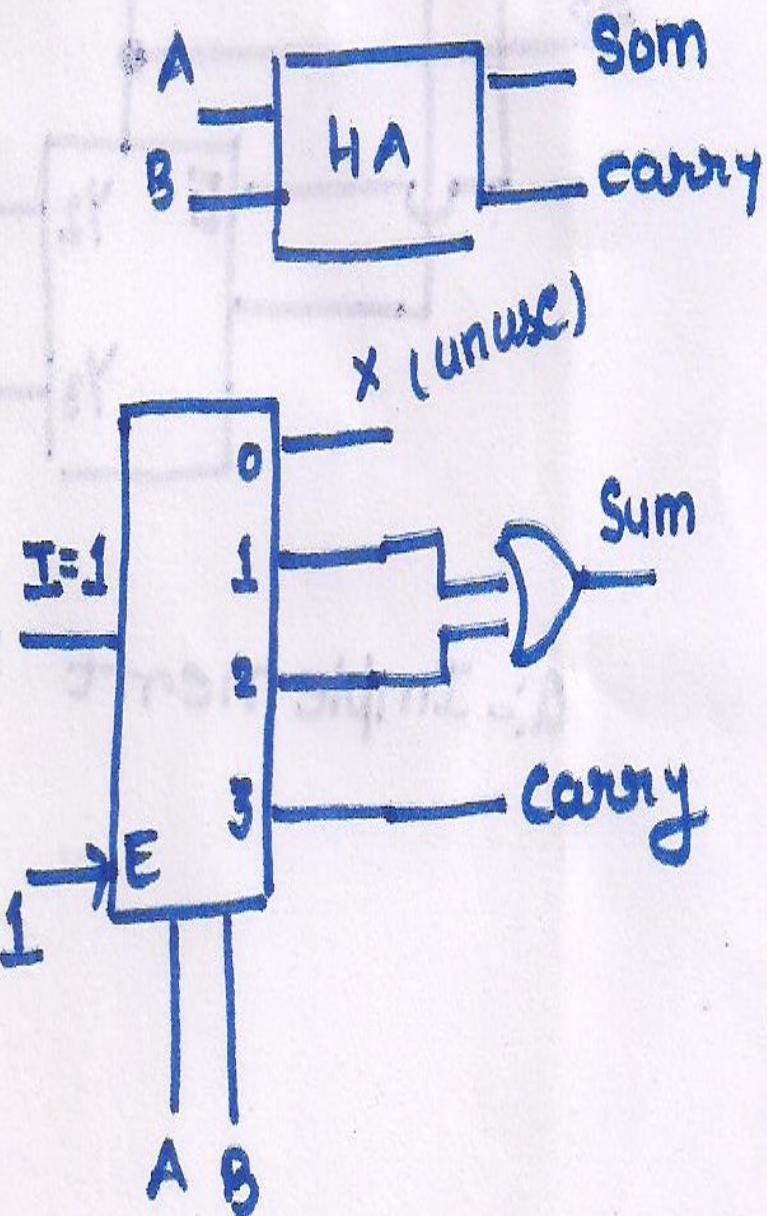
Half adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\text{Sum} = \sum (1, 2)$$

$$\text{Carry} = \sum (3)$$

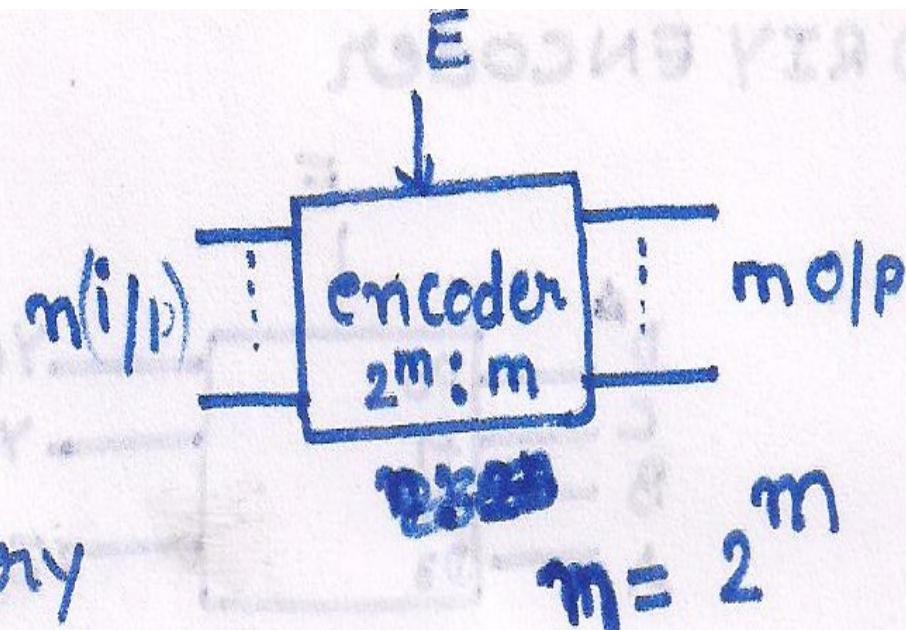
DO same with mux



ENCODERS

m input

m output



1. Octal to binary

2. Decimal to BCD

3. Hexadecimal-to-binary

4. Priority encoder

1. $2^3 = 8$ (octal) (D_0, D_1, \dots, D_7)

3 bit binary (B_2, B_1, B_0)

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	B_2	B_1	B_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$$B_2 = D_4 + D_5 + D_6 + D_7$$

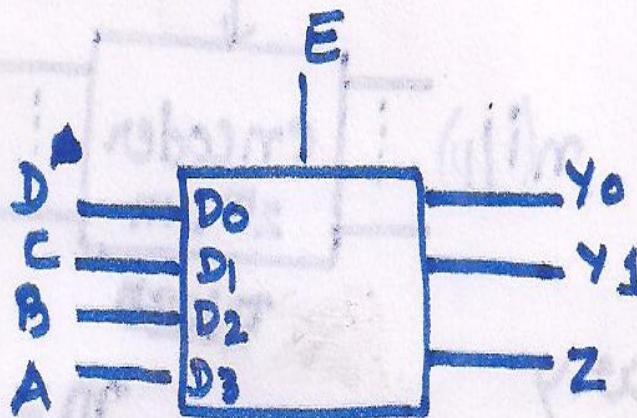
$$B_1 = D_2 + D_3 + D_6 + D_7$$

$$B_0 = D_1 + D_3 + D_5 + D_7$$

PRIORITY ENCODER

ENCODE

③



Let $A > B > C > D$

$Y_1 Y_0$	$Y_1 Y_0$	$Y_1 Y_0$	$Y_1 Y_0$
11	10	01	00
0000	\times	\times	$Z = 1$

no choice are available

A B C D | $Y_1 Y_0$
0 0 0 0 | 0 0 1 0 0 0

if only D is available

0 0 1 0 | 0 1

only C available

0 1 1 0

??

B & C available

$B > C \Rightarrow 0 1 1 0 | 1 0$

(4)

A	B	C	D:	y_1	y_0	Z
0	0	0	0	X	X	1
0	0	0	1	0	0	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	1	0	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	1	1	0
1	0	0	1	1	1	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	1	1	0
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	0

no choice available

⇒

A	B	C	D	y_1	y_0	Z
0	0	0	0	X	X	1
0	0	0	1	0	0	0
0	0	1	X	0	1	0
0	1	X	X	1	0	0
1	X	X	X	1	1	0

5

			y_1		
AB	CD	00	01	11	10
00	X	0	0	0	0
01	1	1	1	1	1
11	1	1	1	1	1
10	1	1	1	1	1

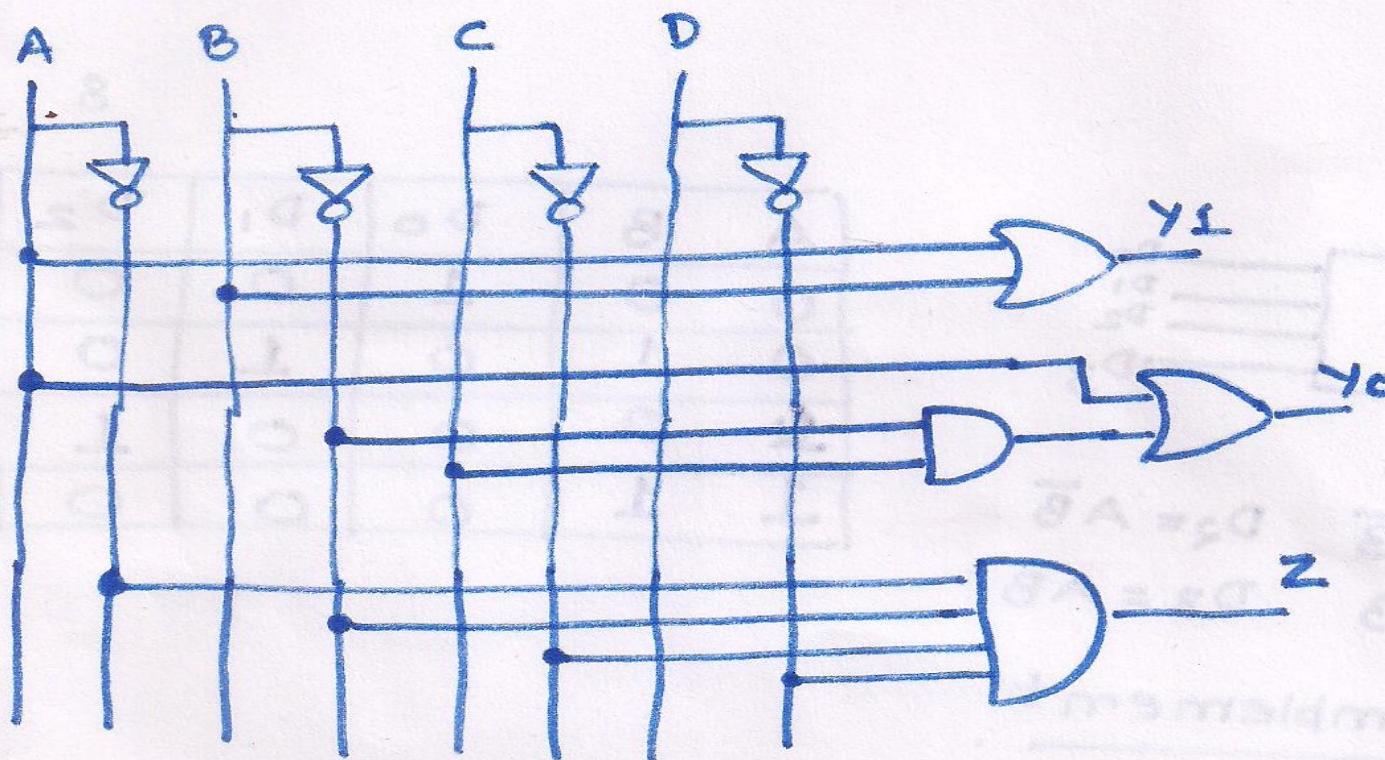
5

		y_0			
AB	CD	00	01	11	10
00	X				
01	0	0	0	0	0
11	1	1	1	1	1
10	1	1	1	1	1

$$y_1 = A + B$$

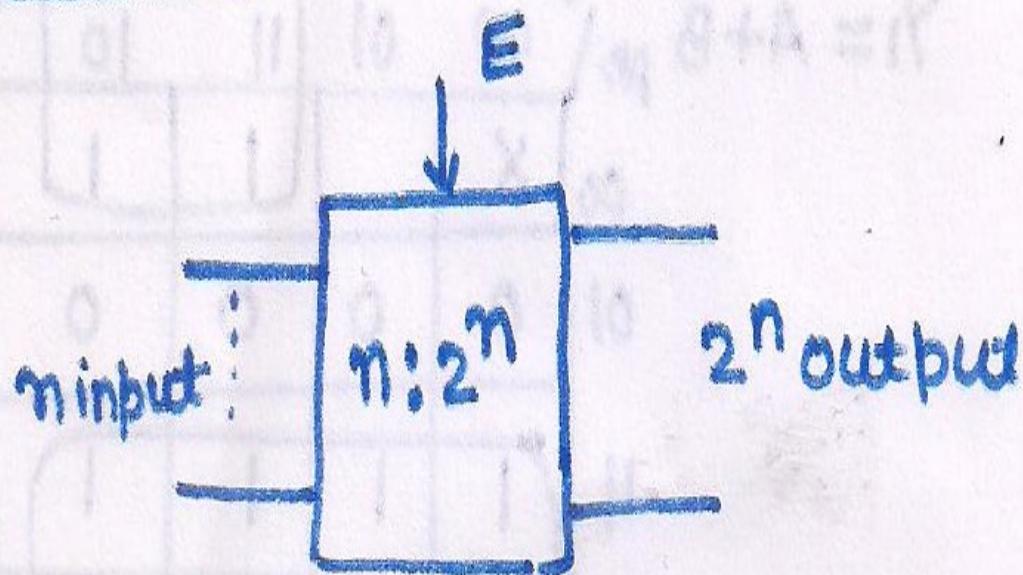
$$y_0 = A + \overline{B}C$$

$$z = \overline{A}\overline{B}\overline{C}\overline{D}$$



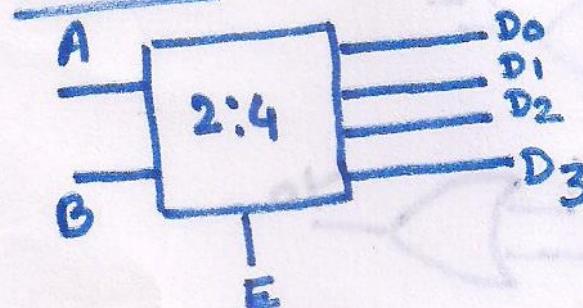
DECODER

7



1. code converters
2. BCD to 7 Segment

1.

2: 4

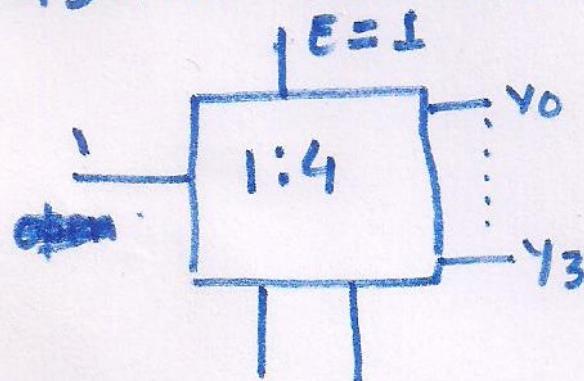
$$D_0 = \bar{A}\bar{B} \quad D_2 = A\bar{B}$$

$$D_1 = \bar{A}B \quad D_3 = AB$$

A	B	D ₀	D ₁	D ₂	D ₃
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Just implement

1:4 DMUX as De coder



S₁ S₀

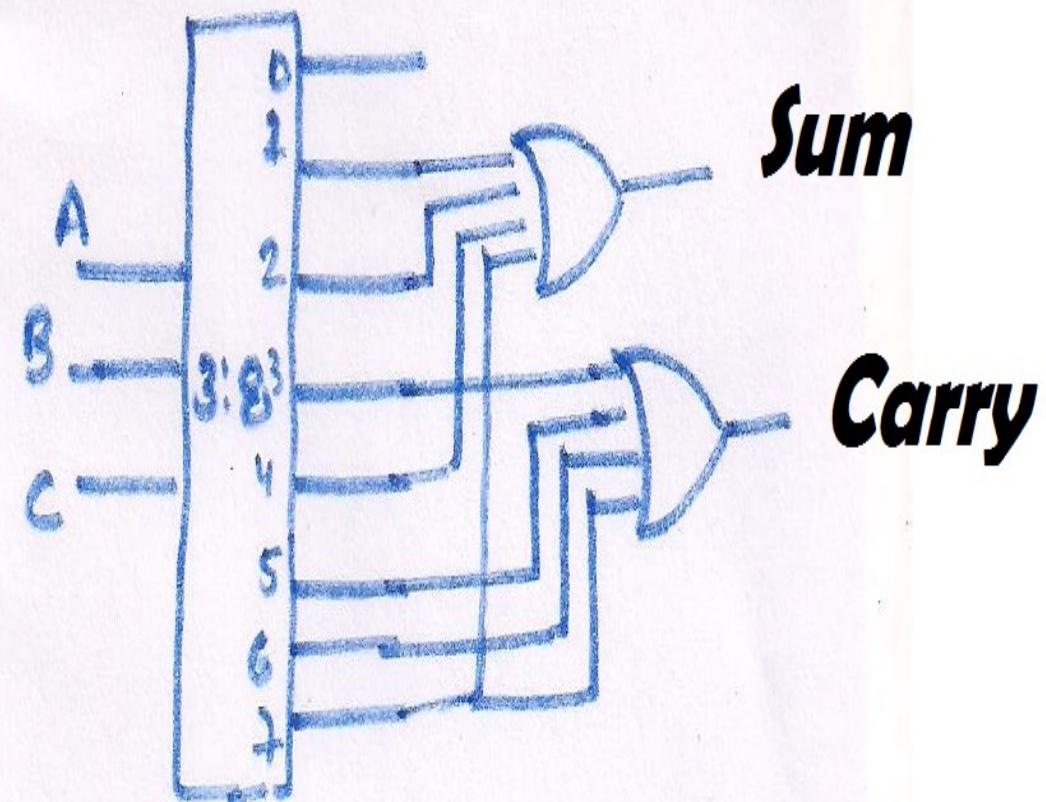
A B

Full adder using 3:8

A	B	C	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\text{Sum} = \Sigma (1, 2, 4, 7)$$

$$\text{carry} = \Sigma (3, 5, 6, 7)$$



7 segment (BCD-to-7) common cathode

$f \mid \underline{g} \mid b$	a
$e \mid \underline{\quad} \mid c$	d
$f \mid \underline{a} \mid b$	a
$e \mid \underline{d} \mid c$	b
$\mid \mid b$	c
$\underline{a} \mid b$	a
$e \mid \underline{d} \mid b$	b
$\underline{a} \mid b$	c
$\underline{\quad} \mid c$	d

A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1
1	0	1	0	x	x	x	x	0	1	1
1	0	1	1	x	x	x	x	x	x	x
1	1	0	0	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x

$$f \frac{1}{1} \frac{2}{2} \frac{1}{1} b \\ |c \quad -|c \quad c| -|c \quad 1b \quad f \frac{1}{1} \frac{2}{2} \frac{1}{1} b \\ d \quad d \quad d \quad 1c \quad \bar{d} \quad 1c$$