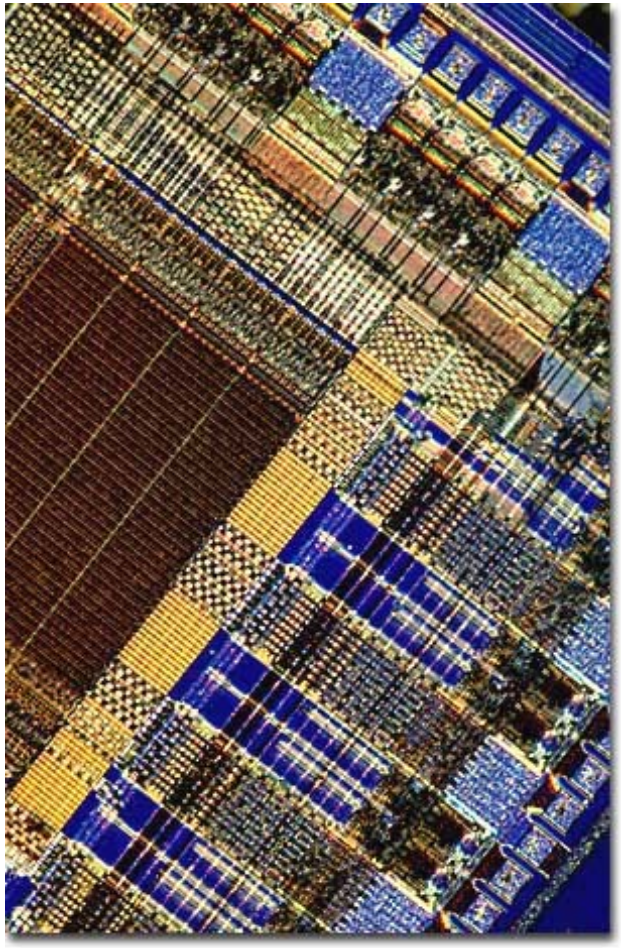
The McGraw-Hill Companies

CMOS Digital Integrated Circuits

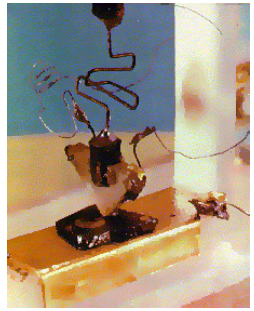


Chapter 1
Introduction

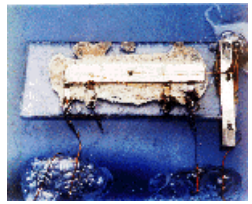
S.M. Kang and Y. Leblebici

Some History

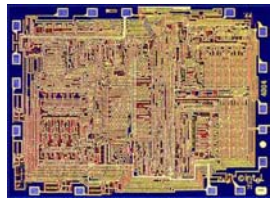
Invention of the transistor (BJT) 1947
Shockley, Bardeen, Brattain – Bell Labs



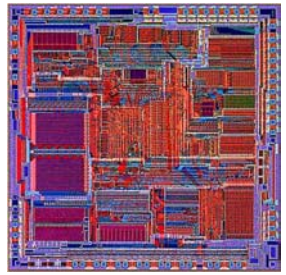
Single-transistor integrated circuit 1958
Jack Kilby – Texas Instruments



Invention of CMOS logic gates 1963
Wanlass & Sah – Fairchild Semiconductor



First microprocessor (Intel 4004) 1970
2,300 MOS transistors, 740 kHz clock frequency



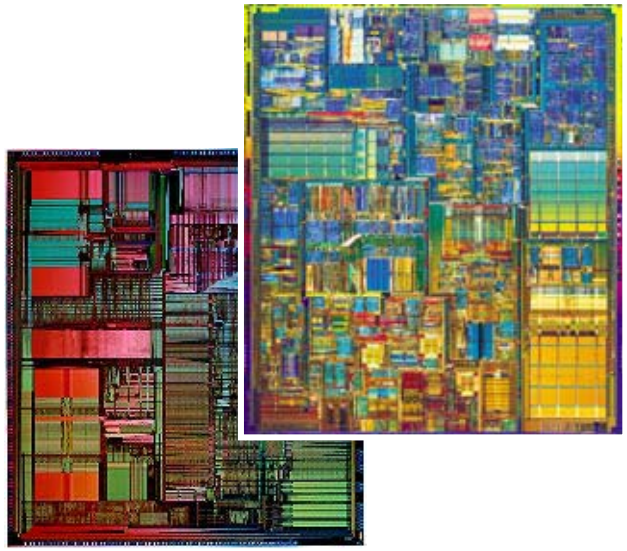
Very **L**arge **S**cale **I**ntegration 1978
Chips with more than ~20,000 devices

More Recently

Ultra **L**arge **S**cale **I**ntegration

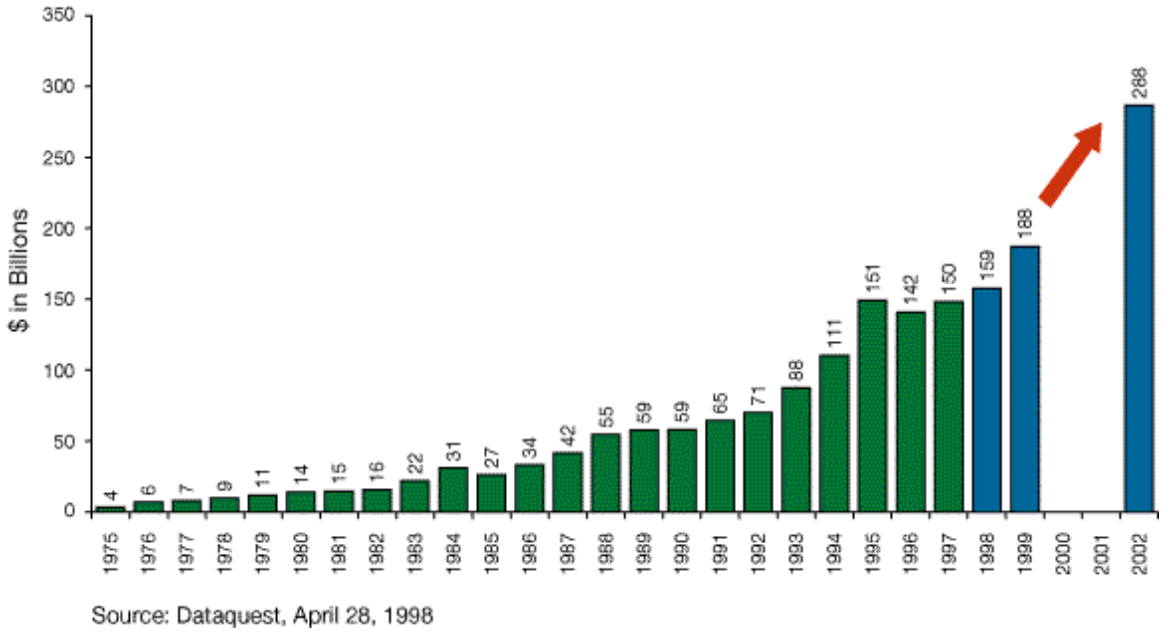
System **o**n **C**hip (**SoC**)

20 ~ 30 million transistors in 2002



The chip complexity has increased by a factor of 1000 since its first introduction, but the term **VLSI** remained virtually universal to denote digital integrated systems with high complexity.

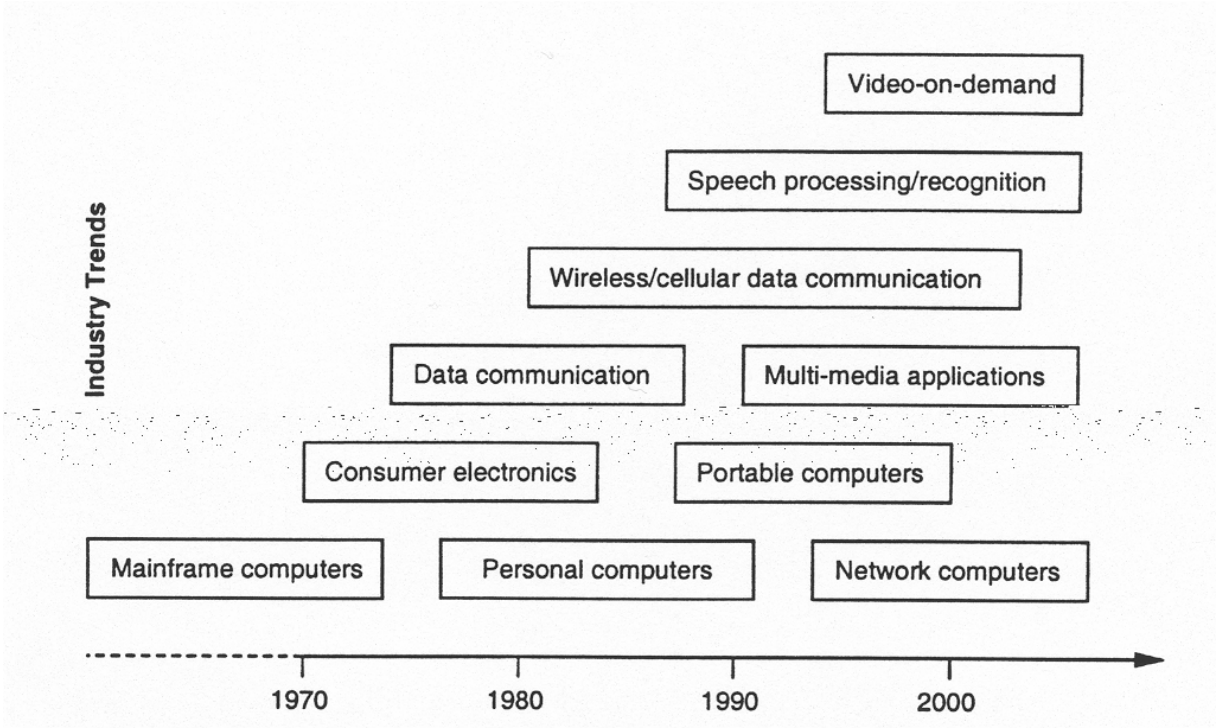
Economic Impact



Source: Dataquest, April 28, 1998

As a result of the continuously increasing integration density and decreasing unit costs, the semiconductor industry has been one of the fastest growing sectors in the worldwide economy.

Industry Trends

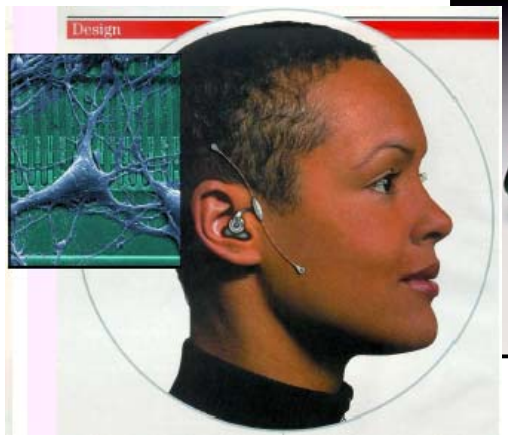


Large
Centralized
Expensive

Small / Portable
Distributed
Inexpensive

Industry Trends

High performance
Low power dissipation
Wireless capability
etc…



More portable, wearable, and more powerful devices for ubiquitous and pervasive computing…

Some Leading-Edge Examples

Intel Pentium 4

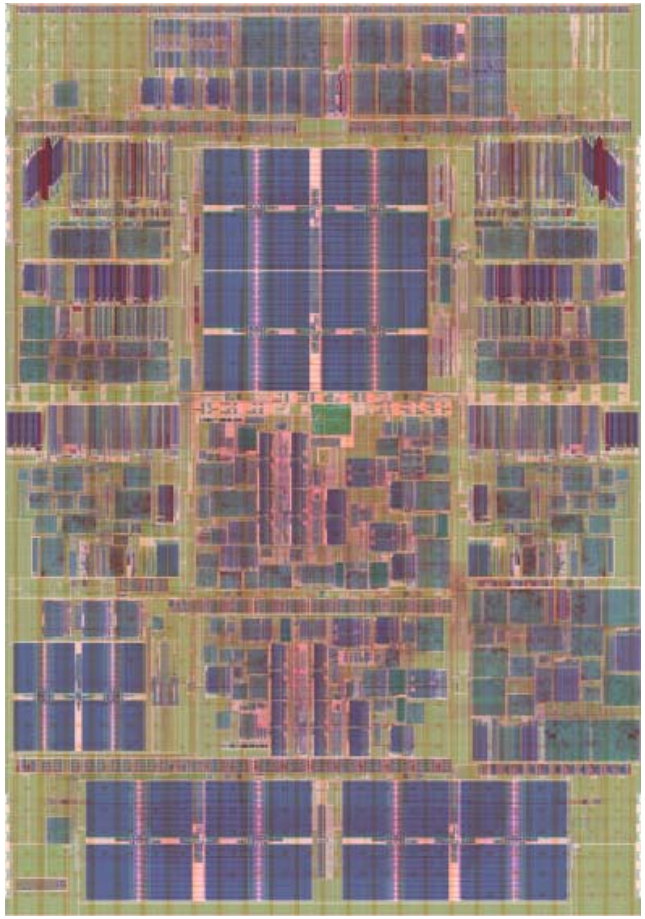
0.13μ process

55 million transistors

2.4GHz clock

145mm^2

Some Leading-Edge Examples



IBM S/390 Microprocessor

0.13 μm CMOS process

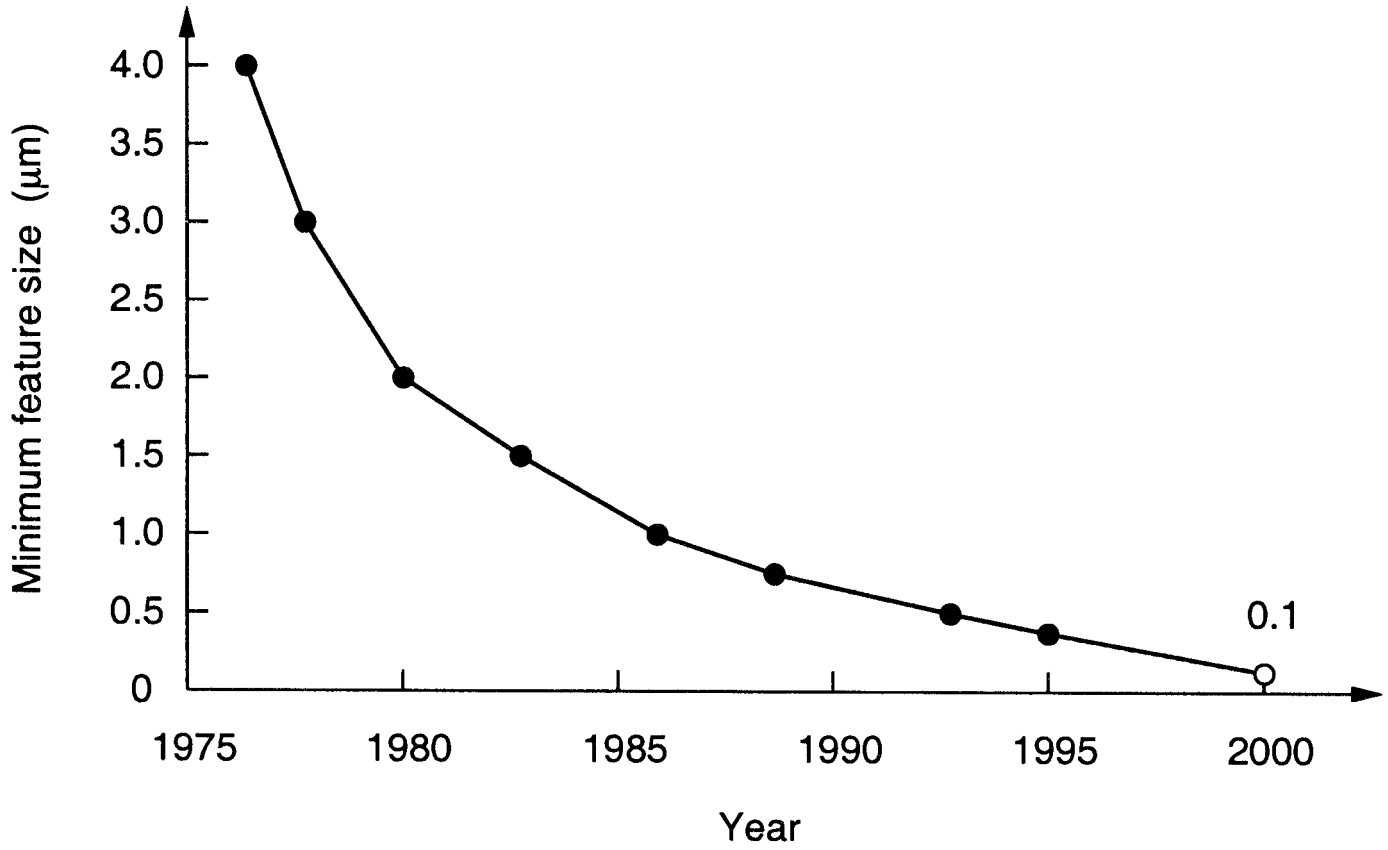
7 layers Cu interconnect

47 million transistors

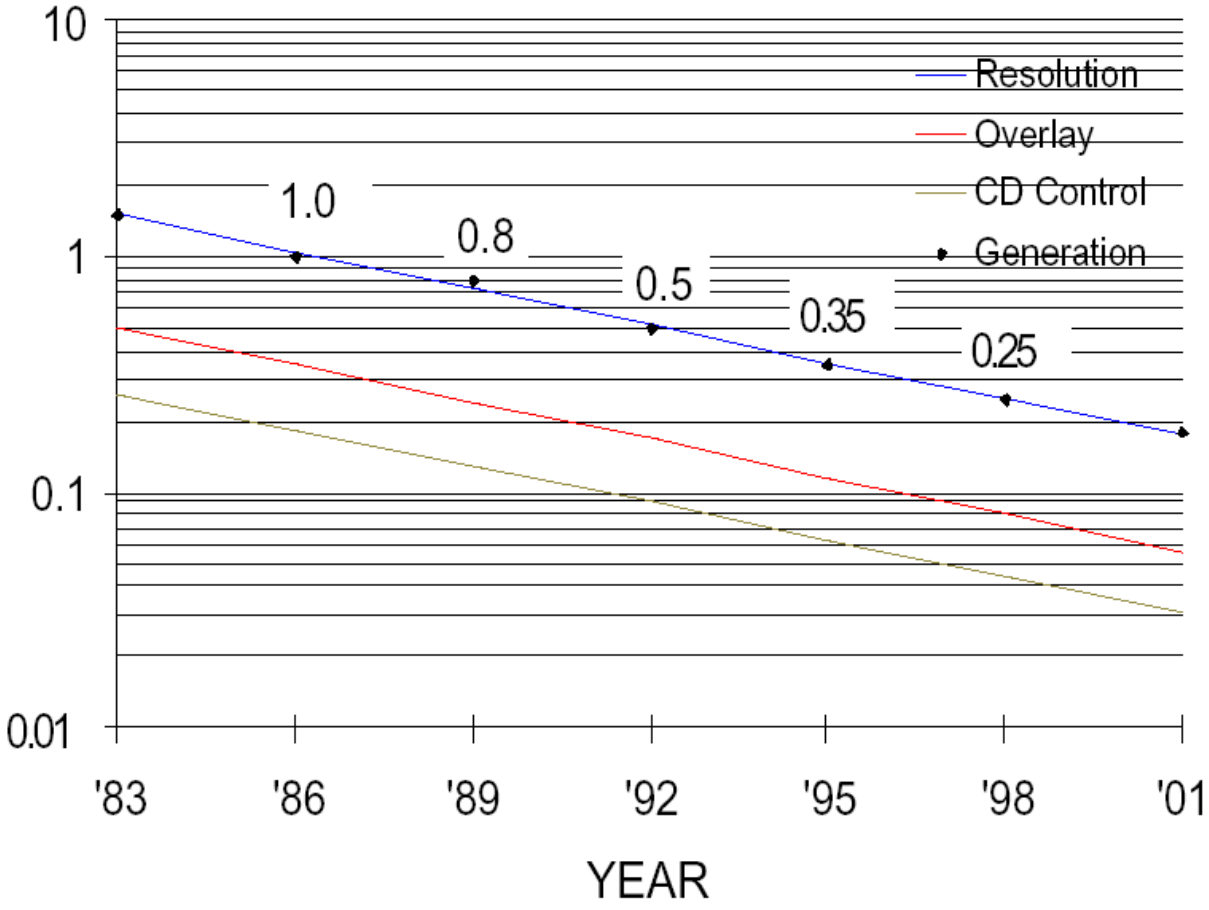
1 GHz clock

180 mm^2

Evolution of Minimum Feature Size



Evolution of Minimum Feature Size



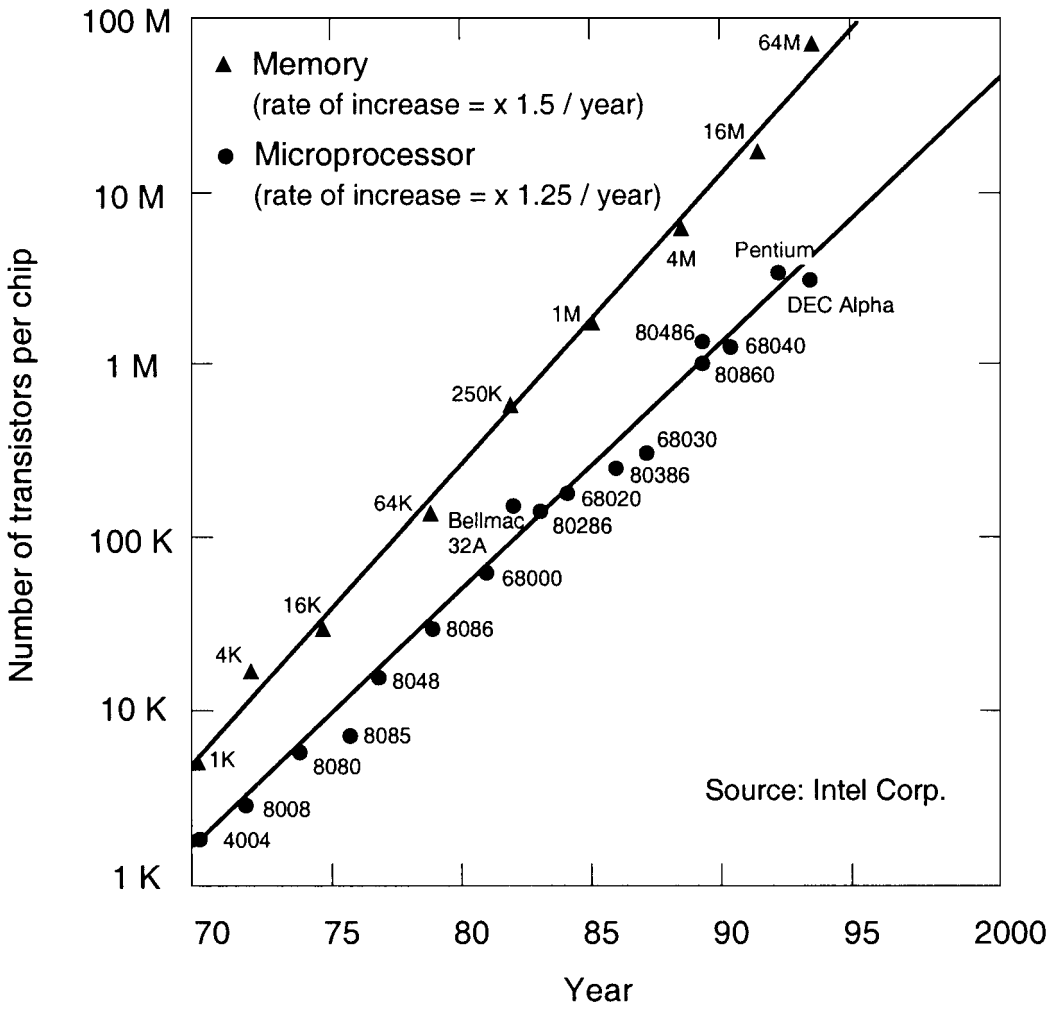
2002: 130 nm

2003: 90 nm

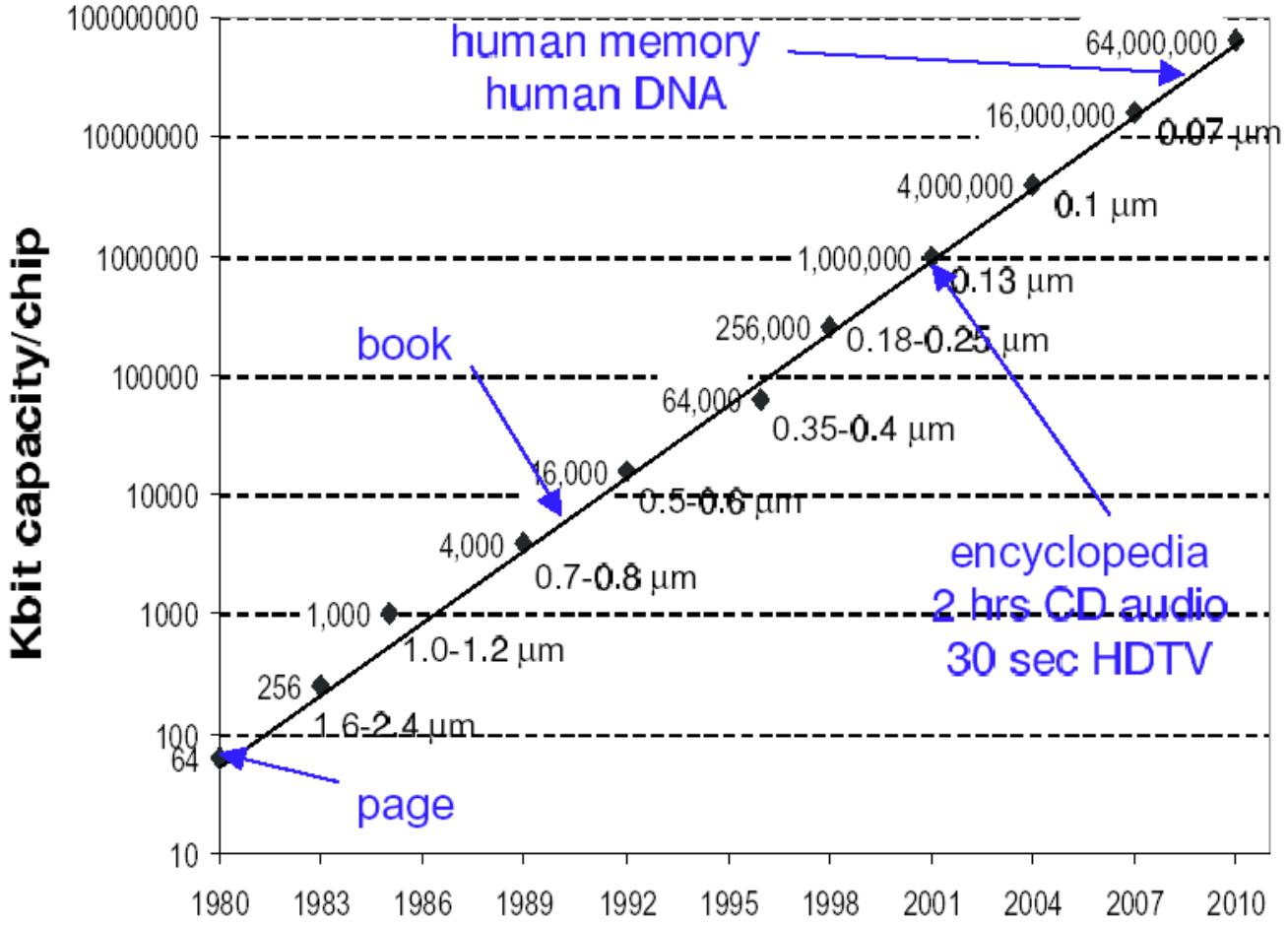
…

2010: 35 nm (?)

Moore's Law



Evolution of Memory Capacity

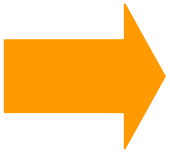


ITRS - International Technology Roadmap for Semiconductors

YEAR	2002	2005	2008	2011	2014
TECHNOLOGY	130 nm	100 nm	70 nm	50 nm	35 nm
CHIP SIZE	400 mm^2	600 mm^2	750 mm^2	800 mm^2	900 mm^2
NUMBER OF TRANSISTORS (LOGIC)	400 M	1 Billion	3 Billion	6 Billion	16 Billion
DRAM CAPACITY	2 Gbits	10 Gbits	25 Gbits	70 Gbits	200 Gbits
MAXIMUM CLOCK FREQUENCY	1.6 GHz	2.0 GHz	2.5 GHz	3.0 GHz	3.5 GHz
MINIMUM SUPPLY VOLTAGE	1.5 V	1.2 V	0.9 V	0.6 V	0.6 V
MAXIMUM POWER DISSIPATION	130 W	160 W	170 W	175 W	180 W
MAXIMUM NUMBER OF I/O PINS	2500	4000	4500	5500	6000

Predictions of the worldwide semiconductor / IC industry about its own future prospects...

Shrinking Device Dimensions



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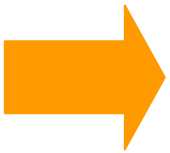
Increasing Function Density



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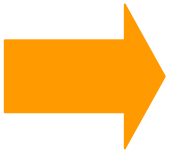
Increasing Clock Frequency



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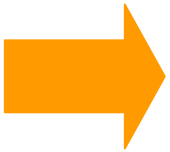
Decreasing Supply Voltage



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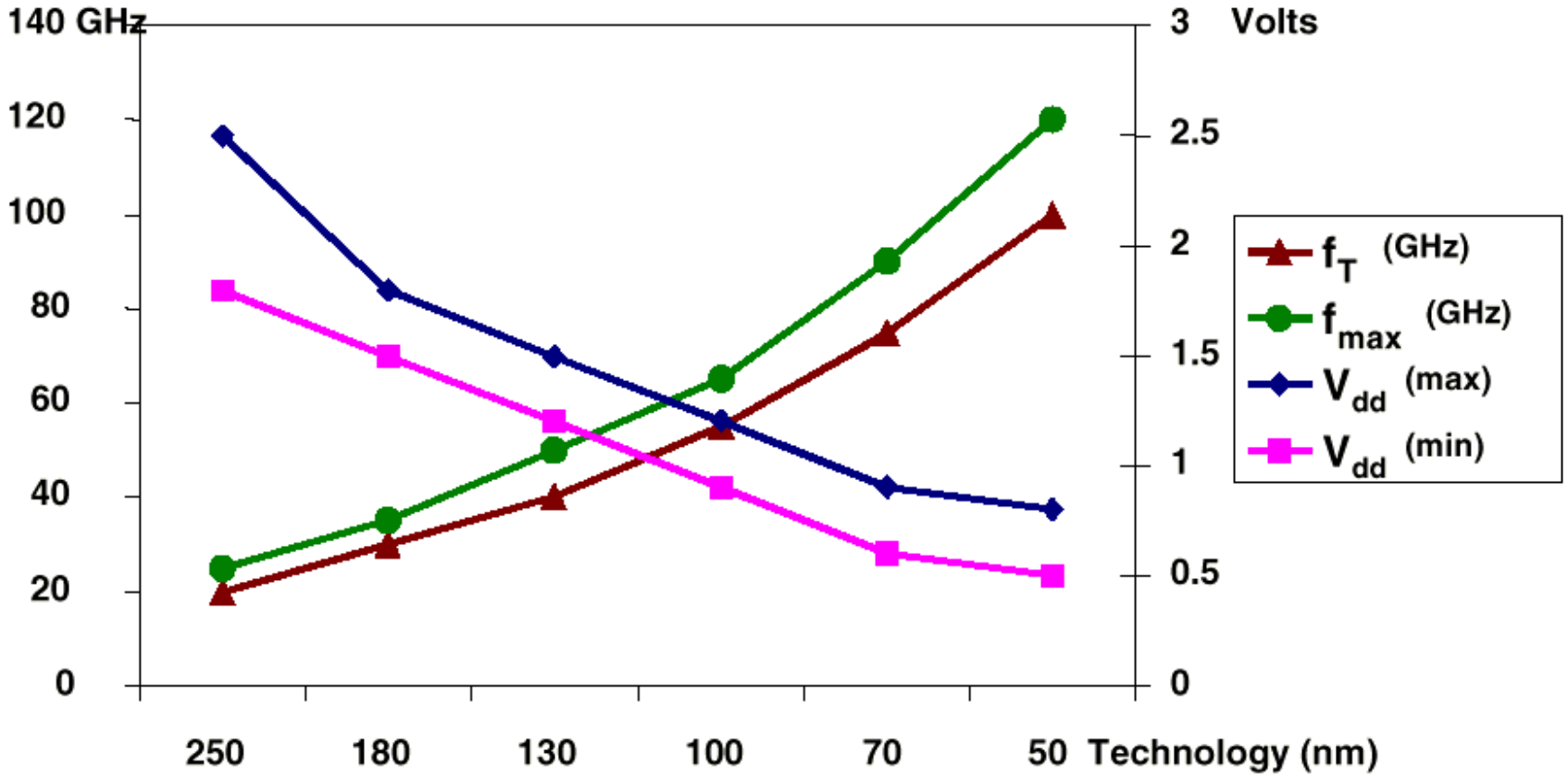
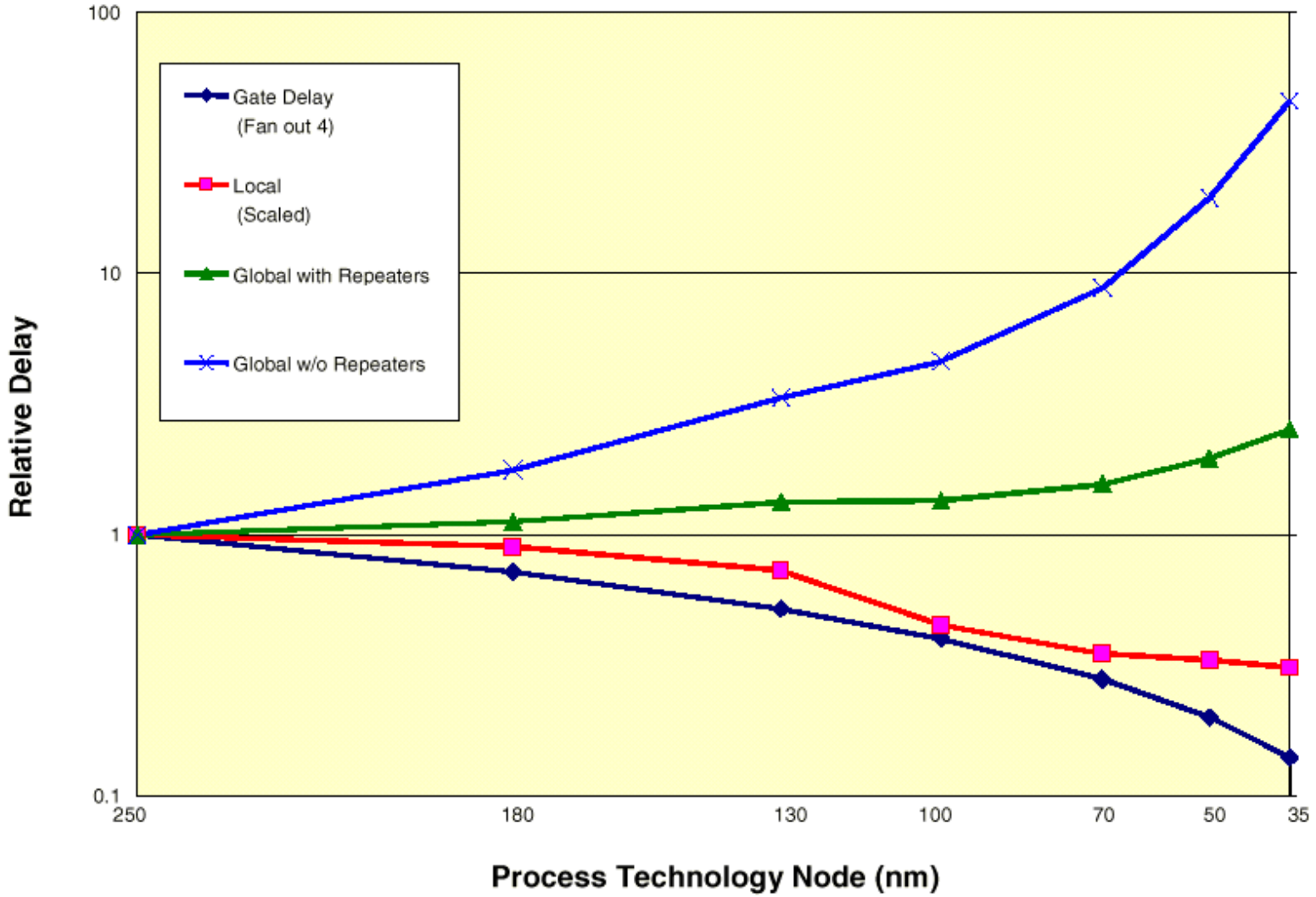
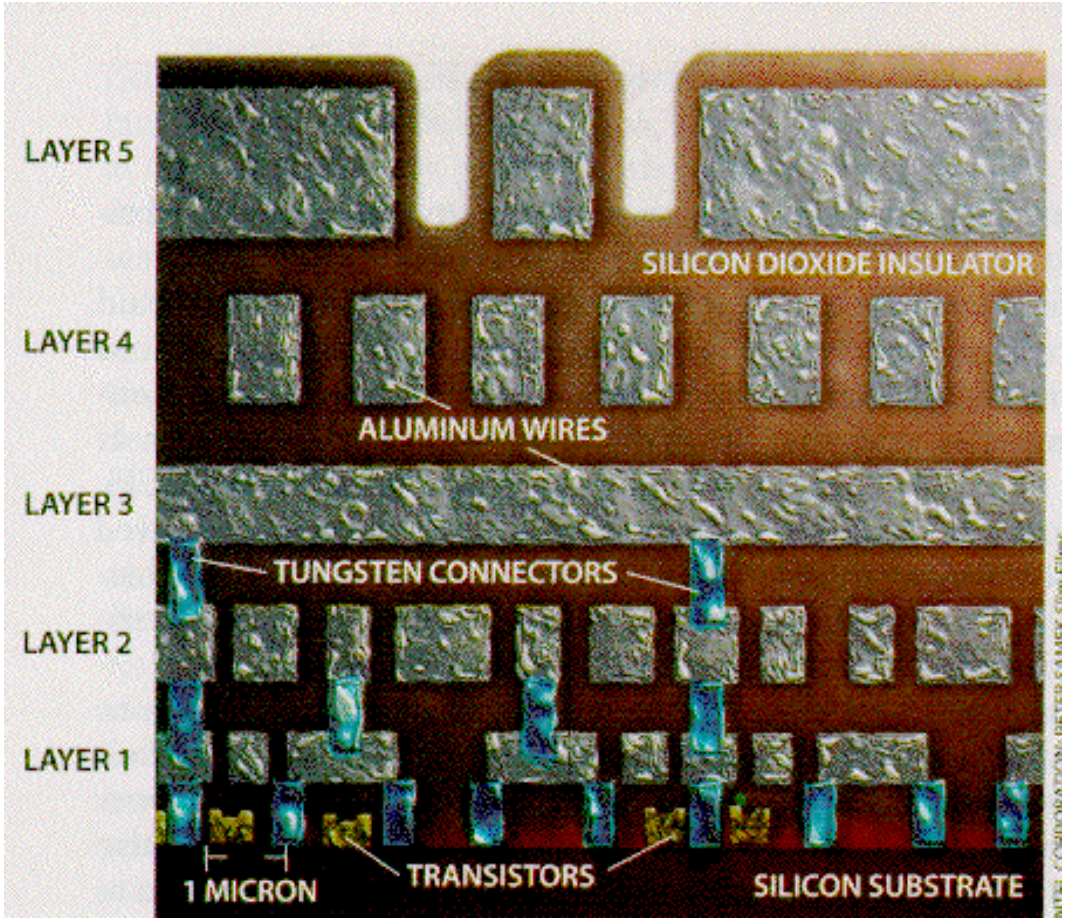
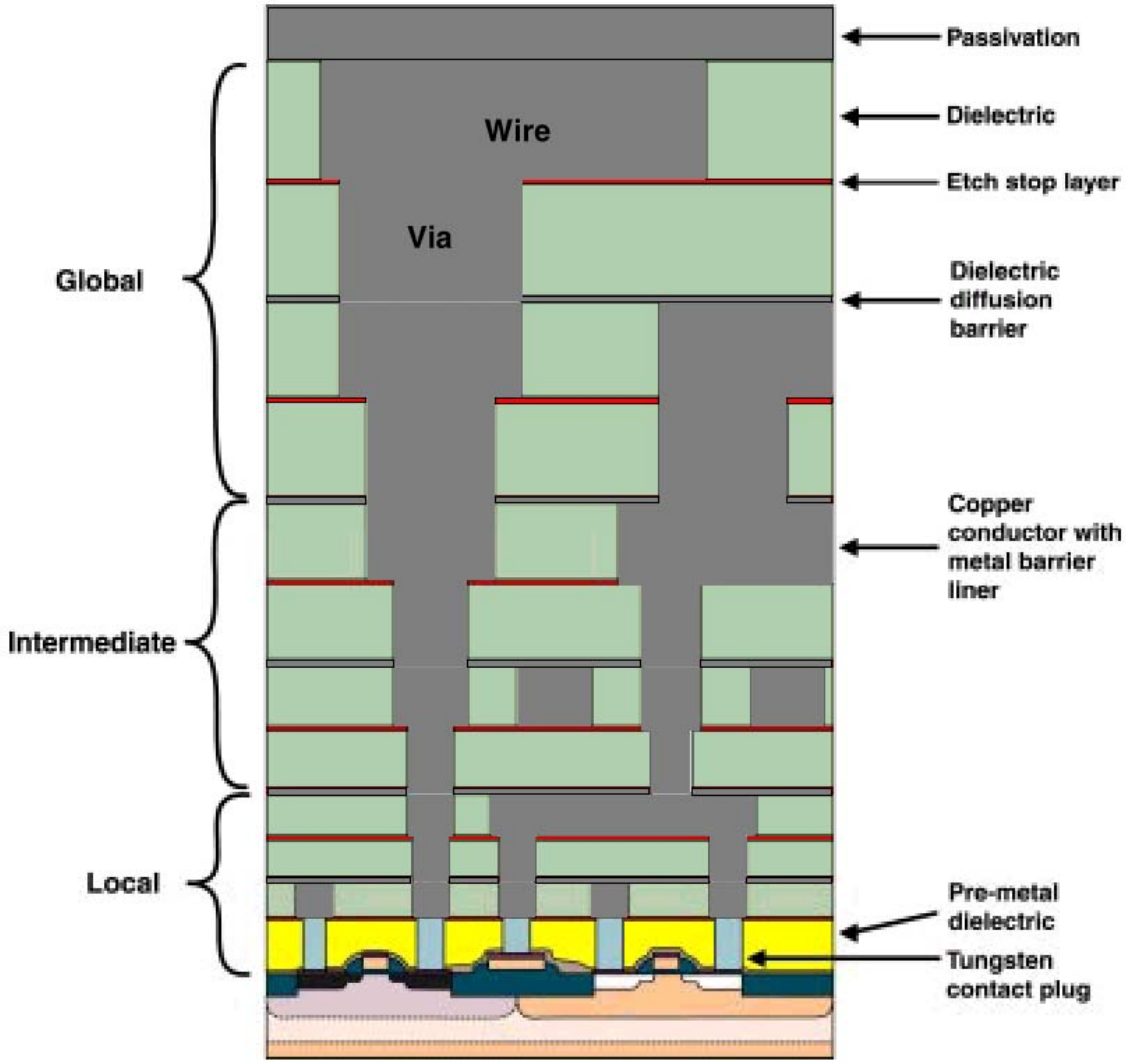

140 GHz
120
100
80
60
40
20
0
3 Volts
2.5
2
1.5
1
0.5
0
250
180
130
100
70
50 Technology (nm)
f_T (GHz)
f_{max} (GHz)
V_{dd} (max)
V_{dd} (min)


100
10
1
0.1
Relative Delay
Gate Delay
(Fan out 4)
Local
(Scaled)
Global with Repeaters
Global w/o Repeaters
250
180
130
100
70
50
35
Process Technology Node (nm)



5-layer cross-section of chip

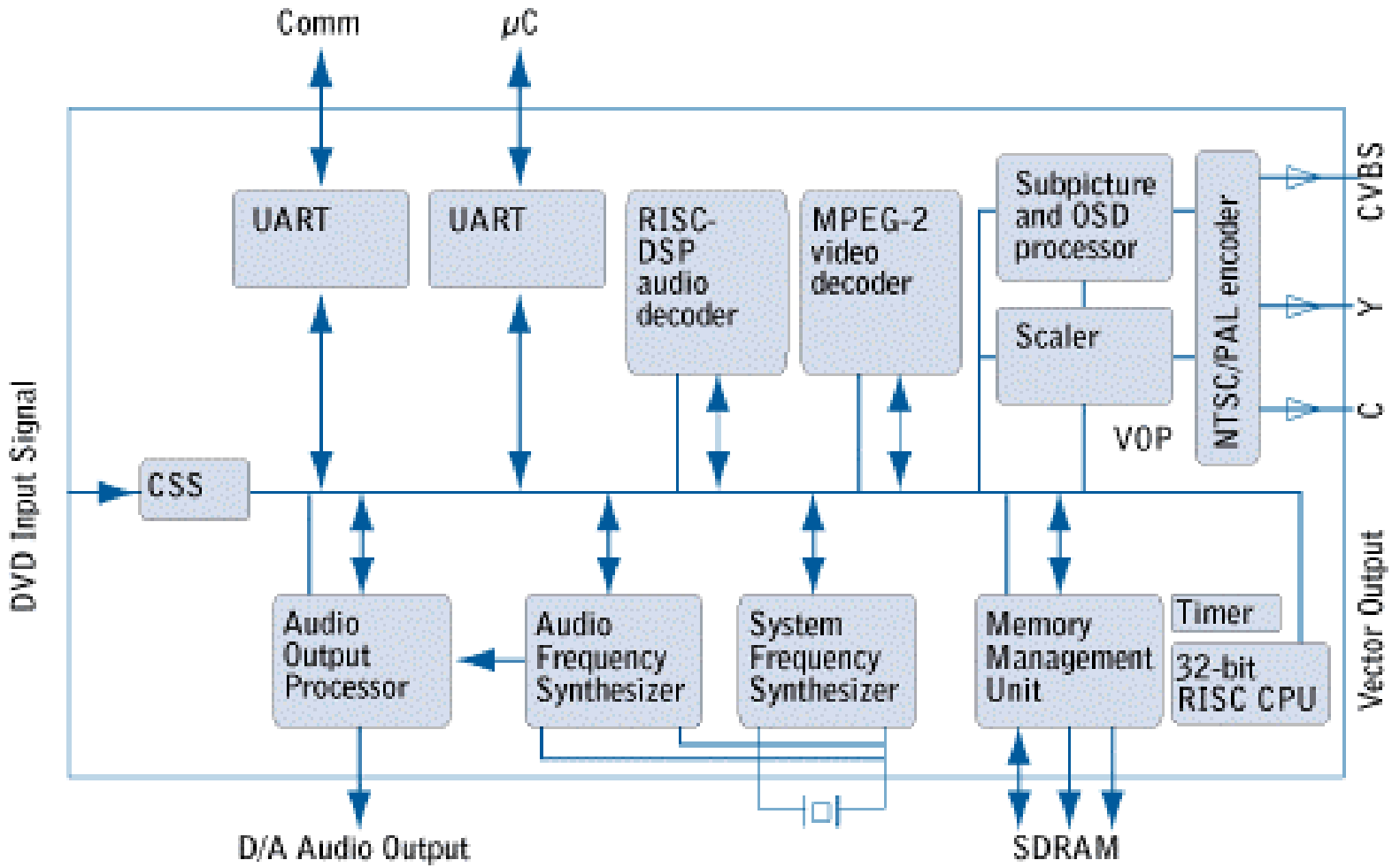
Typical Chip Cross Section



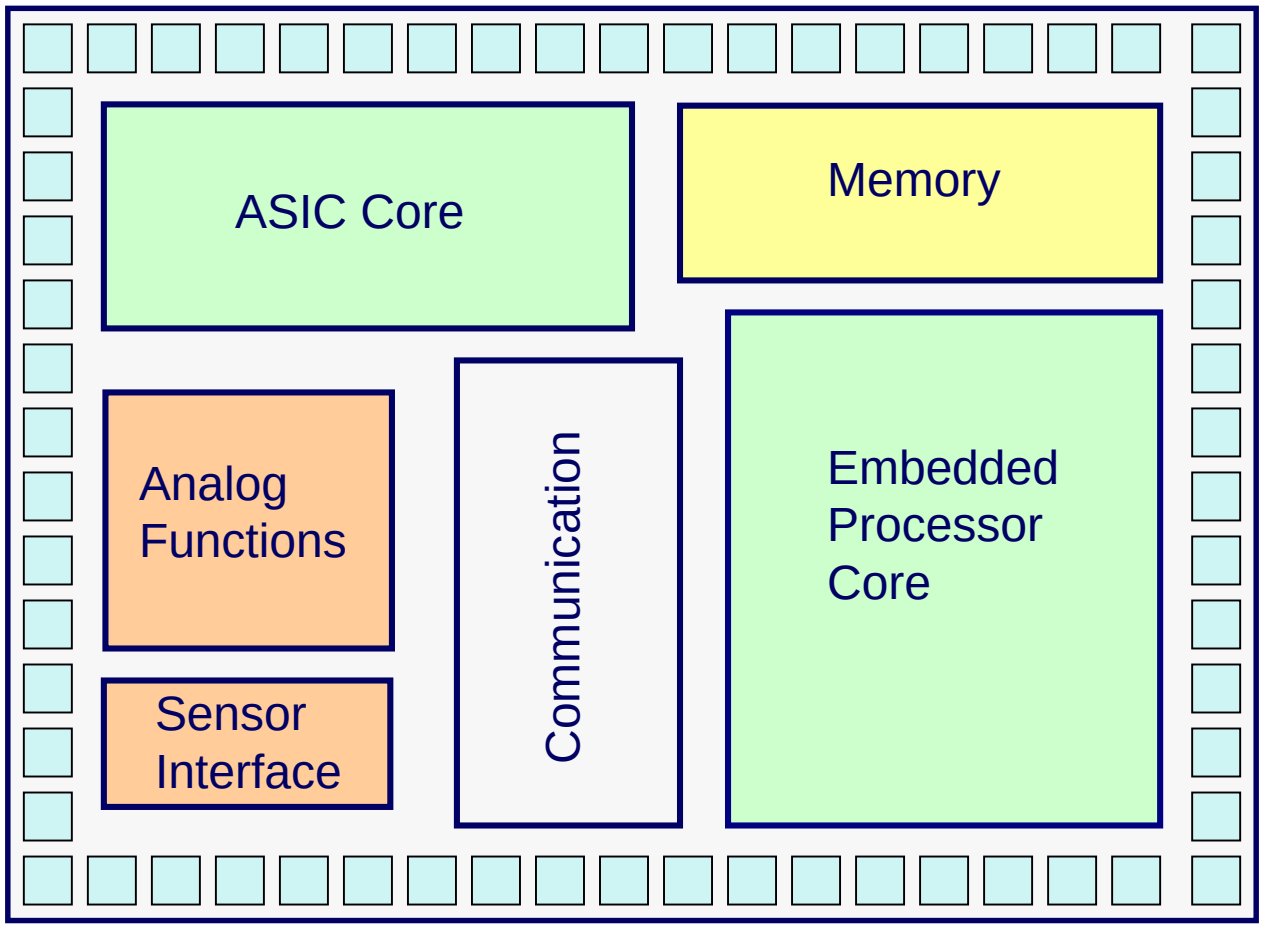
System-on-Chip

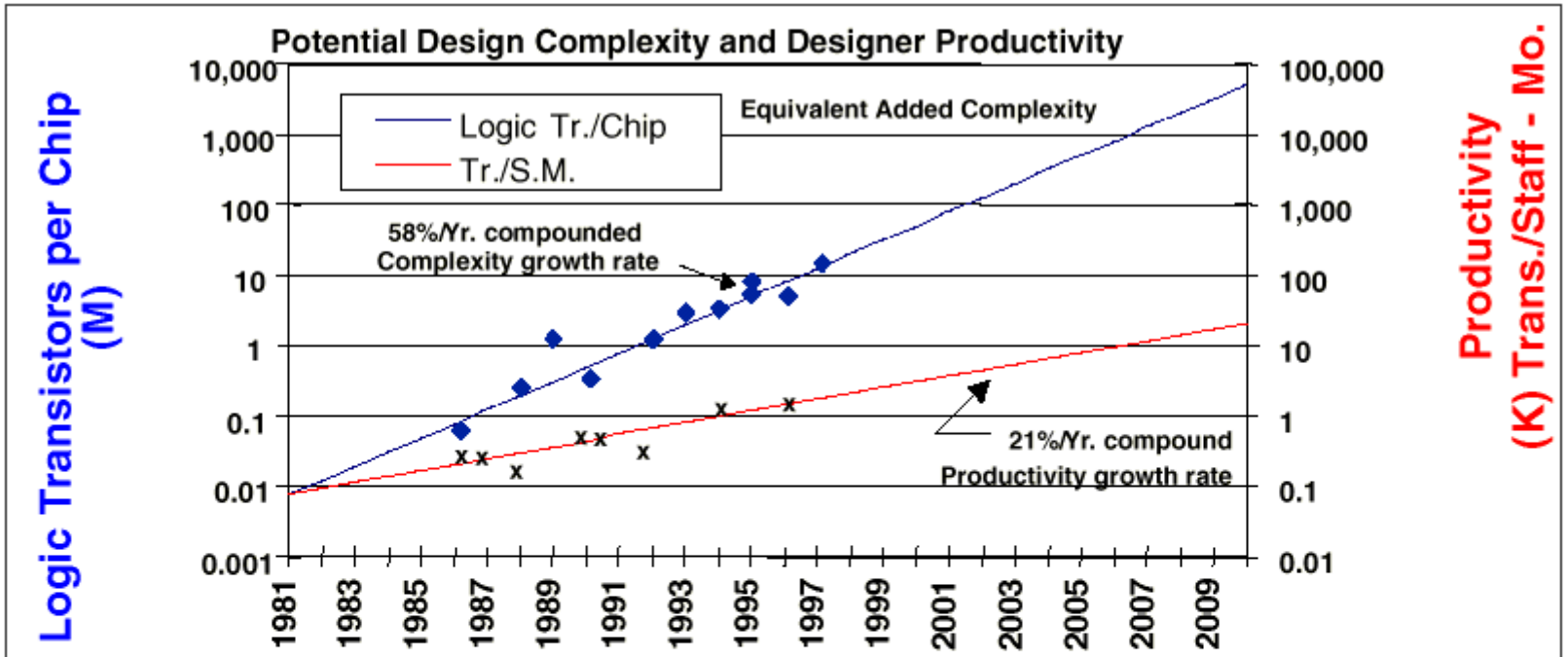
Integrating all or most of the components of a hybrid system on a single substrate (silicon or MCM), rather than building a conventional printed circuit board.

1. More compact system realization
2. Higher speed / performance
   - Better reliability
   - Less expensive !


Comm
µC
UART
UART
RISC-
DSP
audio
decoder
MPEG-2
video
decoder
Subpicture
and OSD
processor
Scaler
VOP
NTSC/PAL encoder
CVBS
Y
C
DVD Input Signal
CSS
Audio
Output
Processor
Audio
Frequency
Synthesizer
System
Frequency
Synthesizer
Memory
Management
Unit
Timer
32-bit
RISC CPU
Vector Output
D/A Audio Output
SDRAM

New Direction: System-on-Chip (SoC)

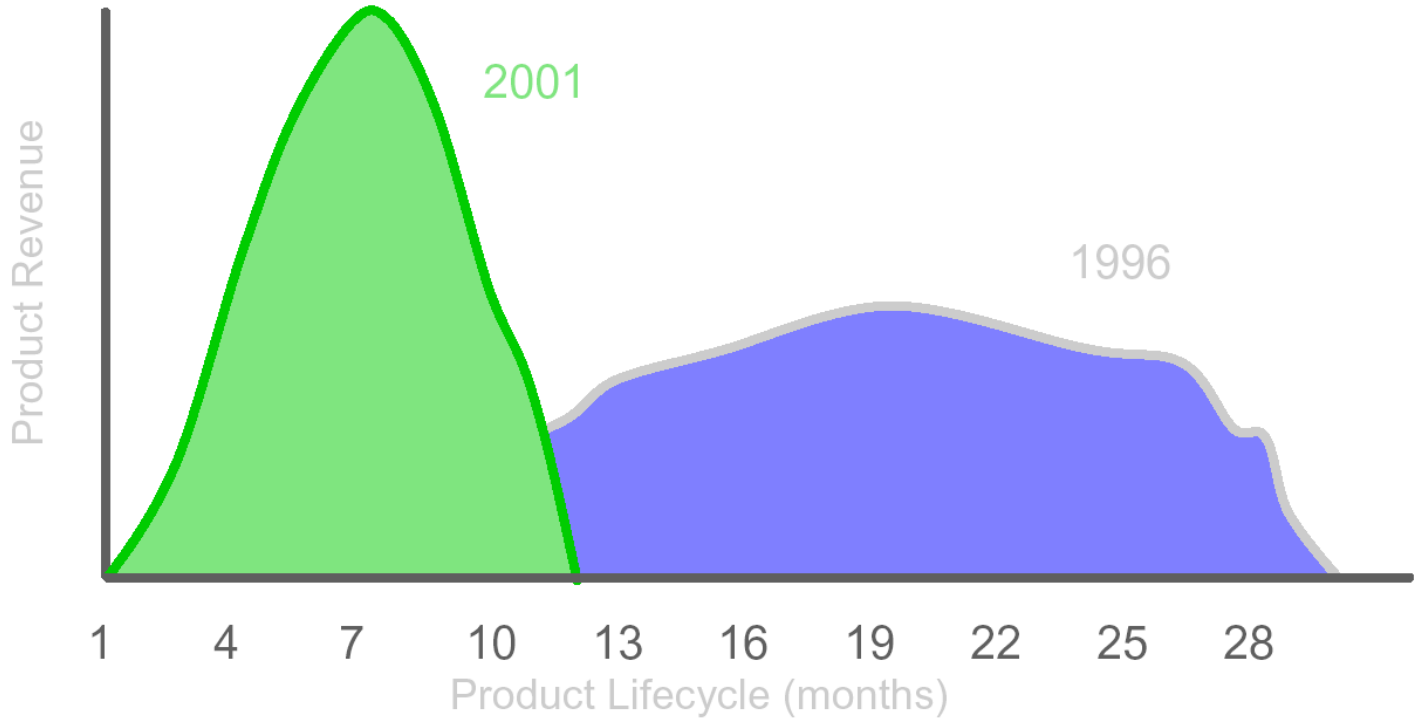


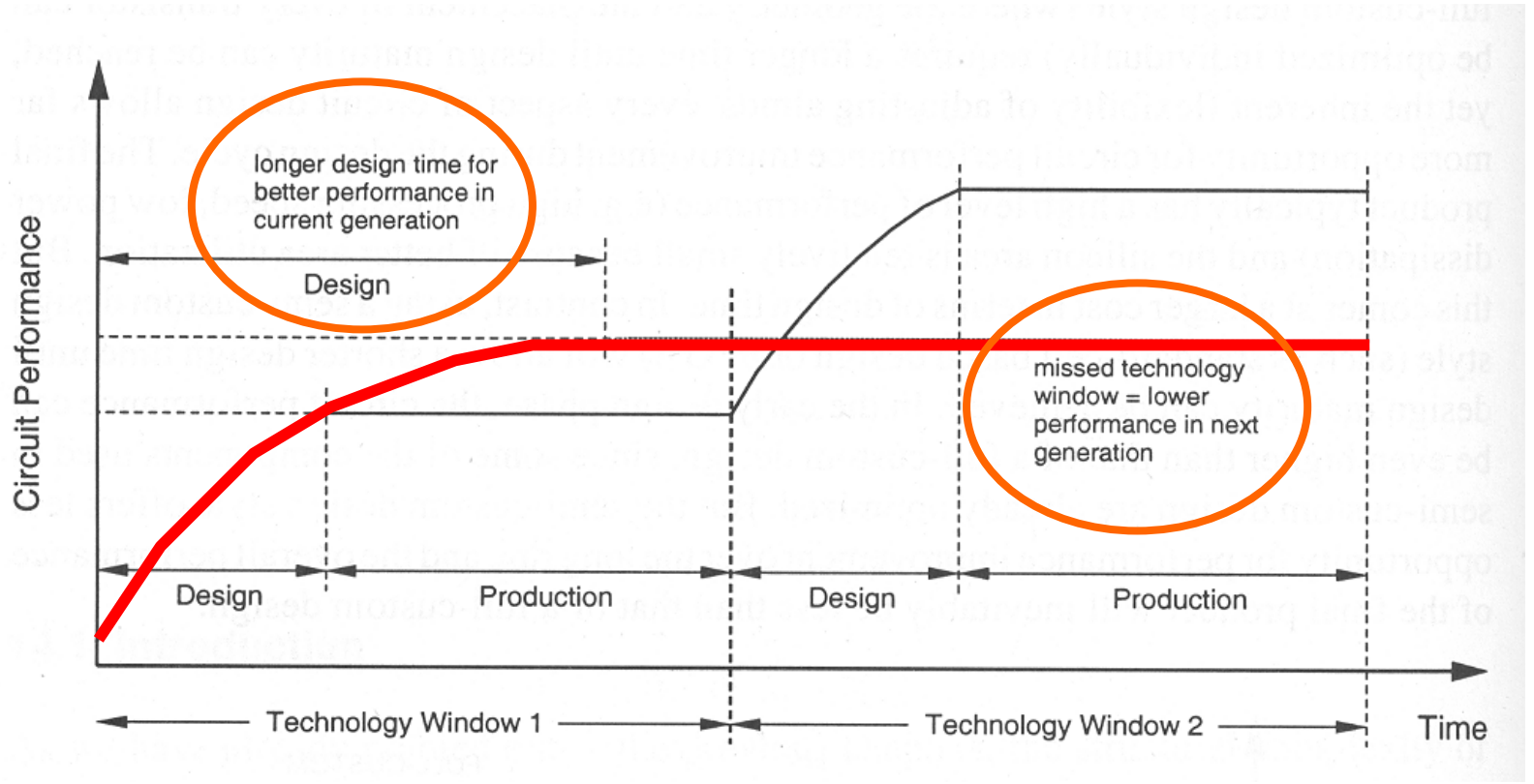


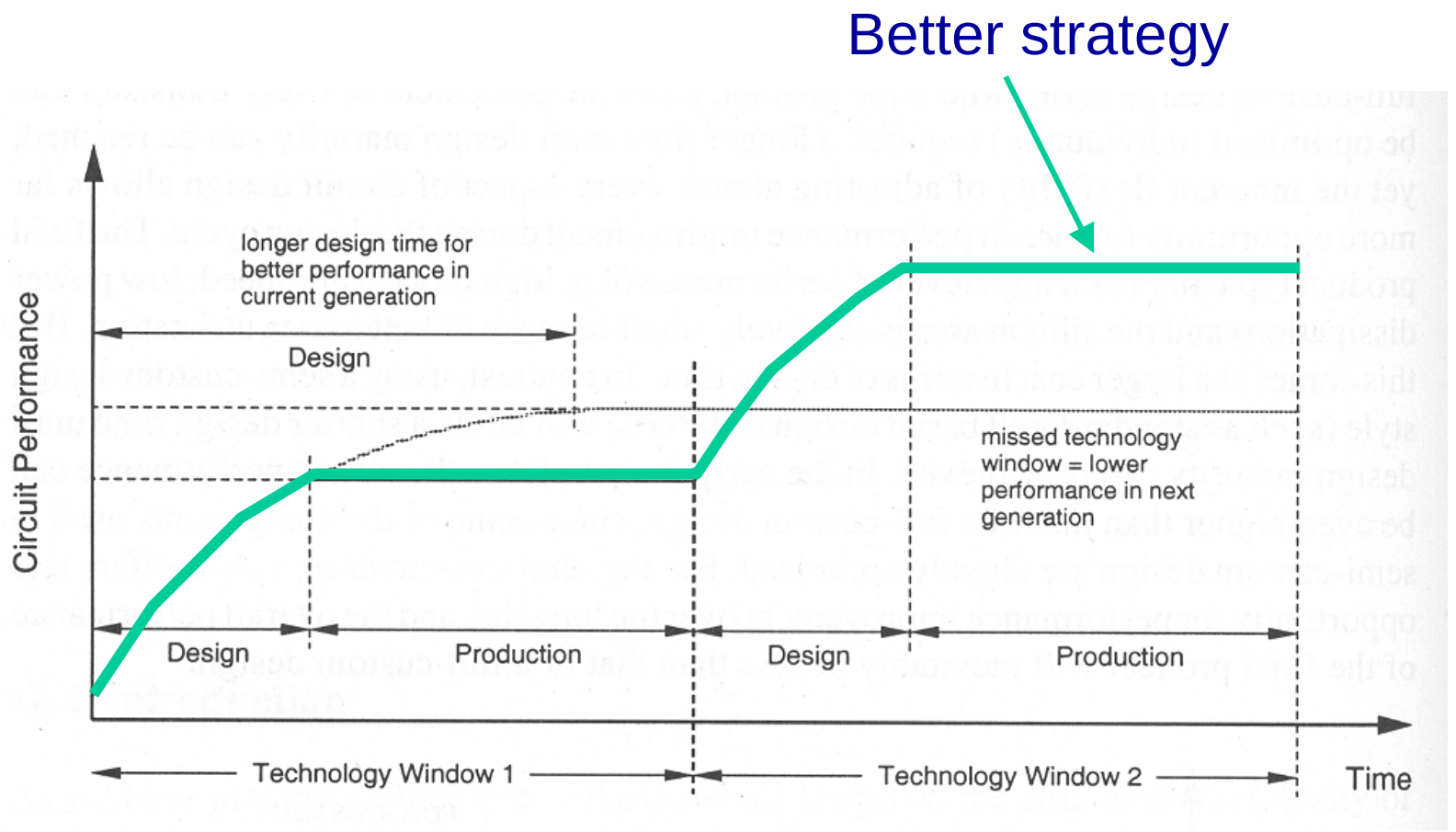
Year	Technology	Chip Complexity	Frequency	3 Yr. Design Staff	Staff Cost*
1997	250 nm	13 M Tr.	400	210	90 M
1998	250 nm	20 M Tr.	500	270	120 M
1999	180 nm	32 M Tr.	600	360	160 M
2002	130 nm	130 M Tr.	800	800	360 M

* @ $150K / Staff Yr. (In 1997 Dollars)

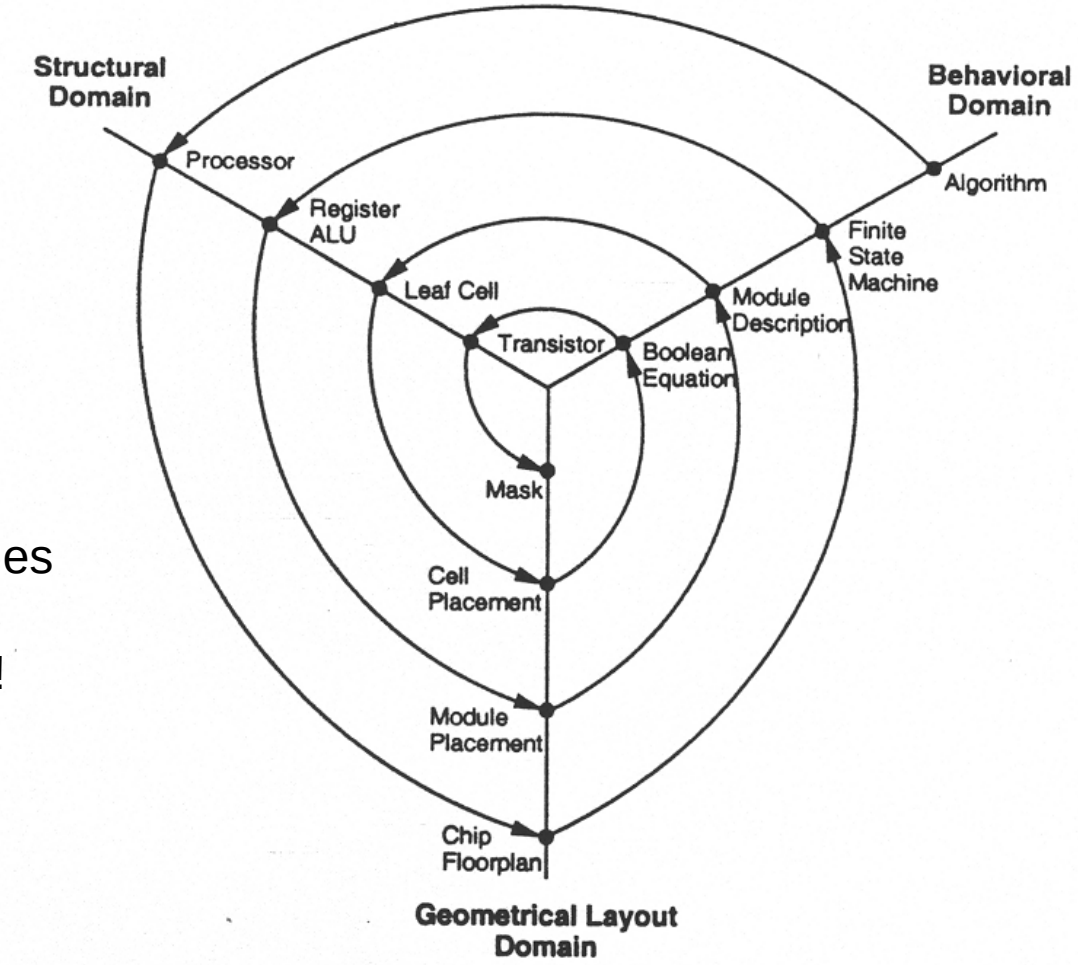
Products have a shorter life-cycle !




longer design time for better performance in current generation
Design
missed technology window = lower performance in next generation
Circuit Performance
Design
Production
Design
Production
Technology Window 1
Technology Window 2
Time

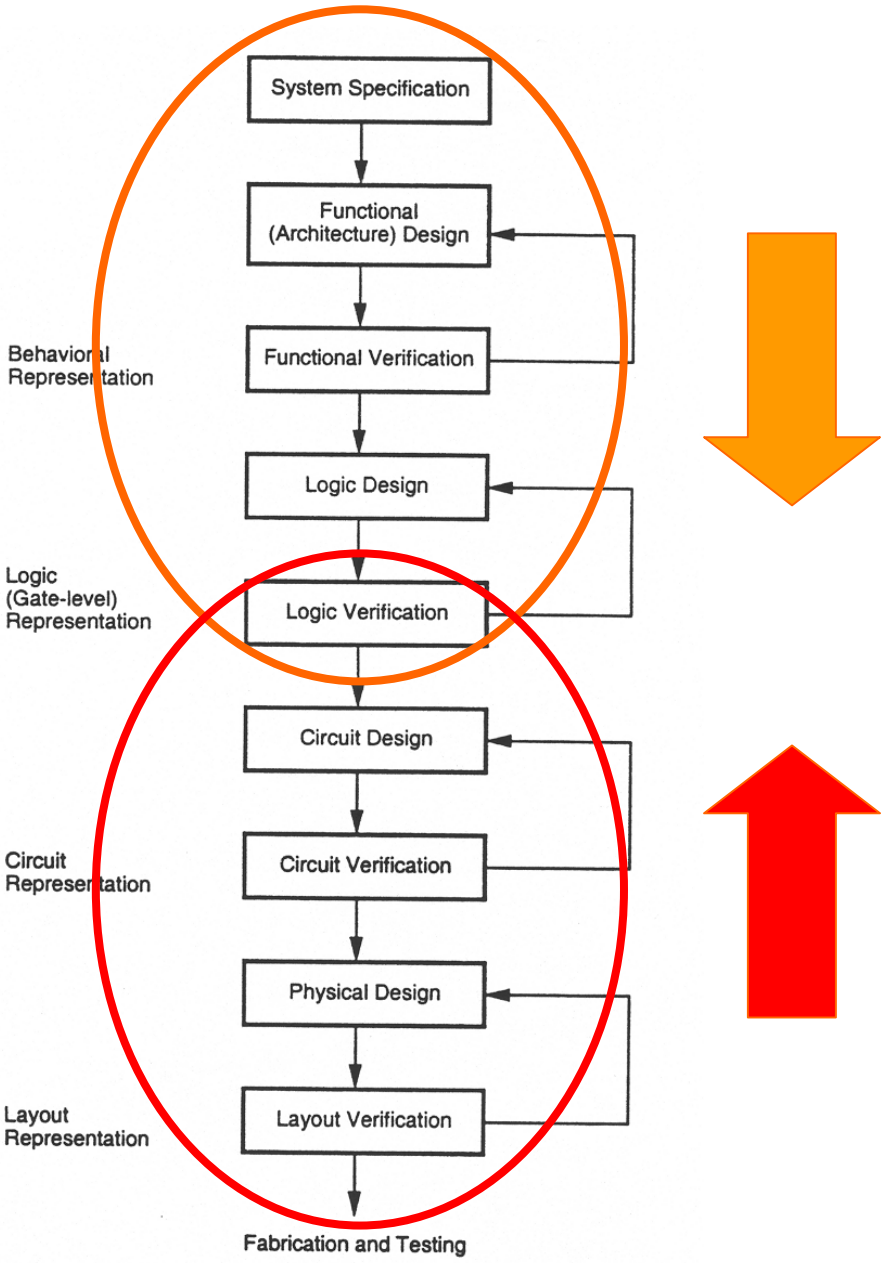

Better strategy
longer design time for
better performance in
current generation
Design
missed technology
window = lower
performance in next
generation
Circuit Performance
Design
Production
Design
Production
Technology Window 1
Technology Window 2
Time

The Y-Chart



Notice: There is a need for structured design methodologies to handle the high level of complexity !

Simplified VLSI Design Flow



Top-down

Bottom-up

Structured Design Principles

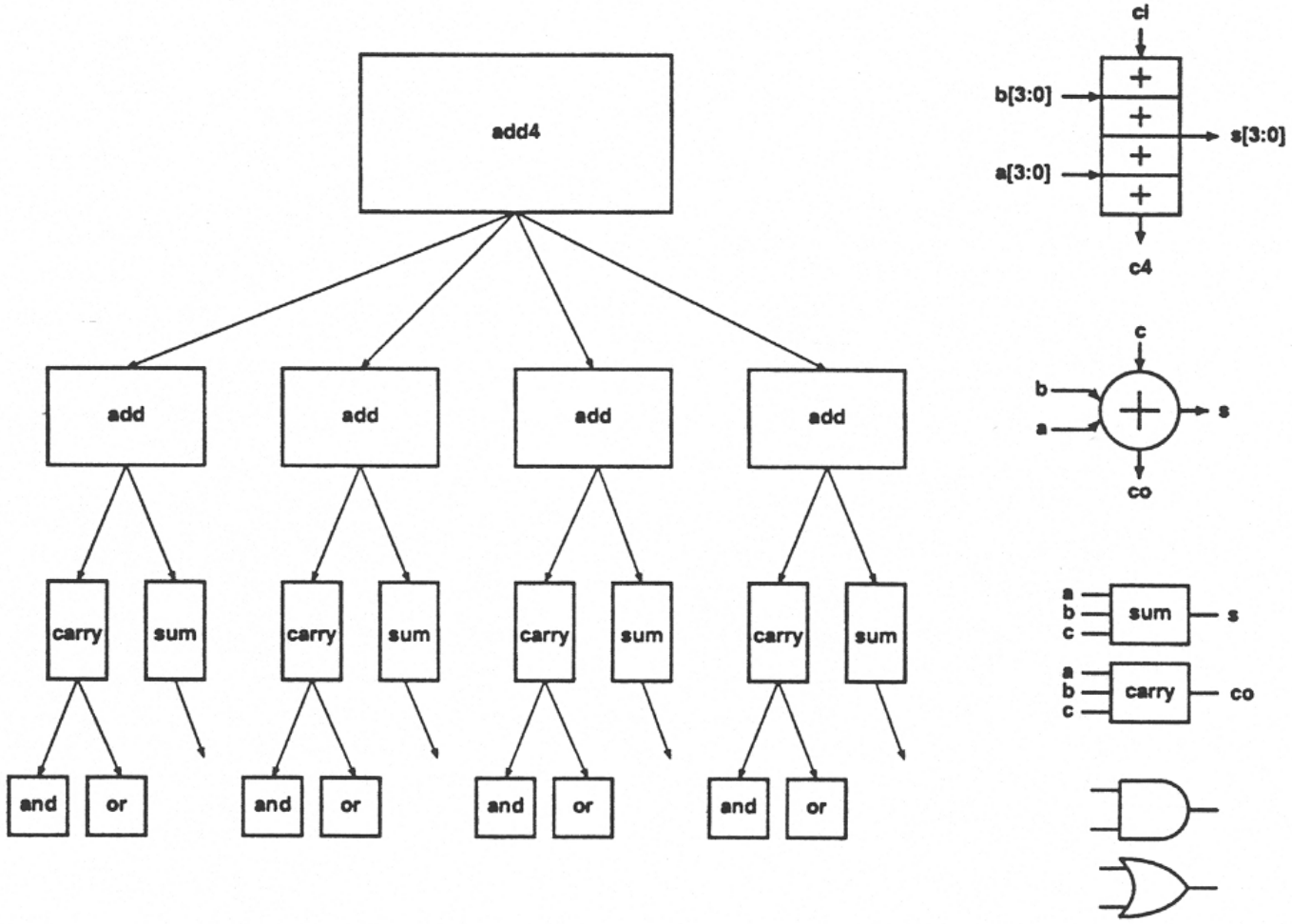
Hierarchy: "Divide and conquer" technique involves dividing a module into sub-modules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable.

Regularity: The hierarchical decomposition of a large system should result in not only **simple**, but also **similar** blocks, as much as possible. Regularity usually reduces the number of different modules that need to be designed and verified, at all levels of abstraction.

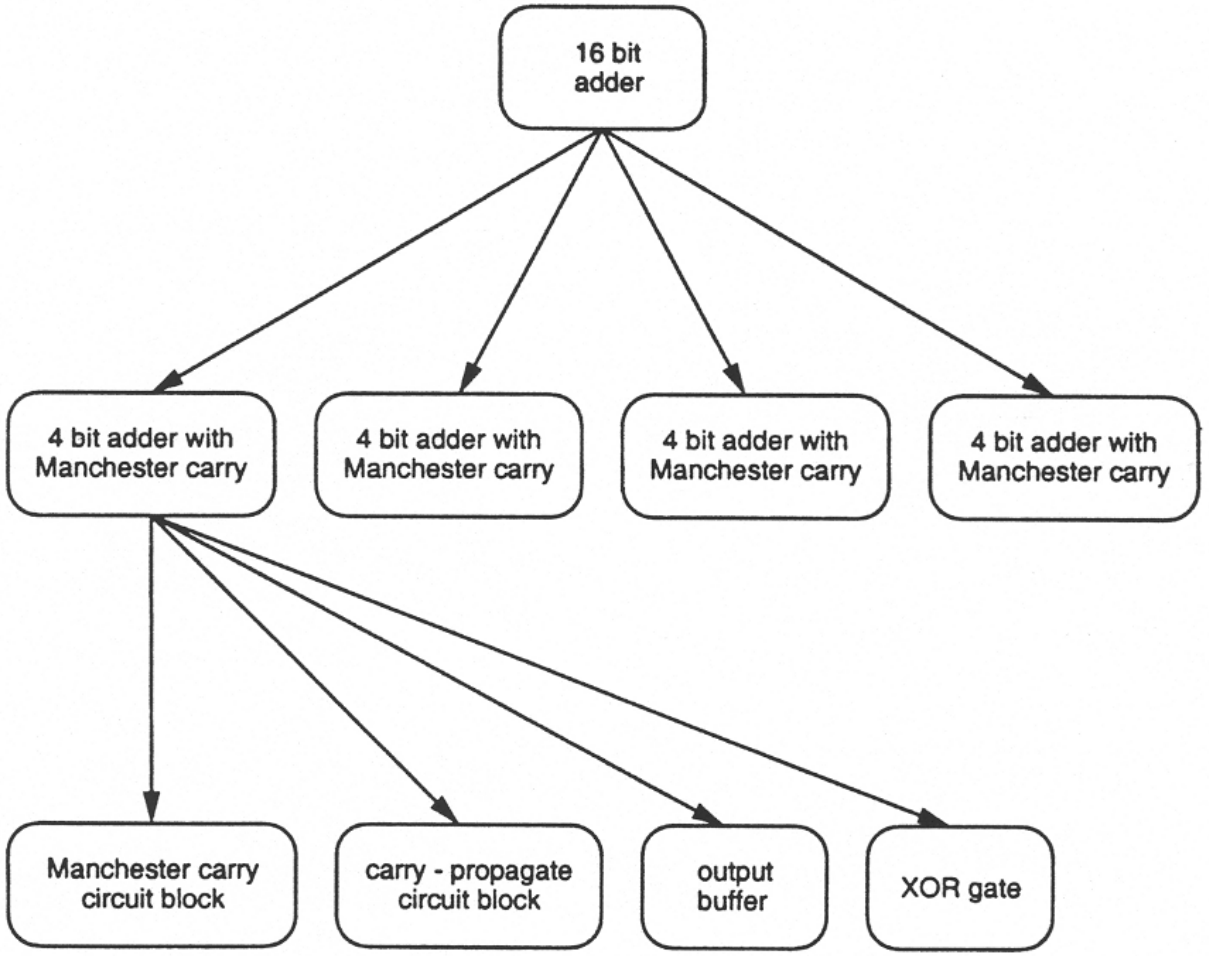
Modularity: The various functional blocks which make up the larger system must have **well-defined functions** and **interfaces**.

Locality: Internal details remain at the local level. The concept of locality also ensures that connections are mostly between neighboring modules, **avoiding long-distance connections** as much as possible.

Hierarchy of a 4-bit Carry Ripple Adder



Hierarchy of a 16-bit Manchester Adder



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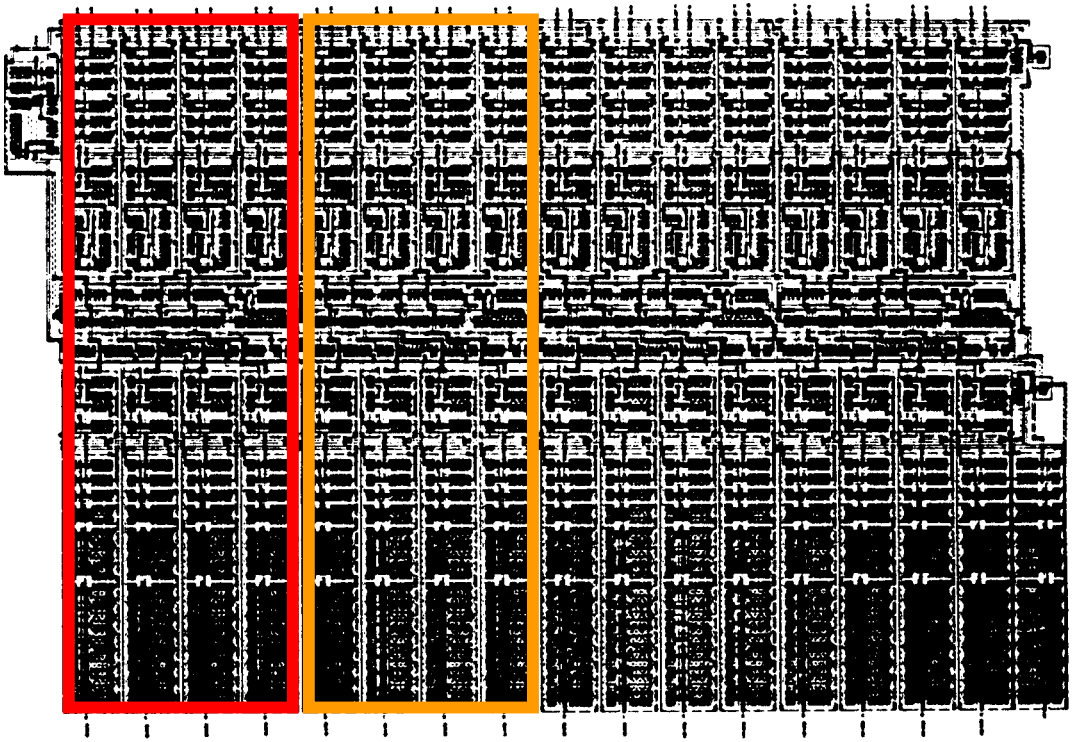
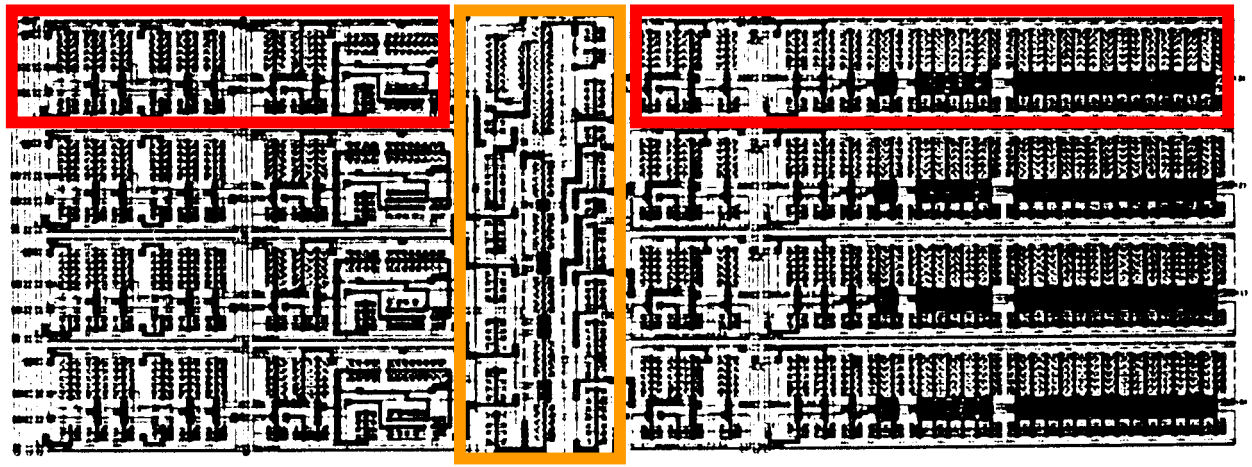


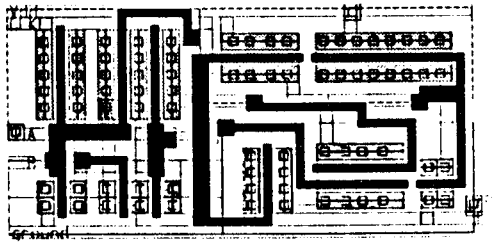
16-bit adder
complete layout

Hierarchy of a 16-bit Manchester Adder

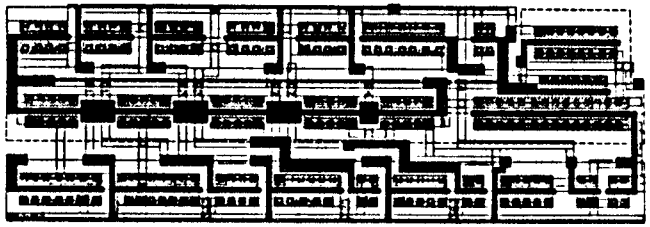


4-bit adder with
Manchester carry

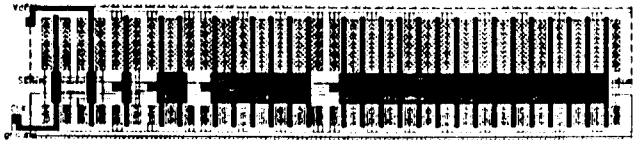
Hierarchy of a 16-bit Manchester Adder



Carry/propagate
circuit layout

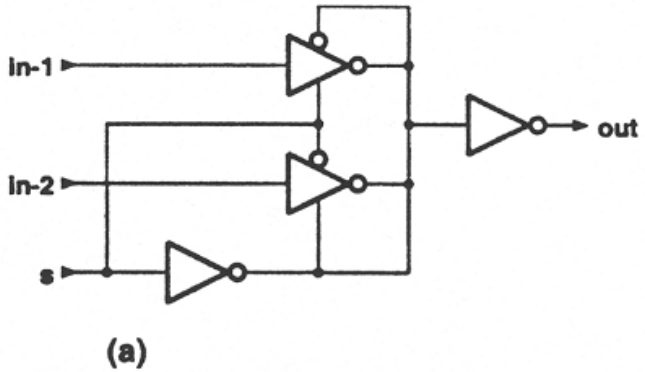


Manchester carry
circuit layout



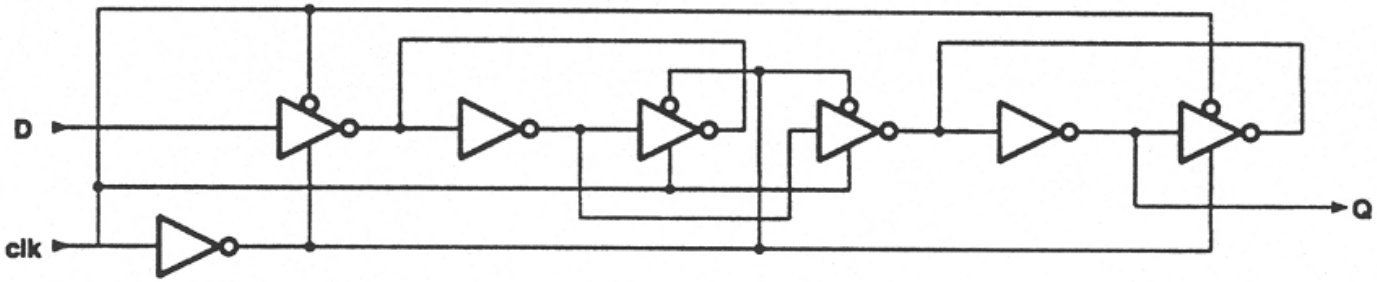
Output buffer/latch
circuit layout

Regularity

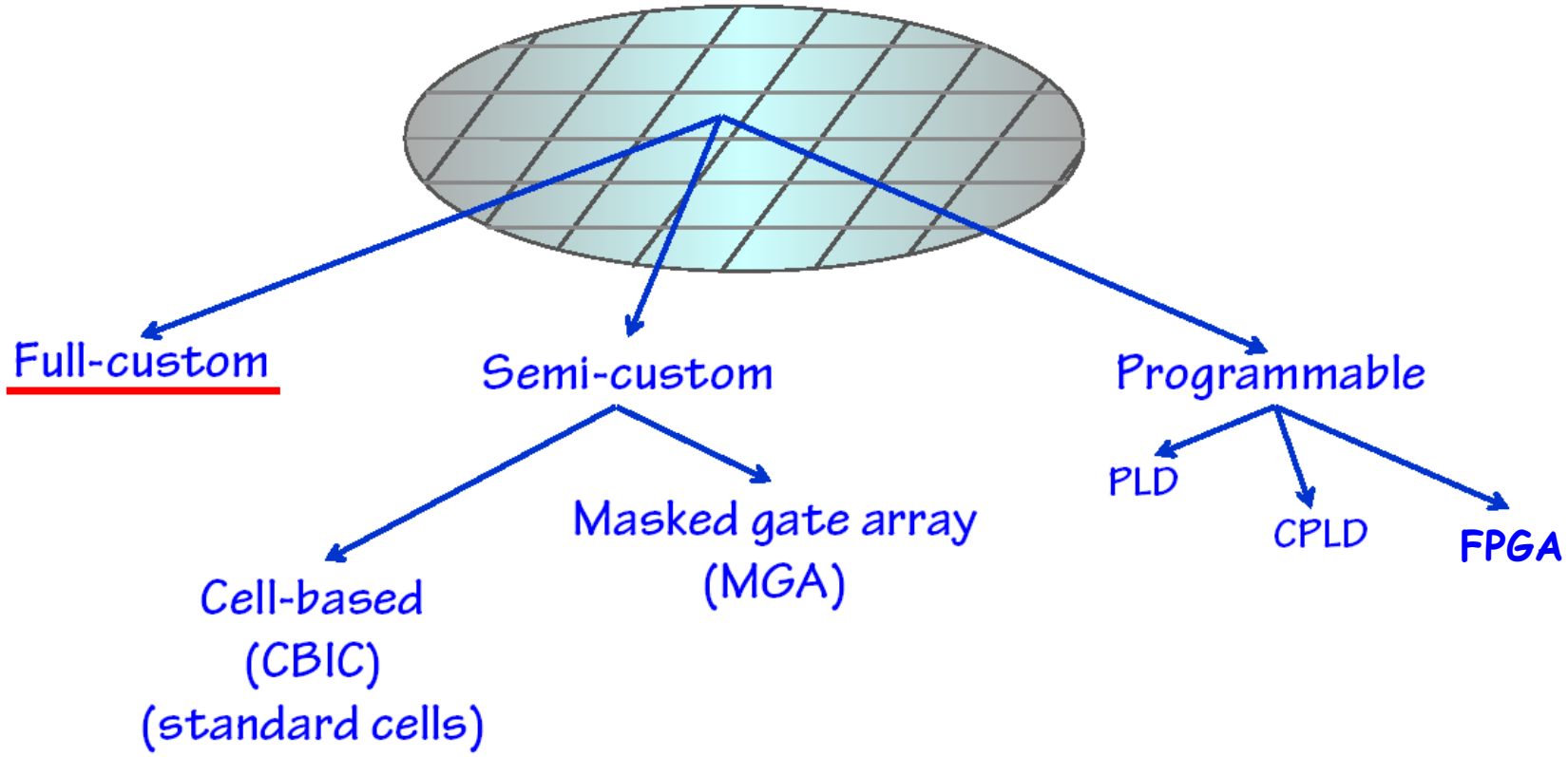


2-input MUX

DFF

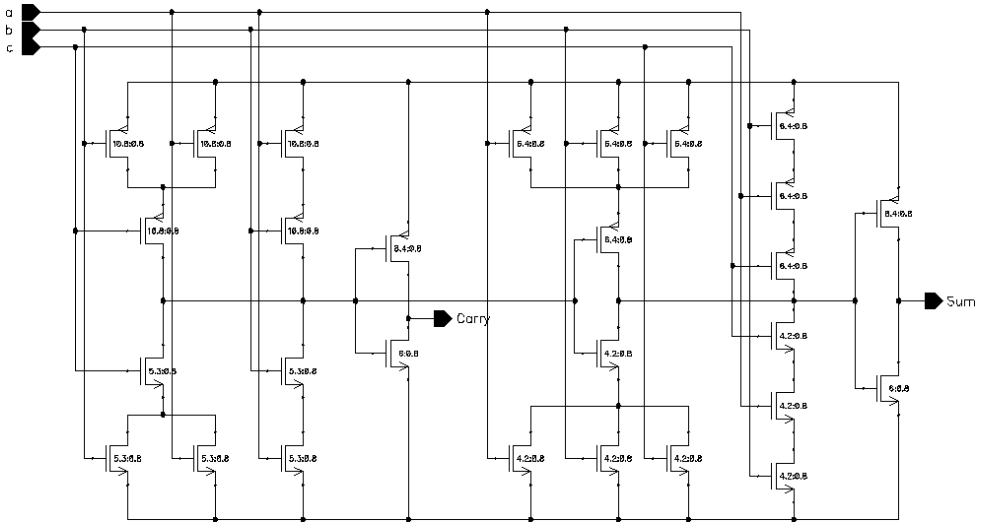


VLSI Design Styles

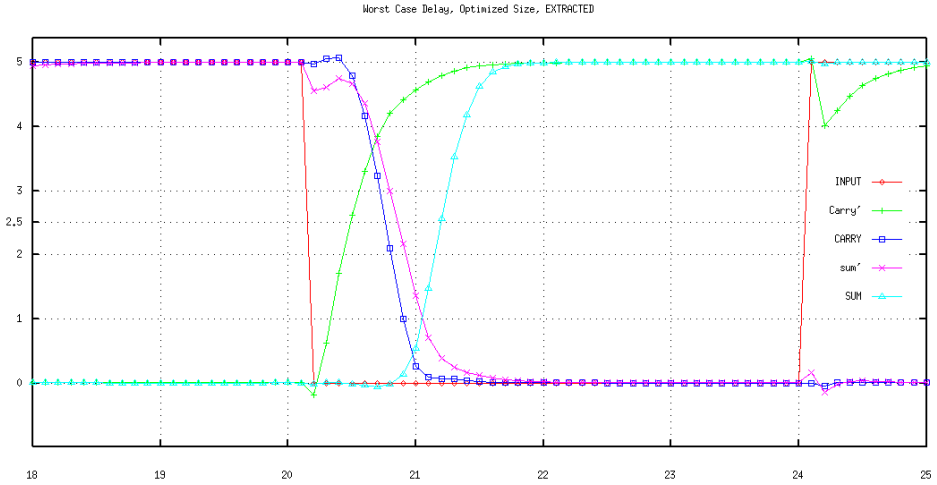


Full Custom Design

Following the partitioning, the transistor level design of the building block is generated and simulated.

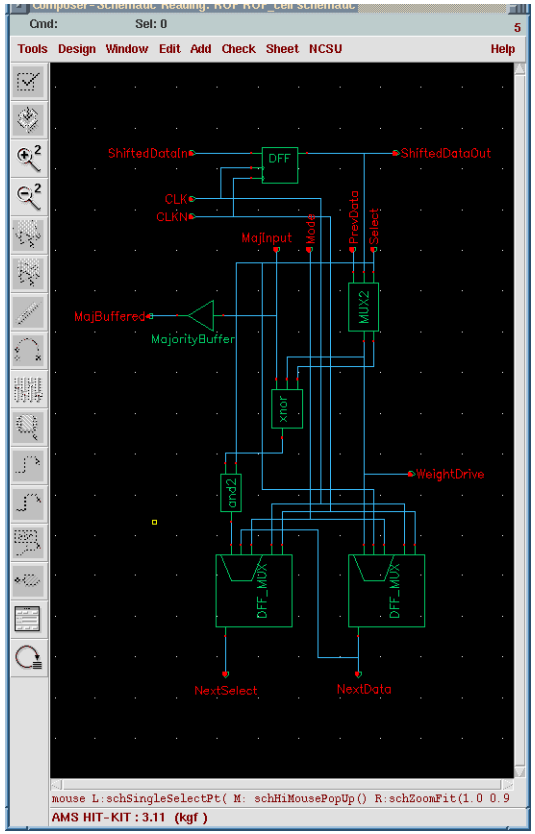


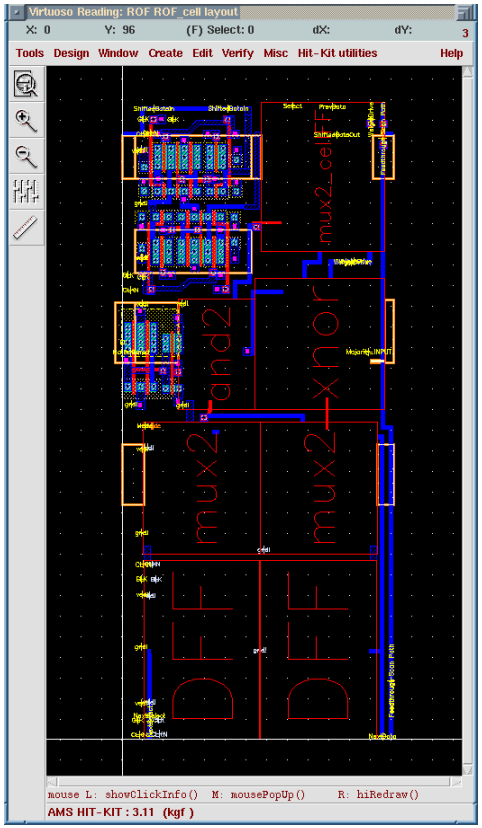
The example shows a 1-bit full-adder schematic and its SPICE simulation results.

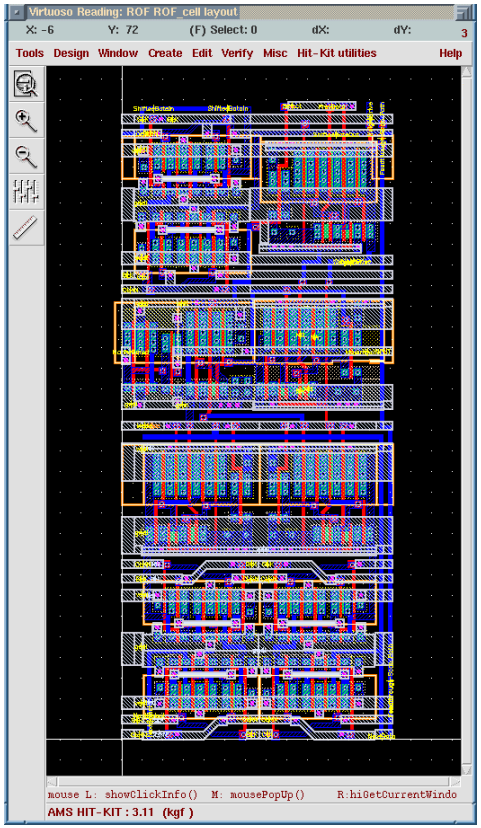


Full Custom Design

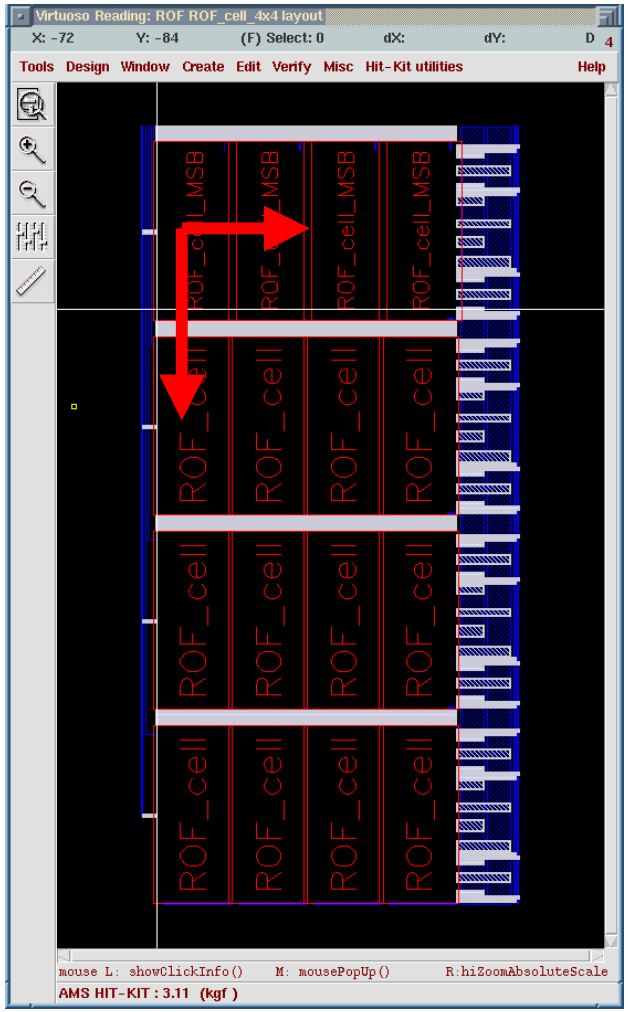
The main objective of full custom design is to ensure fine-grained regularity and modularity.







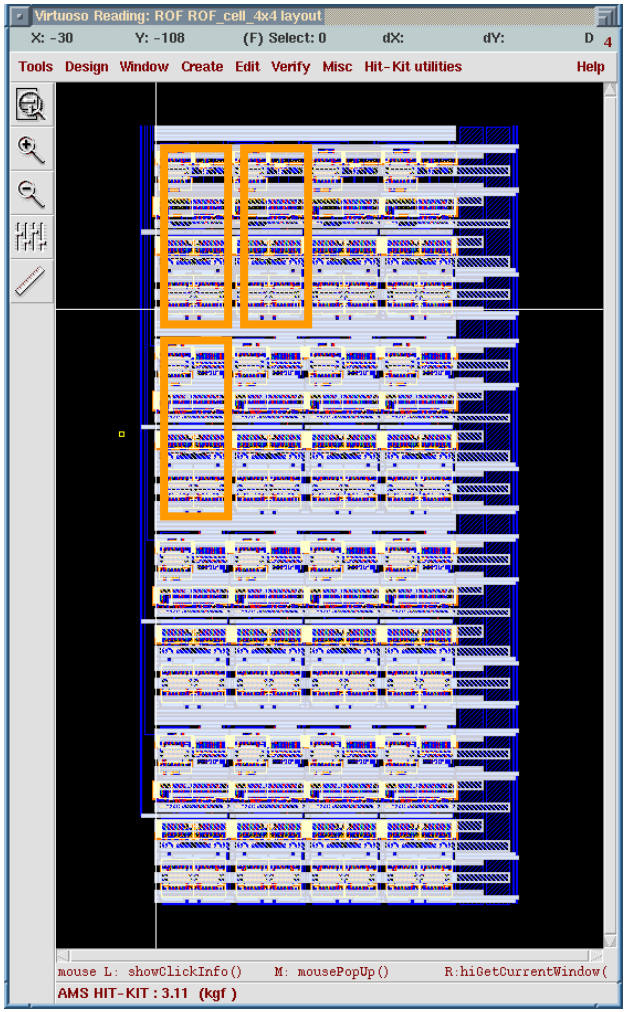
Full Custom Design



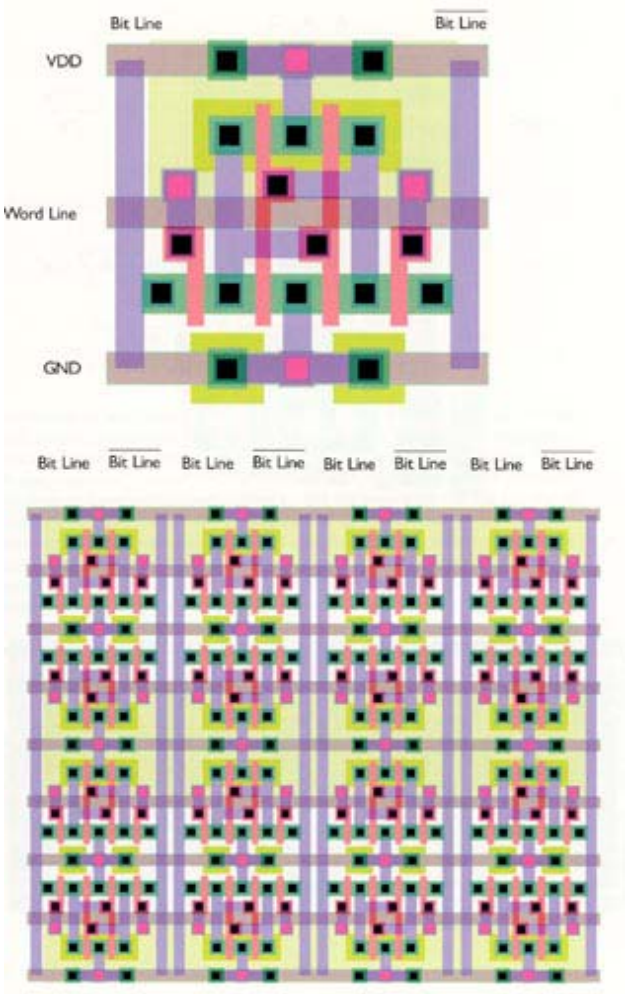
A carefully crafted full custom block can be placed both along the X and Y axis to form an interconnected two-dimensional array.

Example:

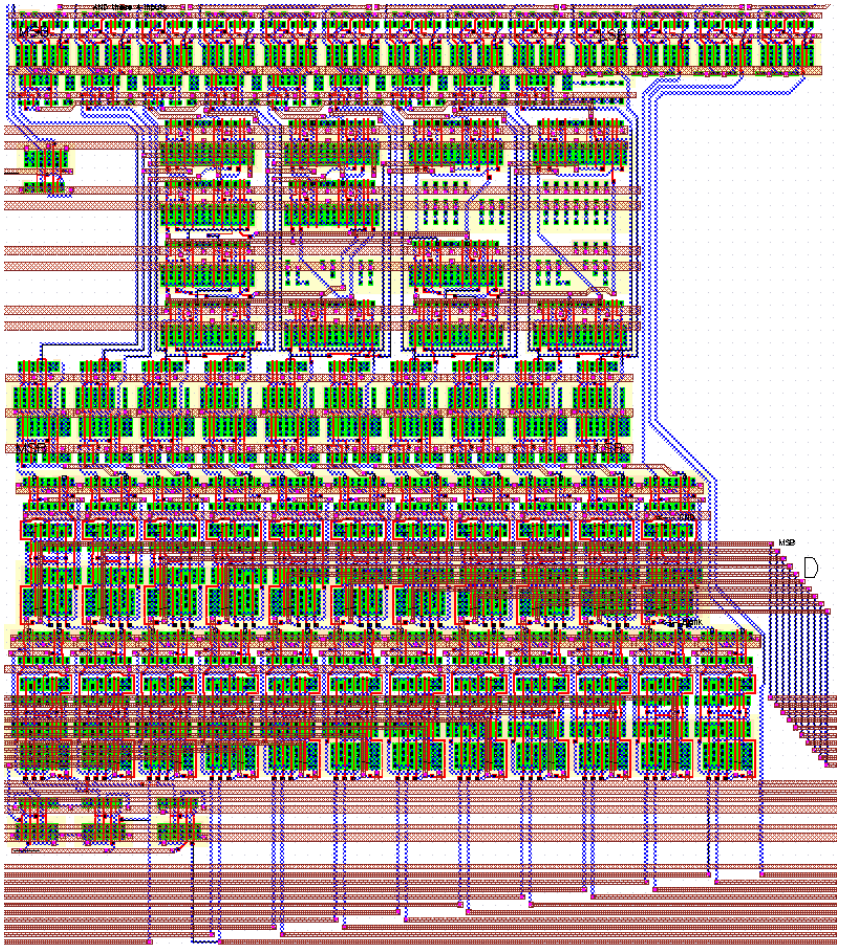
Data-path cells



Full Custom SRAM Cell Design

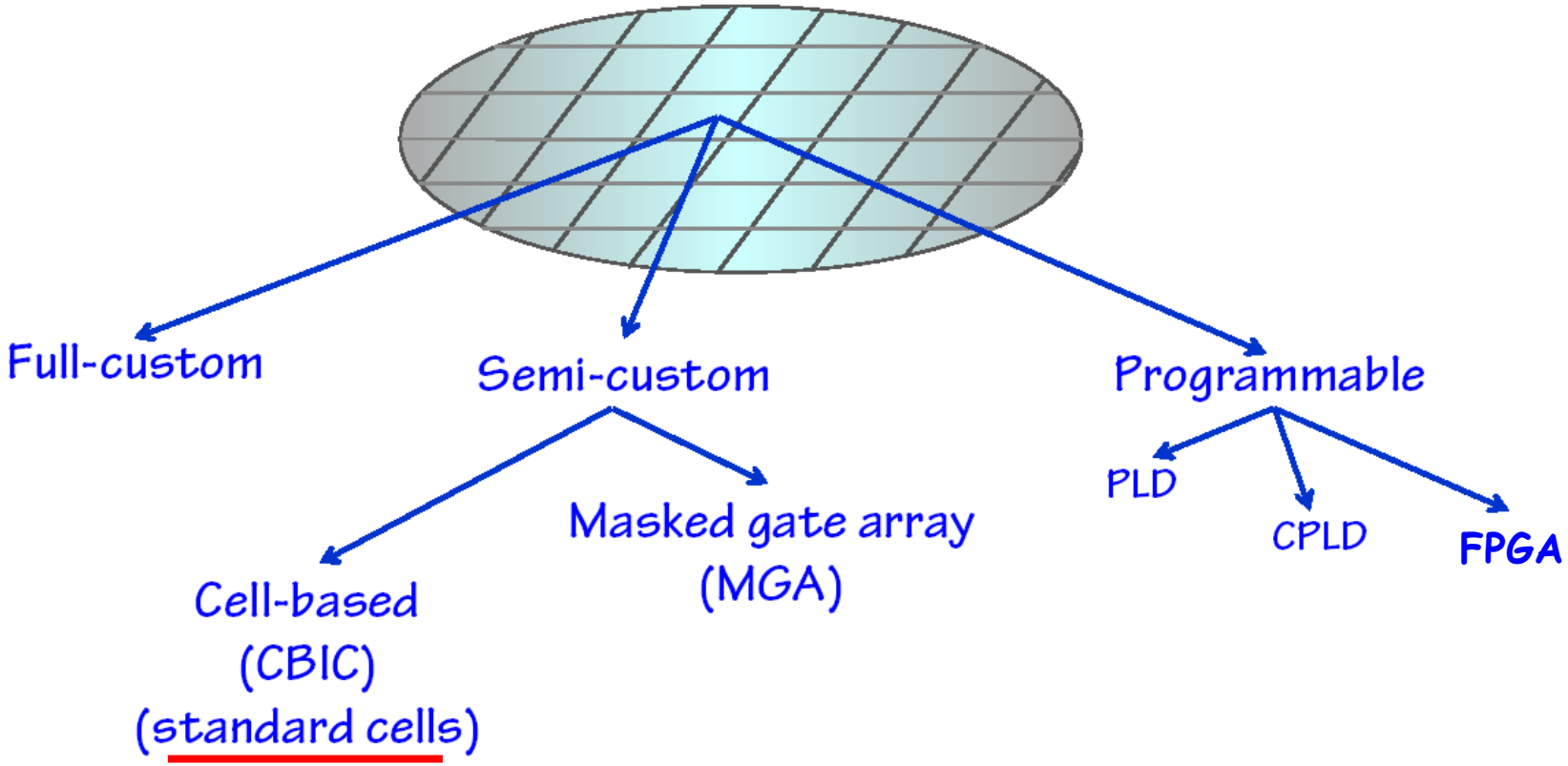


Mapping the Design into Layout



Manual full-custom design can be very challenging and time consuming, especially if the low level regularity is not well defined !

VLSI Design Styles



HDL-Based Design

1980's

Hardware Description Languages (HDL) were conceived to facilitate the information exchange between design groups.

1990's

The increasing computation power led to the introduction of logic synthesizers that can translate the description in HDL into a synthesized gate-level net-list of the design.

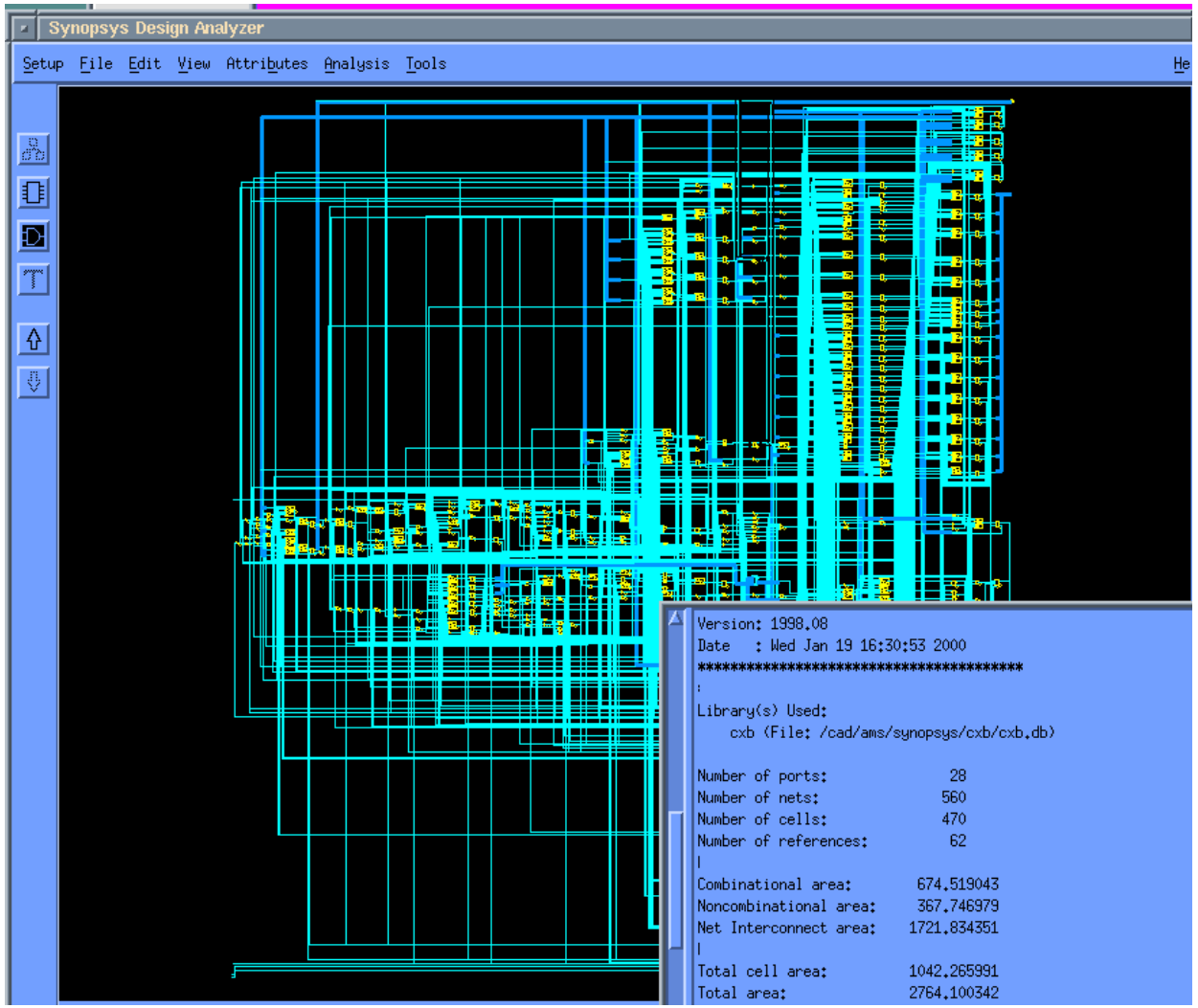
2000's

Modern synthesis algorithms can optimize a digital design and explore different alternatives to identify the design that best meets the requirements.

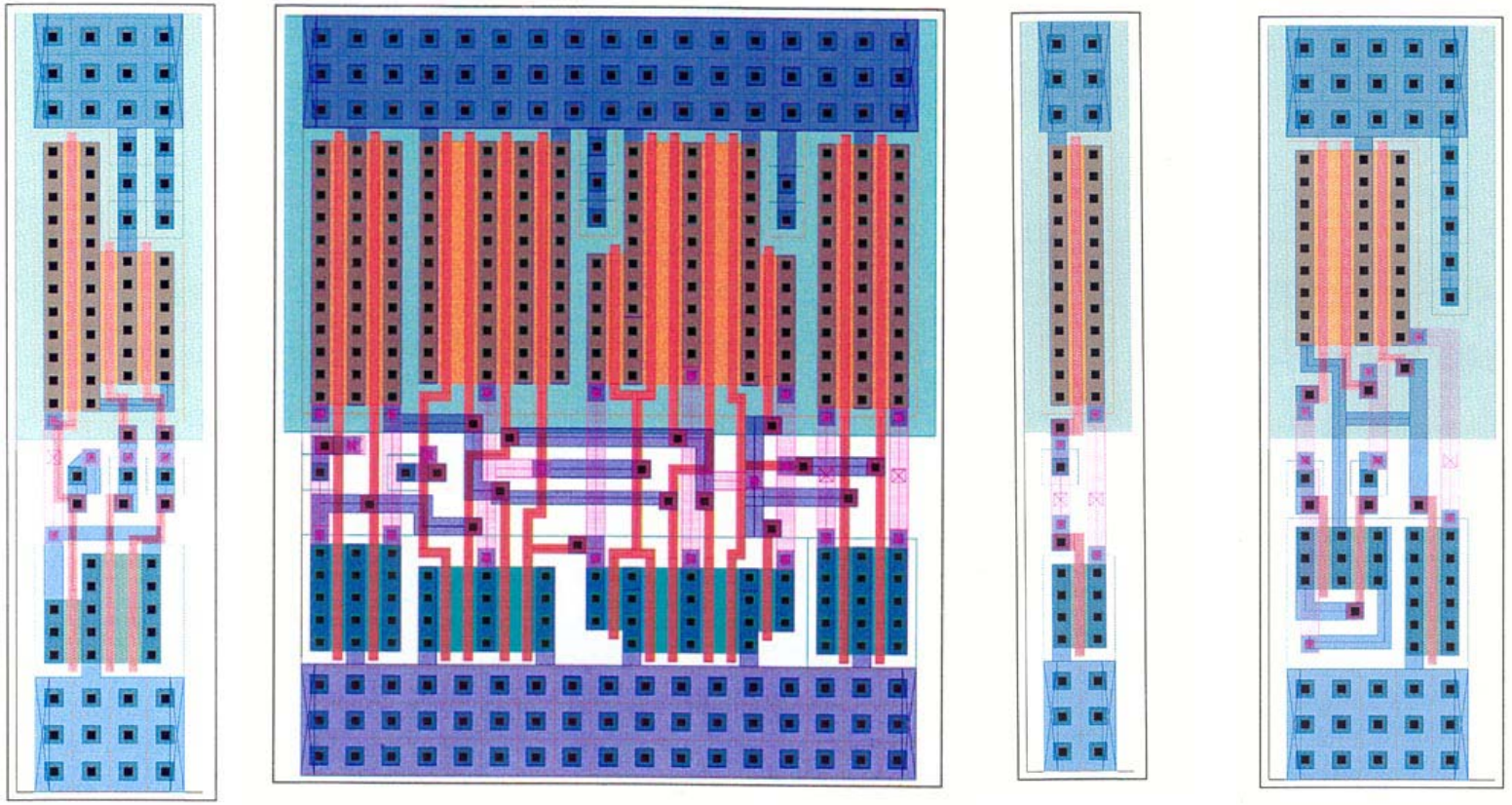
HDL-Based Design

The design is synthesized and mapped into the target technology.

The logic gates have one-to-one equivalents as standard cells in the target technology.

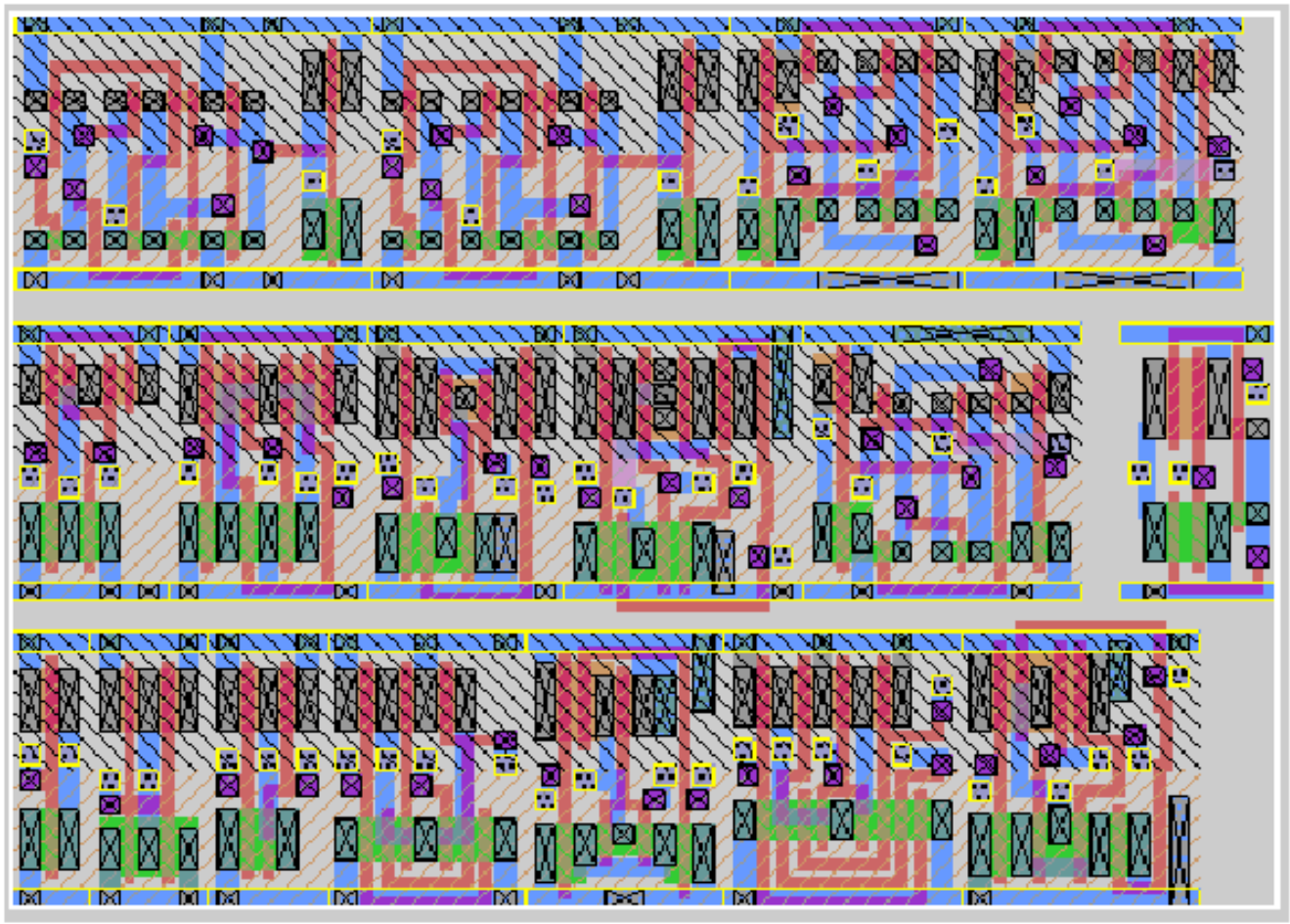


Standard Cells

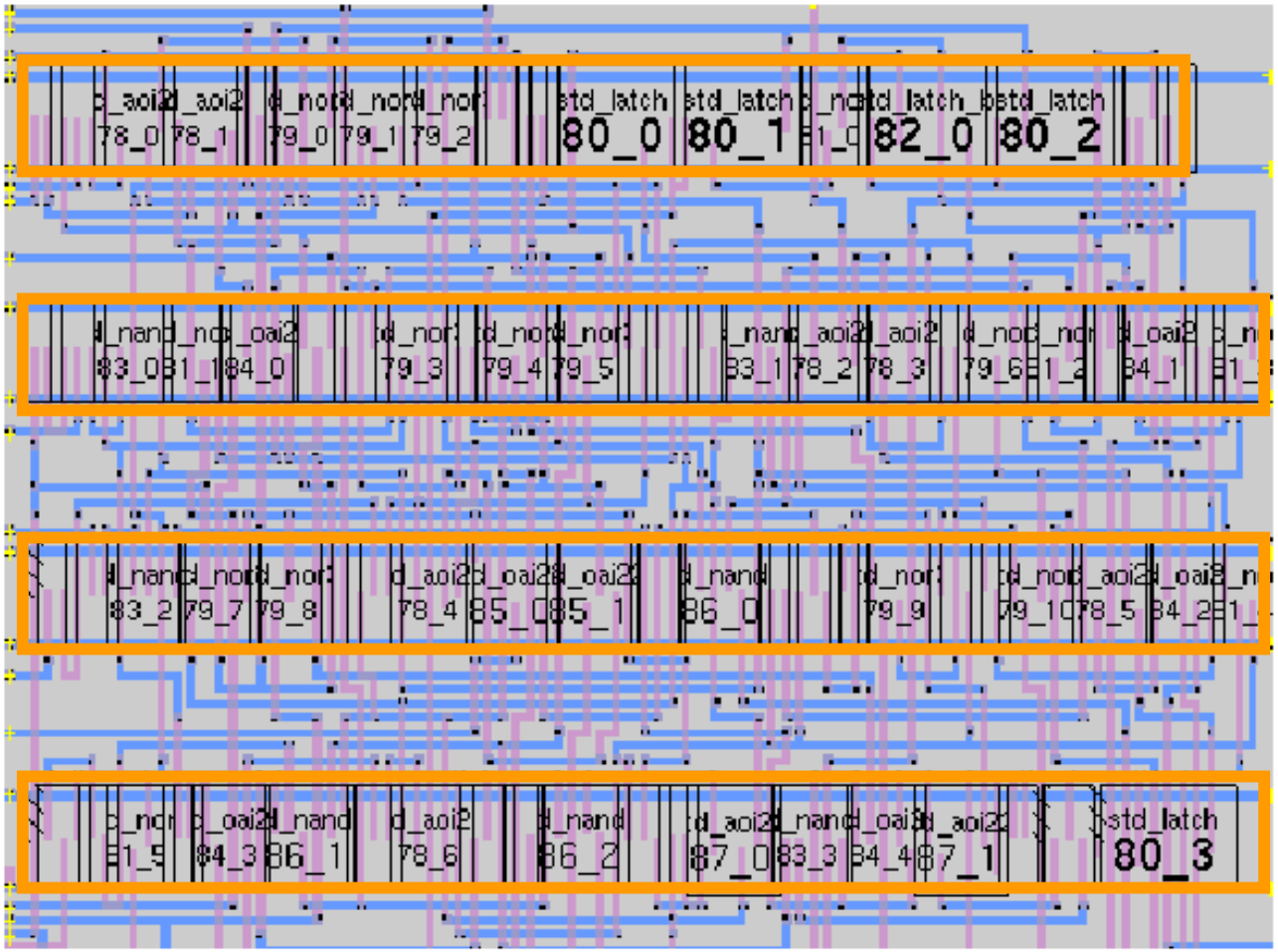


AND DFF INV XOR

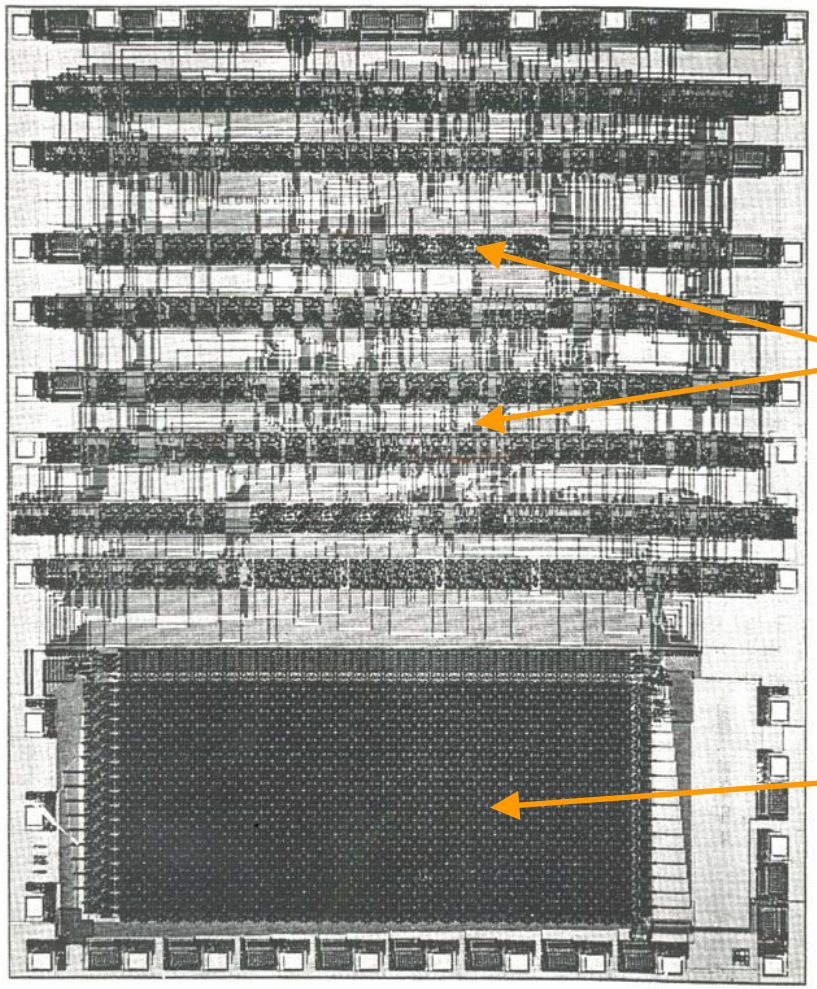
Standard Cells



Standard Cells



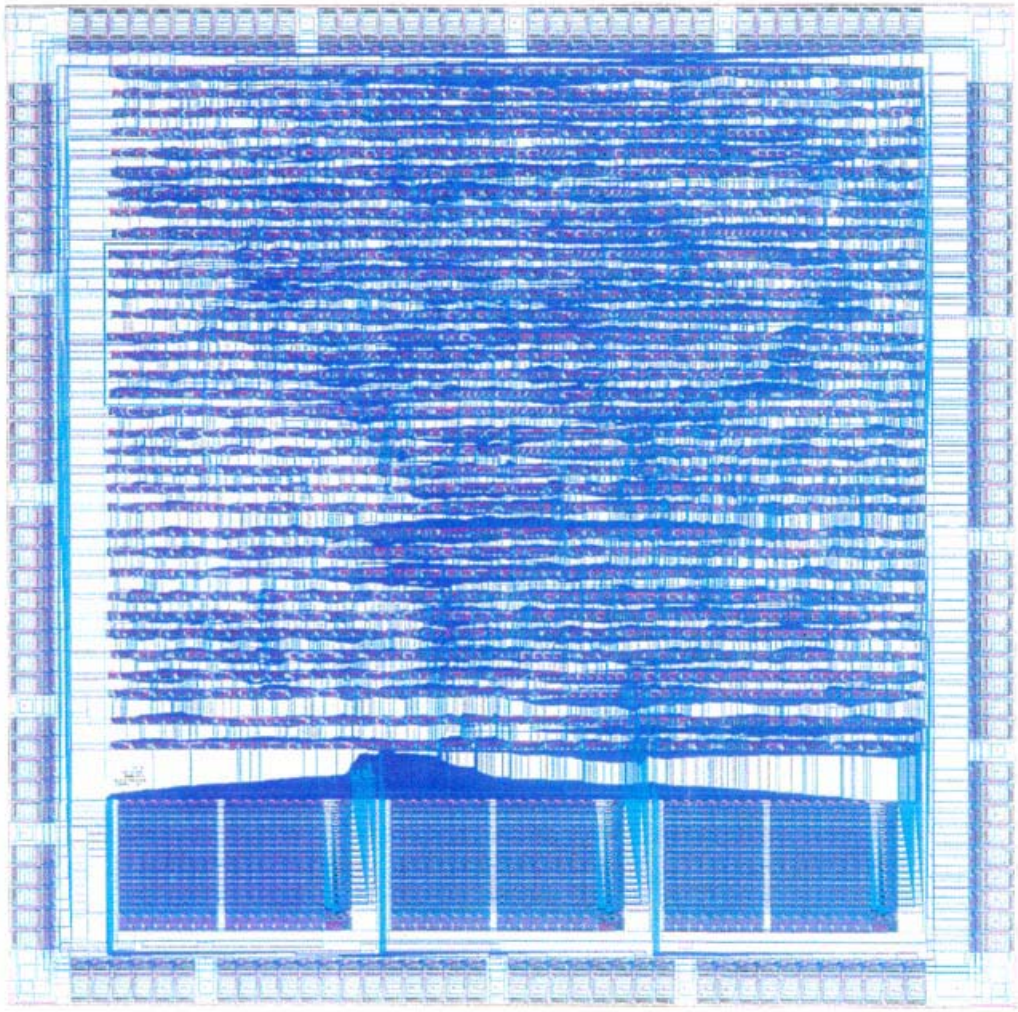
Standard Cells



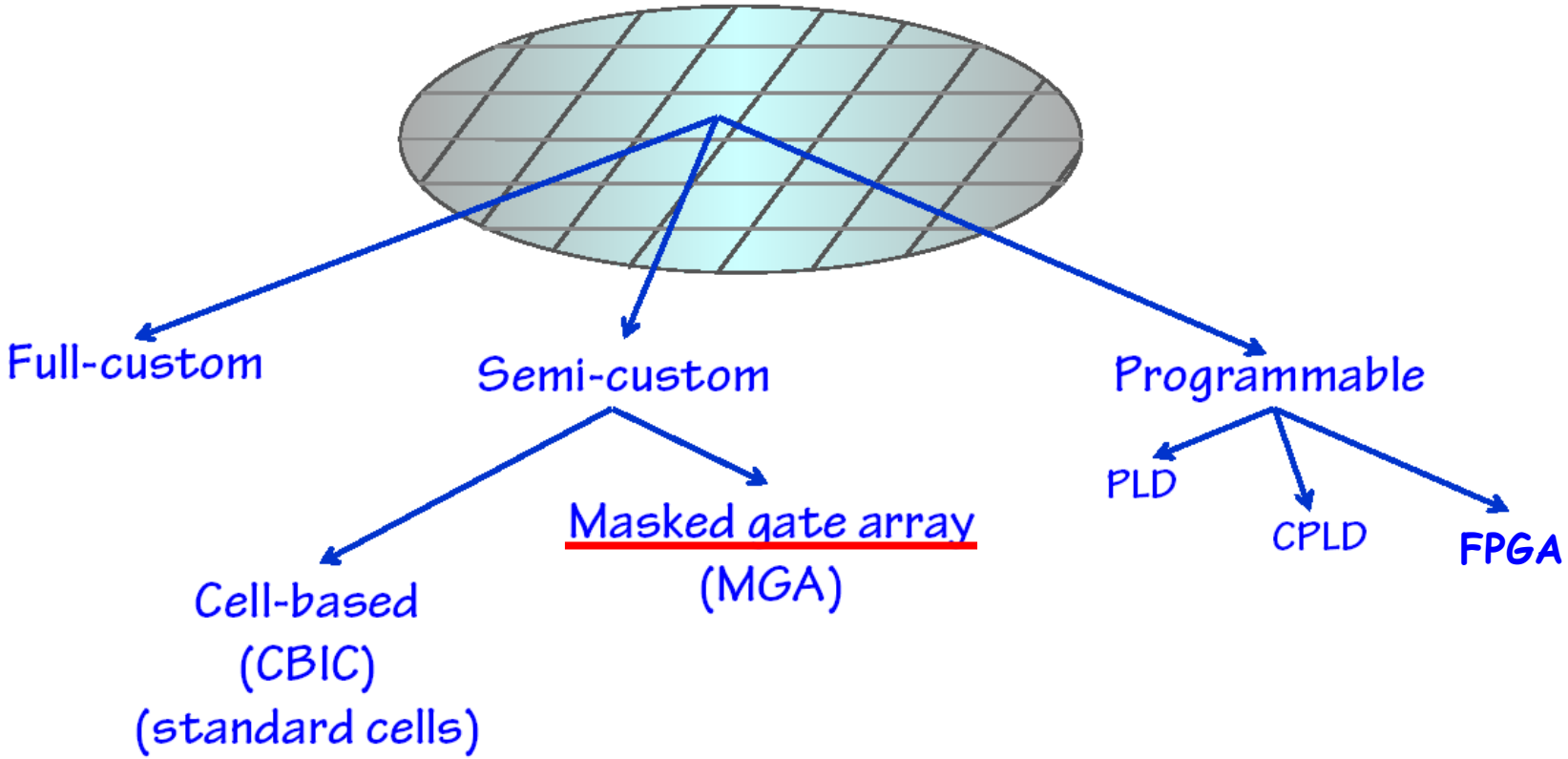
Rows of standard cells with routing channels between them

Memory array

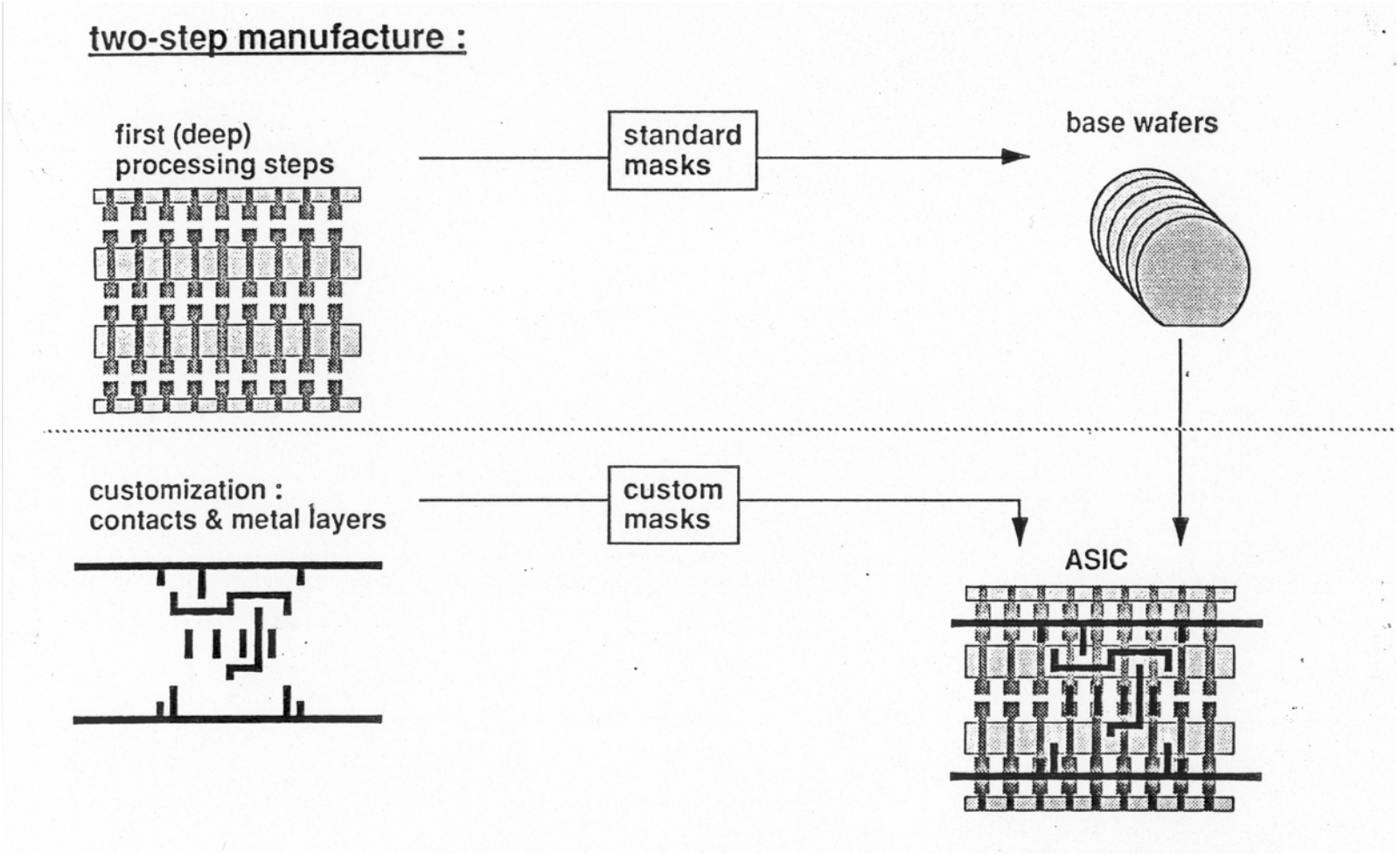
Standard Cells



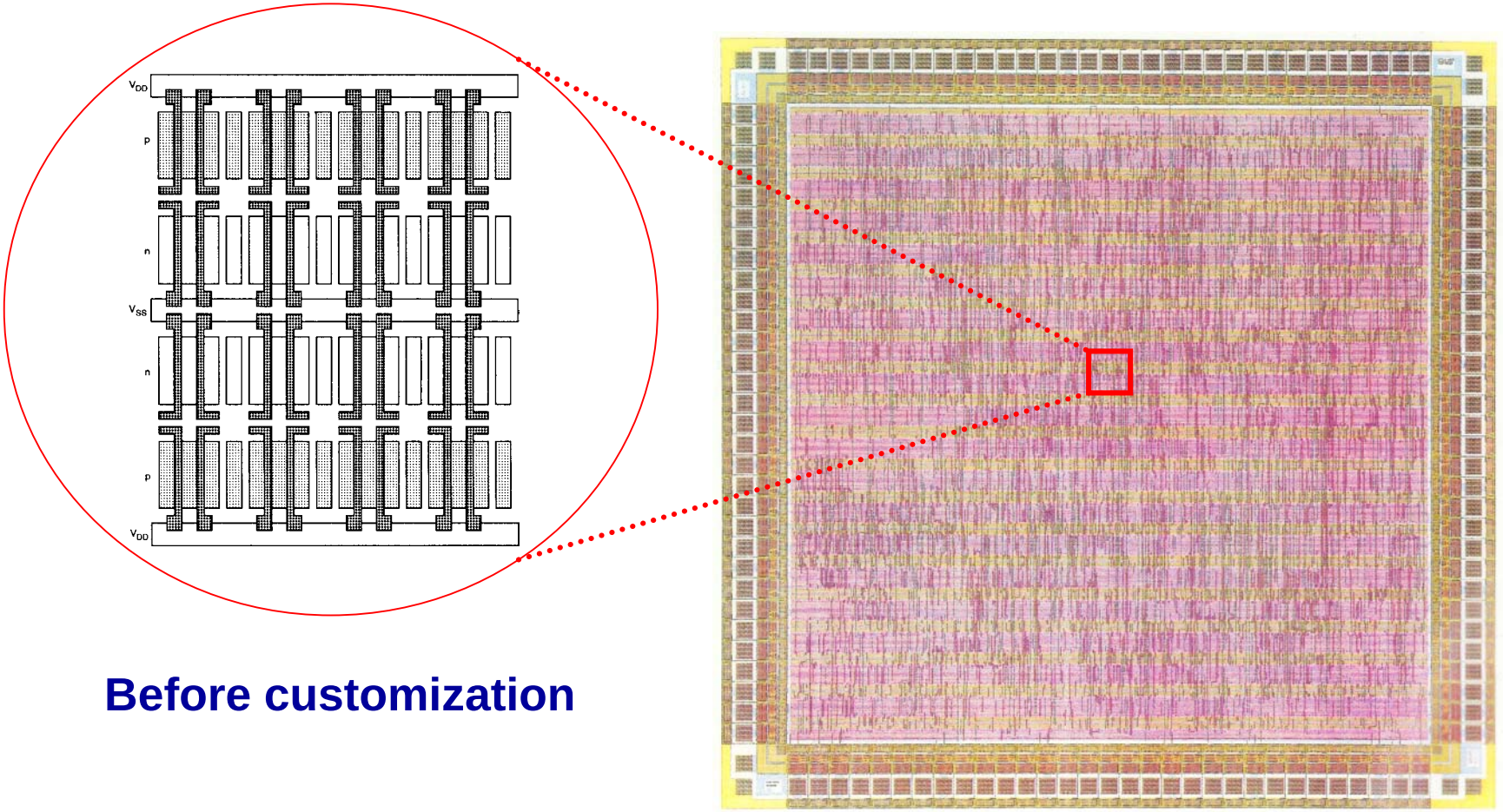
VLSI Design Styles



Mask Gate Array

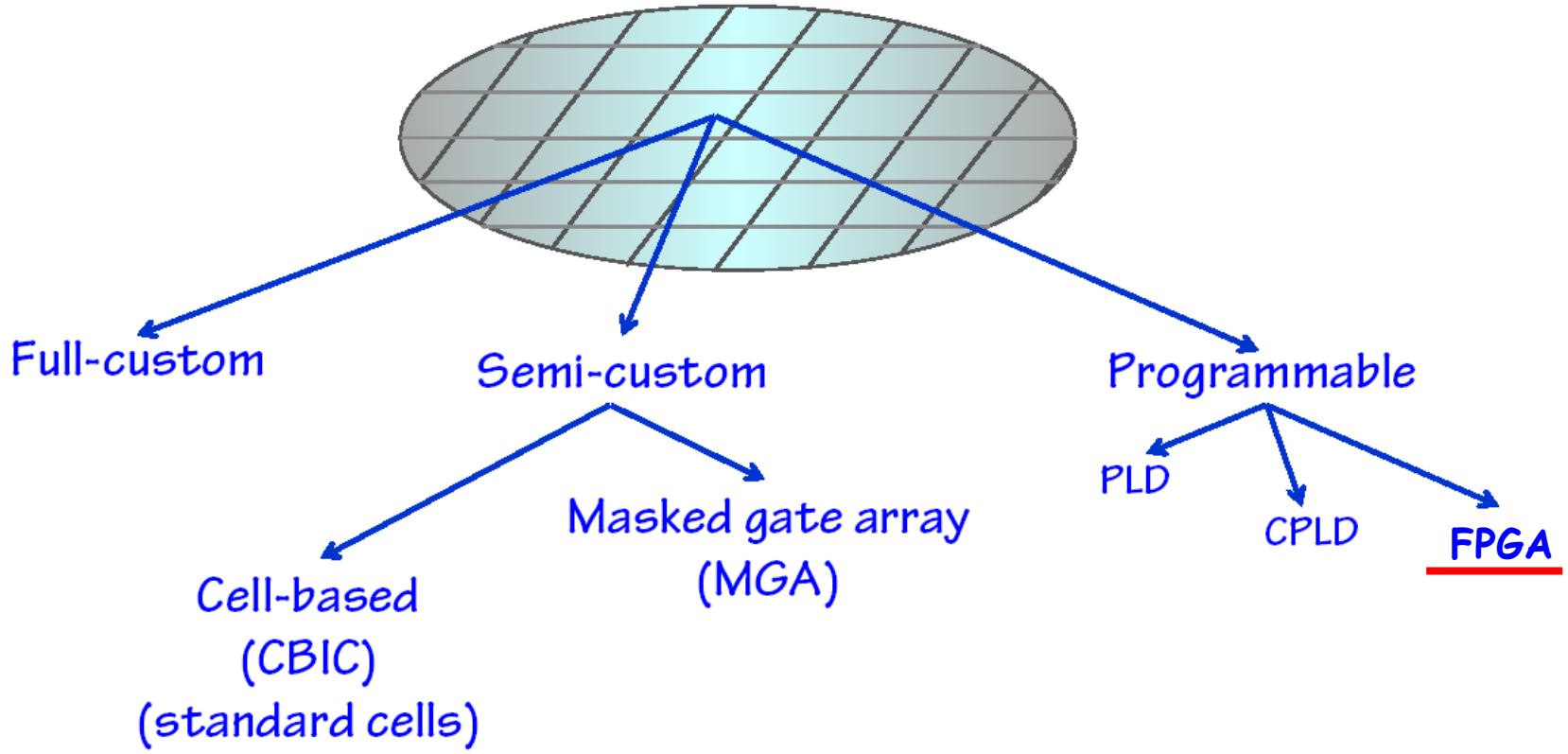


Mask Gate Array

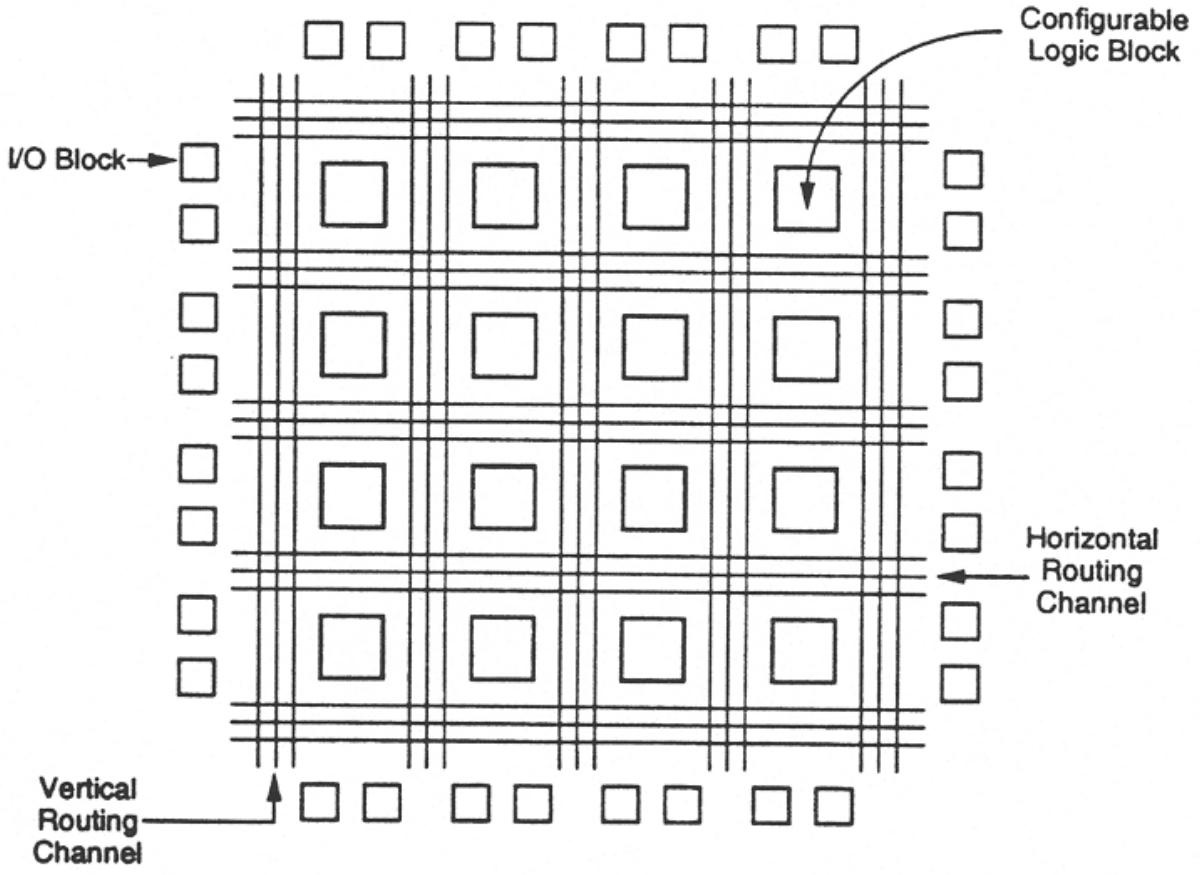


Before customization

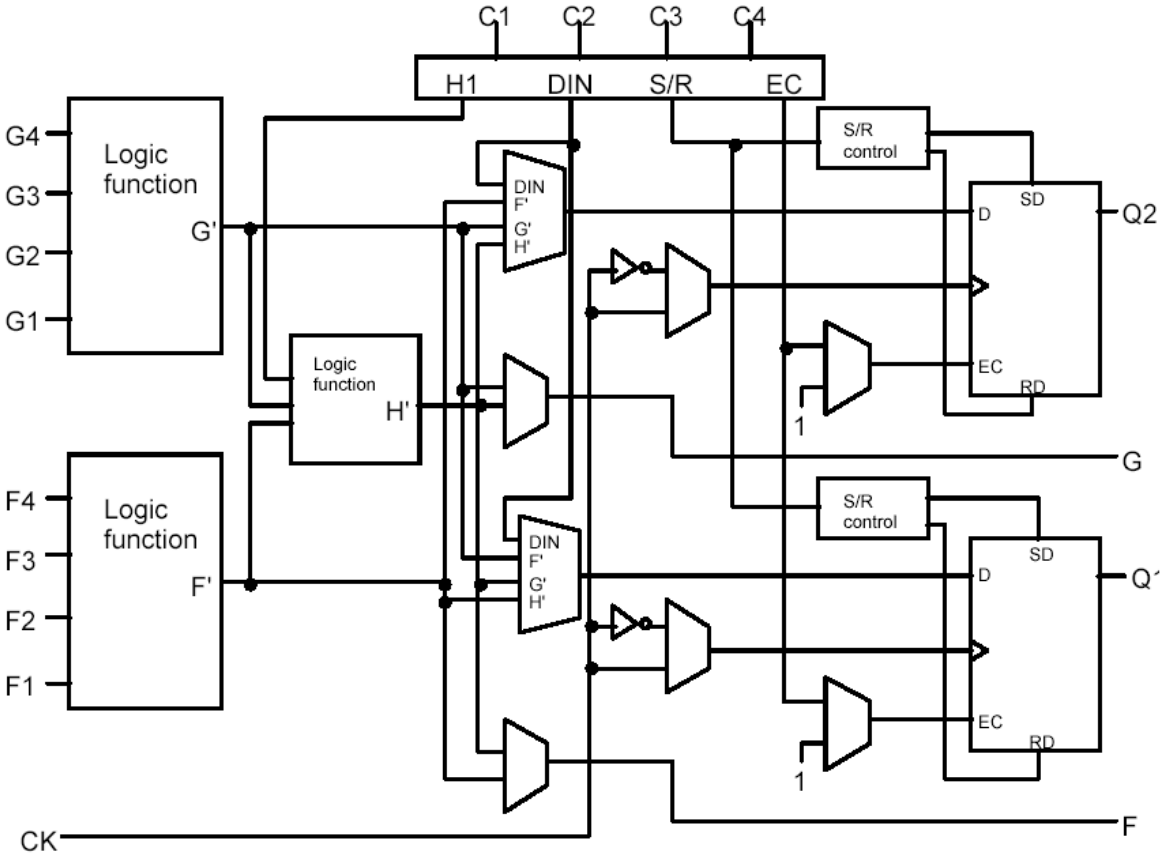
VLSI Design Styles



Field Programmable Gate Array



Field Programmable Gate Array



Internal structure of a CLB

Field Programmable Gate Array