CMOS

Digital Integrated Circuits

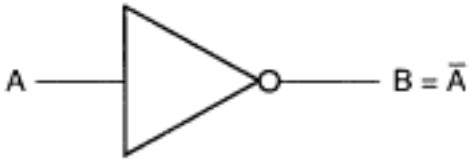
Analysis and Design

Chapter 5

MOS Inverters:

Static Characteristics

Introduction



Symbol

A	B
0	1
1	0

Truth Table

Figure 5.1 Logic symbol and truth table of the inverter.

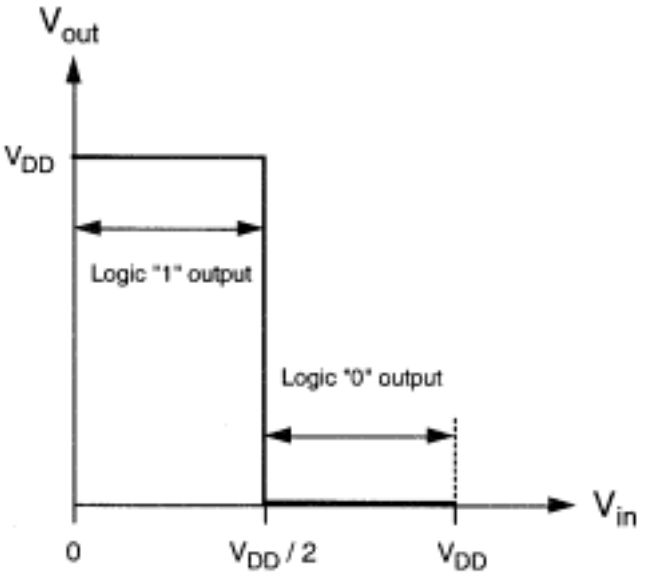


Figure 5.2 Voltage transfer characteristic (VTC) of the ideal inverter.

- Positive logic convention
  - "1" represents high voltage of V_{DD}
  - "0" represents low voltage of 0
- The inverter threshold voltage, V_{th}
  - The input voltage, $0<V_{in}<V_{th}$⇨output V_{DD}
  - The input voltage, $V_{th}<V_{in}<V_{DD}$⇨output 0

General circuit structure of an nMOS inverter

- The driver transistor
  - The input voltage $V_{in}=V_{GS}$
  - The output voltage $V_{out}=V_{DS}$
  - The source and the substrate are ground, $V_{SB}=0$
- The load device
  - Terminal current I_L, terminal voltage V_L

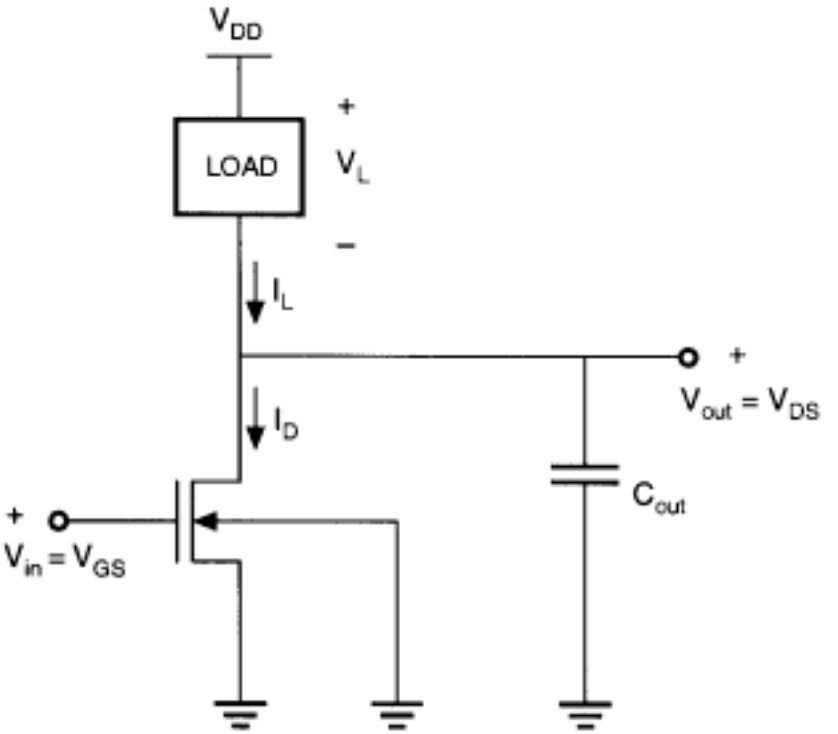


Figure 5.3 General circuit structure of an nMOS inverter.

Voltage transfer characteristic (VTC)

- The VTC describing V_{out} as a function of V_{in} under DC condition
- Very low voltage level
  - $V_{out}=V_{OH}$
  - nMOS off, no conducting current, voltage drop across the load is very small, the output voltage is high
- As V_{in} increases
  - The driver transistor starts conducting, the output voltage starts to decrease
  - The critical voltage point, $dV_{out}/dV_{in}=-1$
    - The input low voltage VIL
    - The input high voltage VIH
    - Determining the noise margins
- Further increase V_{in}
  - Output low voltage V_{OL}, when the input voltage is equal to V_{OH}
  - The inverter threshold voltage V_{th}
    - Define as the point where $V_{in}=V_{out}$

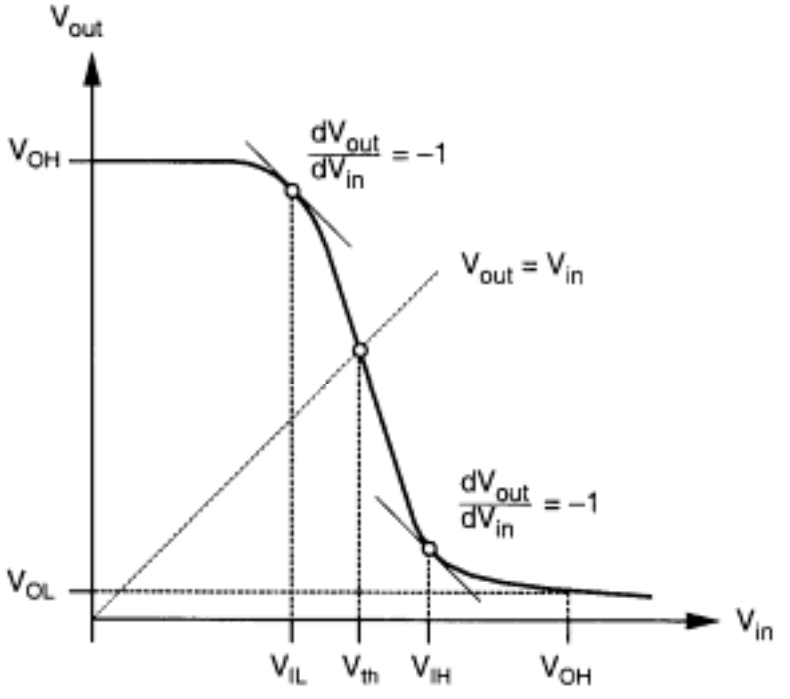


Figure 5.4 Typical voltage transfer characteristic (VTC) of a realistic nMOS inverter.

Noise immunity and noise margin

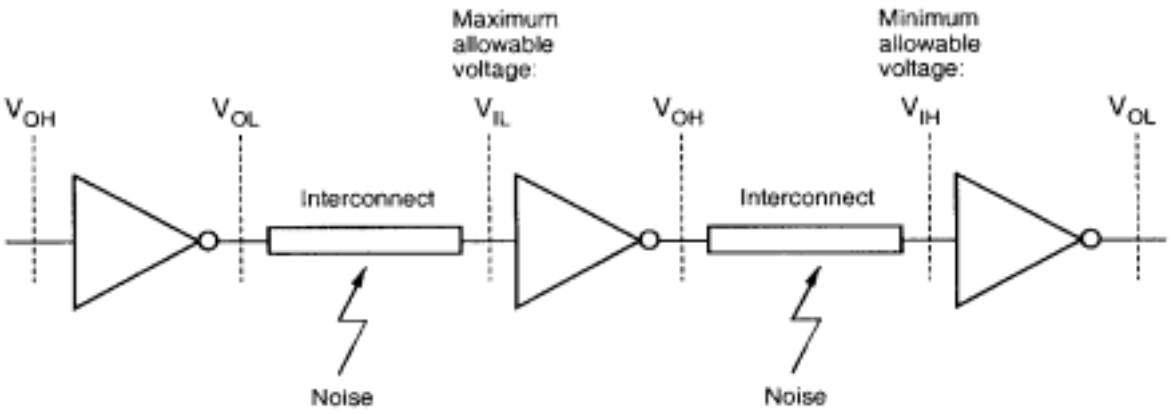


Figure 5.5 Propagation of digital signals under the influence of noise.

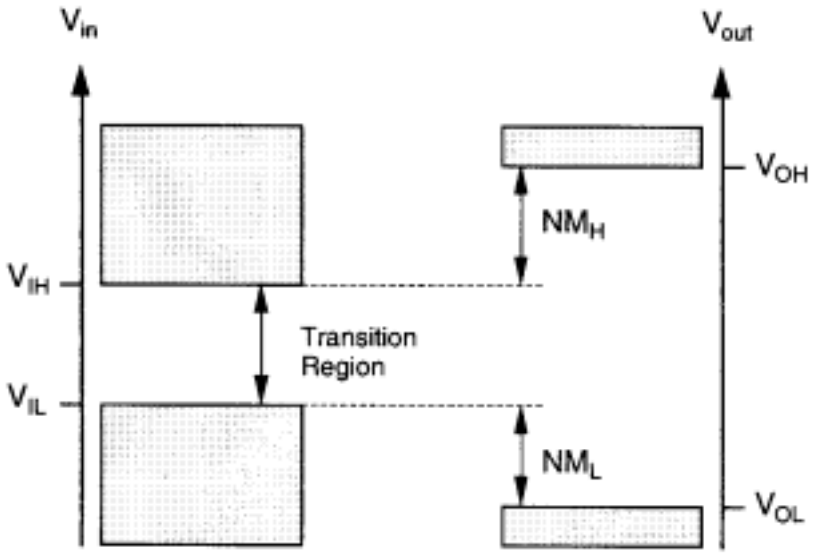


Figure 5.6 Definition of noise margins NM_L and NM_H. Note that the shaded regions indicate valid high and low levels for the input and output signals.

- $N_{ML}=V_{IL}-V_{OL}$
- $N_{MH}=V_{OH}-V_{IH}$
- The transition region, uncertain region

Power and area consideration

- The DC power dissipation
  - The product of its power supply voltage and the amount of current down from the power supply during steady state or in standby mode
  - $P_{DC}=V_{DD}I_{DC}=(V_{DD}/2)[I_{DC}(V_{in}=low)+I_{DC}(V_{in}=high)]$
  - In deep submicron technologies
    - Subthreshold current ⇨more power consumption
- The chip area
  - To reduce the area of the MOS transistor
    - The gate area of the MOS transistor
    - The product of W and L

Resistive-load inverter

Input Voltage Range	Operating Mode
$V_{in} < V_{T0}$	cut-off
$V_{T0} \le V_{in} < V_{out} + V_{T0}$	saturation
$V_{in} \ge V_{out} + V_{T0}$	linear

- Operation mode
  - $V_{in}<V_{T0}$, cut off
    - No current, no voltage drop across the load resistor
    - $V_{out}=V_{DD}$
  - $V_{T0}\le V_{in}<V_{out}+V_{T0}$, saturation
    - Initially, $V_{DS}>V_{in}-V_{T0}$
    - $I_R = \frac{k_n}{2}\cdot(V_{in}-V_{T0})^2$
    - With $V_{in}\uparrow \Rightarrow V_{out}\downarrow$
  - $V_{in}\ge V_{out}+V_{T0}$, linear
    - The output voltage continues to decrease
    - $I_R = \frac{k_n}{2}\cdot\left[2\cdot(V_{in}-V_{T0})\cdot V_{out}-V_{out}^2\right]$

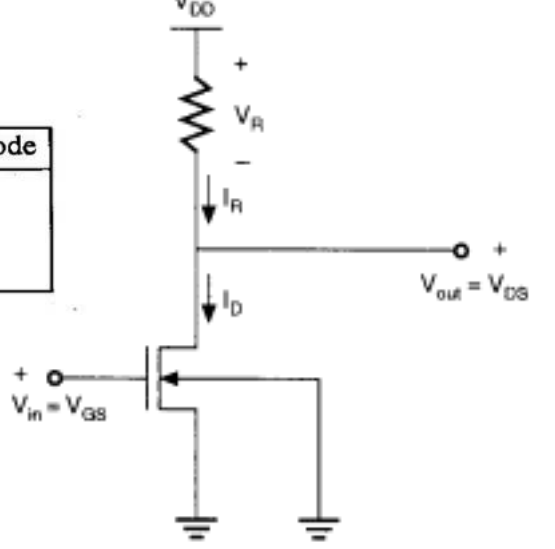


Figure 5.7 Resistive-load inverter circuit

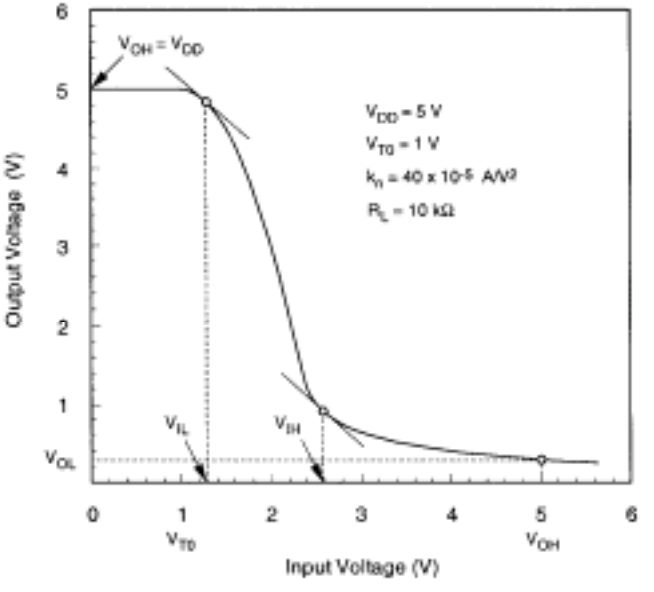


Figure 5.8 Typical VTC of a resistive-load inverter circuit. Important design parameters of the circuit are shown in the inset.

Calculation of V_{OH}, V_{OL}

- Calculation of V_{OH}
  - $V_{out}=V_{DD}-R_L I_R$
  - When V_{in} is low $\Rightarrow I_D=I_R=0 \Rightarrow V_{OH}=V_{DD}$
- Calculation of V_{OL}
  - Assume the input voltage is equal to V_{OH}
  - $V_{in}-V_{T0} \geq V_{out} \Rightarrow$ linear region
  - $$I_R = \frac{V_{DD}-V_{out}}{R_L}$$

    Using KCL for the output node, i.e. $I_R = I_D$

    $$\frac{V_{DD}-V_{OL}}{R_L} = \frac{k_n}{2}\cdot\left[2\cdot(V_{DD}-V_{T0})\cdot V_{0L}-V_{0L}^2\right]$$

    $$V_{0L}^2 - 2\cdot\left(V_{DD}-V_{T0}+\frac{1}{k_n R_L}\right)\cdot V_{0L} + \frac{2}{k_n R_L}\cdot V_{DD} = 0$$

    $$V_{0L} = V_{DD}-V_{T0}+\frac{1}{k_n R_L} - \sqrt{\left(V_{DD}-V_{T0}+\frac{1}{k_n R_L}\right)^2 - \frac{2V_{DD}}{k_n R_L}}$$

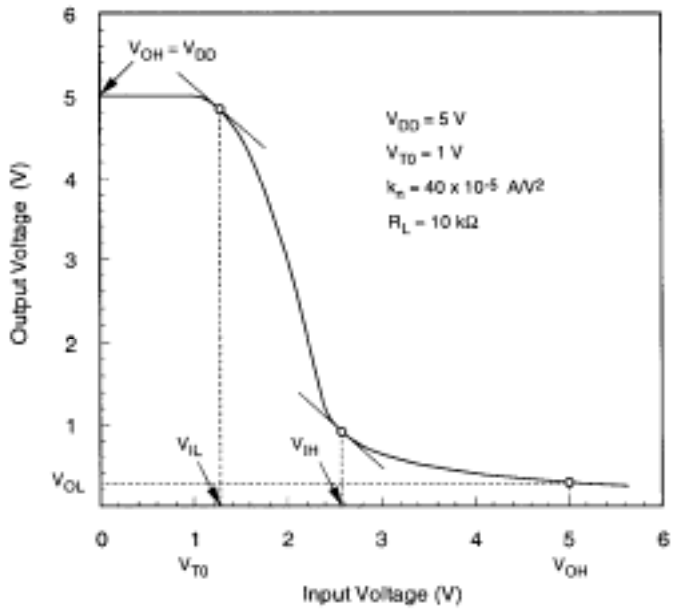


Figure 5.8 Typical VTC of a resistive-load inverter circuit. Important design parameters of the circuit are shown in the inset.

Calculation of V_{IL}, and V_{IH}

By definition, V_{IL} is the smaller of the two input voltage at which the slope of the VTC becomes equal to -1. i.e. $dV_{out}/dV_{in} = -1$

$V_{out} > V_{in} - V_{T0}$, saturation region

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2$$

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = k_n \cdot (V_{in} - V_{T0}) \Rightarrow -\frac{1}{R_L} \cdot (-1) = k_n \cdot (V_{in} - V_{T0})$$

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L}$$

$$V_{out}(V_{in} = V_{IL}) = V_{DD} - \frac{k_n R_L}{2} \cdot \left(V_{T0} + \frac{1}{k_n R_L} - V_{T0} \right)^2 = VDD - \frac{1}{2 k_n R_L}$$

V_{IH} is the larger of the two voltage points on the VTC at which the slope is equal to -1

$V_{out} < V_{in} - V_{TO}$, linear region

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot \left[2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - V_{out}^2 \right]$$

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = \frac{k_n}{2} \cdot \left[2 \cdot (V_{in} - V_{T0}) \cdot \frac{dV_{out}}{dV_{in}} - 2V_{out} \cdot \frac{dV_{out}}{dV_{in}} \right]$$

$$-\frac{1}{R_L} \cdot (-1) = k_n \cdot \left[(V_{in} - V_{T0}) \cdot (-1) + 2V_{out} \right]$$

$$V_{IH} = V_{T0} + 2V_{out} - \frac{1}{k_n R_L}$$

To determine the unknown variables

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \cdot \left[2 \cdot \left(V_{T0} + 2V_{out} - \frac{1}{k_n R_L} - V_{T0} \right) \cdot V_{out} - V_{out}^2 \right]$$

$$V_{out}(V_{in} = V_{IH}) = \sqrt{\frac{2}{3} \cdot \frac{V_{DD}}{k_n R_L}}$$

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}$$

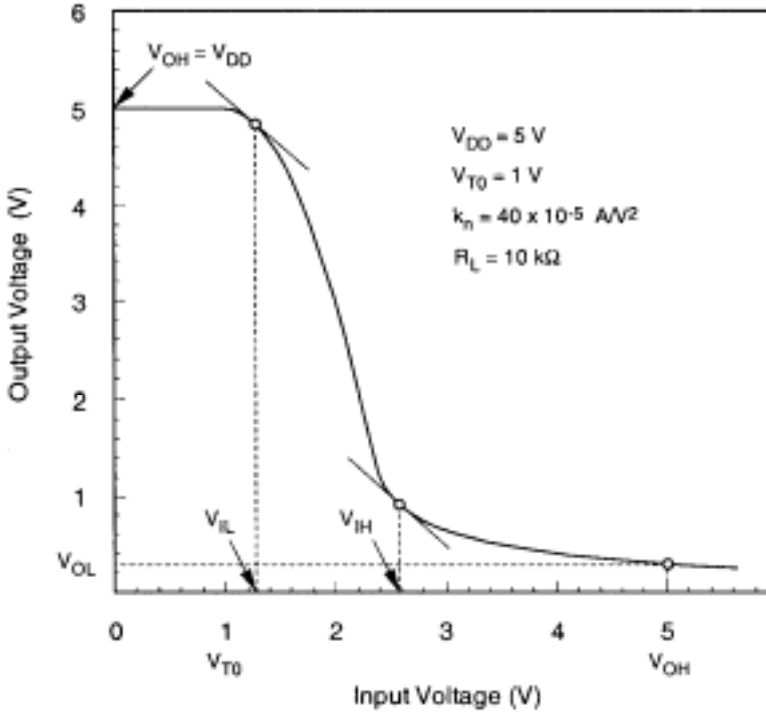


Figure 5.8 Typical VTC of a resistive-load inverter circuit. Important design parameters of the circuit are shown in the inset.

VTC for different k_nR_L

- The term k_nR_L plays an important role in determining the shape of the voltage transfer characteristic
- k_nR_L appears as a critical parameter in expressions for V_{OL}, V_{IL}, and V_{IH}
- k_nR_L can be adjusted by circuit designer
- V_{OH} is determine primarily by the power supply voltage, V_{DD}
- The adjustment of V_{OL} receives primarily attention than V_{IL}, V_{IH}
- Larger $k_nRL \Rightarrow V_{OL}$ becomes smaller, larger transition slope

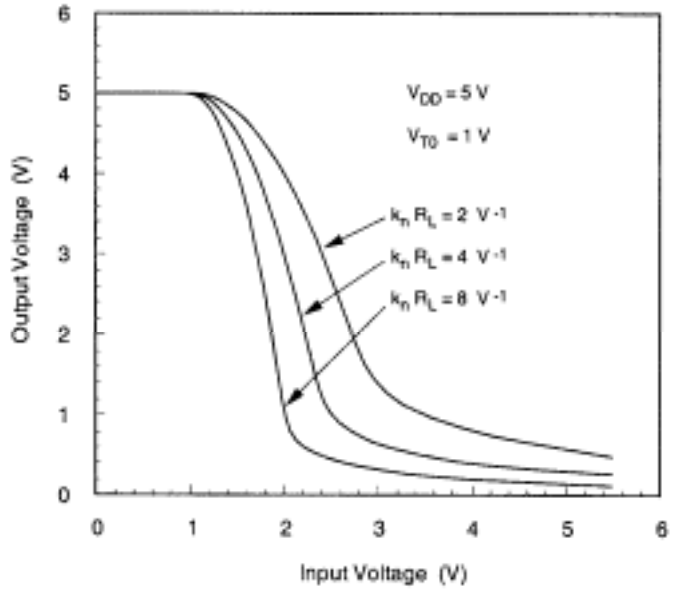


Figure 5.9 Voltage transfer characteristics of the resistive-load inverter, for different values of the parameter (k_nR_L).

Example 5.1

Consider the following inverter design problem: Given $V_{DD} = 5\,\text{V}$, $k_n' = 30\,\mu\text{A/V}^2$, and $V_{T0} = 1\,\text{V}$, design a resistive-load inverter circuit with $V_{OL} = 0.2\,\text{V}$. Specifically, determine the (W/L) ratio of the driver transistor and the value of the load resistor R_L that achieve the required V_{OL}.

In order to satisfy the design specification on the output low voltage V_{OL}, we start our design by writing the relevant current equation. Note that the driver transistor is operating in the linear region when the output voltage is equal to V_{OL} and the input voltage is equal to $V_{OH} = V_{DD}$.

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{OH} - V_{T0}) \cdot V_{OL} - V_{OL}^2\right]$$

Assuming $V_{OL} = 0.2\,\text{V}$ and using the given values for the power supply voltage, the driver threshold voltage and the driver transconductance k_n', we obtain the following equation:

$$\frac{5 - 0.20}{R_L} = \frac{30 \times 10^{-6}}{2} \cdot \frac{W}{L} \cdot (2 \cdot 4 \cdot 0.20 - 0.20^2)$$

This equation can be rewritten as:

$$\frac{W}{L} \cdot R_L = 2.05 \times 10^5\ \Omega$$

At this point, we recognize that the designer has a choice of different (W/L) and R_L values, all of which satisfy the given design specification, $V_{OL} = 0.2\,\text{V}$. The selection of the pair of values to use for (W/L) and R_L in the final design ultimately depends on other considerations, such as the power consumption of the circuit and the silicon area. The next table lists some of the design possibilities, along with the average DC power consumption estimated for each design.

$\left(\frac{W}{L}\right)$ – Ratio	Load resistor R_L[kΩ]	DC power consumption $P_{DC,average}$ [μW]
1	205.0	58.5
2	102.5	117.1
3	68.4	175.4
4	51.3	233.9
5	41.0	292.7
6	34.2	350.8

It is seen that the power consumption increases significantly as the value of the l
resistor R_L is decreased, and the (W/L) ratio is increased. If lowering the DC po
consumption is the overriding concern, we may choose a small (W/L) ratio ar
large load resistor. On the other hand, if the fabrication of the large load resistor
quires a large silicon area, a clear trade-off exists between the DC power dissipat
and the area occupied by the inverter circuit.

Power consumption

- The average power consumption
  - When input low, V_{OL}
    - The driver cut-off, no steady-state current flow, DC power consumption is zero
  - When input high, V_{OH}
    - Both driver MOSFET and the load resistor conduct a nonzero current
    - The output voltage V_{OL}, so the current $I_D=I_R=(V_{DD}-V_{OL})/R_L$
  - $$P_{DC(average)} = \frac{V_{DD}}{2} \cdot \frac{V_{DD} - V_{OL}}{R_L}$$

Chip area

- The chip area depend on two parameters
  - The W/L ratio of the driver transistor
    - Gate area WxL
  - The value of the resistor R_L
    - Diffused resistor
      - Sheet resistance 20 to 100Ω/□
      - Very large length-to-width rations to achieve resistor values on the order if tens to hundreds of kΩ
    - Ploysilicon resistor
      - Doped polysilicon (for gate of the transistor), Rs~20 to 40 Ω/□
      - Undoped polysilicon, Rs Rs~10M Ω/□
      - The resistance value can not be controlled very accurately ⇨ large variation of the VTC
      - Low power static random access memory (SRAM)

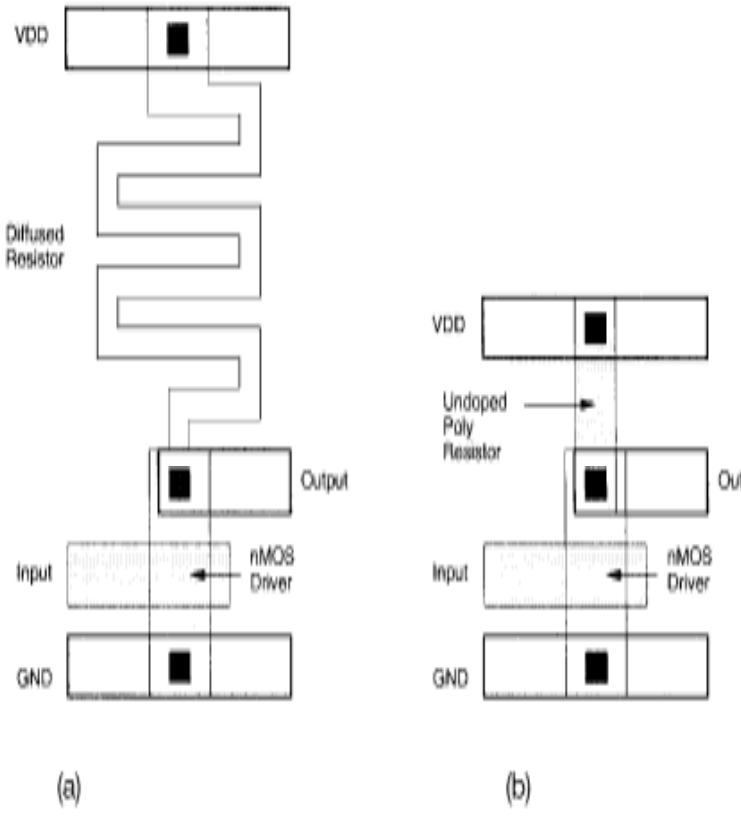


Figure 5.10 Sample layout of resistive-load inverter circuits with (a) diffused resistor and (b) undoped polysilicon resistor.

Example 5.2

Consider a resistive-load inverter circuit with $V_{DD} = 5\,\text{V}$, $k_n' = 20\,\mu\text{A/V}^2$, $V_{T0} = 0.8\,\text{V}$, $R_L = 200\,\text{k}\Omega$, and $W/L = 2$. Calculate the critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) on the VTC and find the noise margins of the circuit.

When the input voltage is low, i.e., when the driver nMOS transistor is cut-off, the output high voltage can be found as

$$V_{OH} = V_{DD} = 5\,\text{V}$$

Note that in this resistive-load inverter example, the transconductance of the driver transistor is $k_n = k_n'(W/L) = 40\,\mu\text{A/V}^2$ and, hence, $(k_n R_L) = 8\,\text{V}^{-1}$.

The output low voltage V_{OL} is calculated by using (5.18):

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L}\right)^2 - \frac{2V_{DD}}{k_n R_L}}$$

$$= 5 - 0.8 + \frac{1}{8} - \sqrt{\left(5 - 0.8 + \frac{1}{8}\right)^2 - \frac{2 \cdot 5}{8}}$$

$$= 0.147\,\text{V}$$

The critical voltage V_{IL} is found using (5.22), as follows.

$$V_{IL} = V_{T0} + \frac{1}{k_n R_L} = 0.8 + \frac{1}{8} = 0.925\,\text{V}$$

Finally, the critical voltage V_{IH} can be calculated by using (5.30).

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L} = 0.8 + \sqrt{\frac{8}{3} \cdot \frac{5}{8}} - \frac{1}{8} = 1.97\,\text{V}$$

Now, the noise margins can be found, according to (5.3) and (5.4).

$$NM_L = V_{IL} - V_{OL} = 0.93 - 0.15 = 0.78\,\text{V}$$

$$NM_H = V_{OH} - V_{IH} = 5.0 - 1.97 = 3.03\,\text{V}$$

At this point, we can comment on the quality of this particular inverter design for DC operation. Notice that the noise margin NM_L found here is quite low, and it may eventually lead to misinterpretation of input signal levels. For better noise immunity, the noise margin for "low" signals should be at least about 25% of the power supply voltage V_{DD}, i.e., about 1.25 V for 5.0 V power supply.

Inverters with n-type MOSFET load

- The resistive-load inverter
  - The large area occupied by the load resistor
- The main advantage of using a MOSFET as the load device
  - Smaller silicon area occupied by the transistor
  - Better overall performance
- Enhancement-load nMOS inverter
  - The saturated enhancement-load inverter
    - A single voltage supply
    - A relative simple fabrication process
    - $V_{OH}=V_{DD}-V_{T,load}$
  - The linear enhancement-type load
    - $V_{OH}=V_{DD}$
    - Higher noise margins
    - Two separate power supply voltage (drawback)
  - Both type suffer from relatively high stand-by (DC) power dissipation
    - Not used in any large-scale digital applications

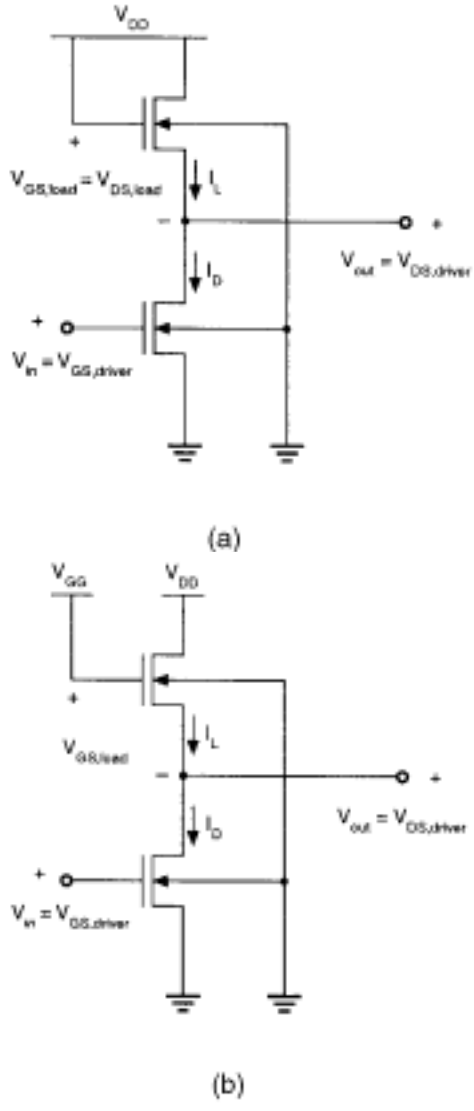
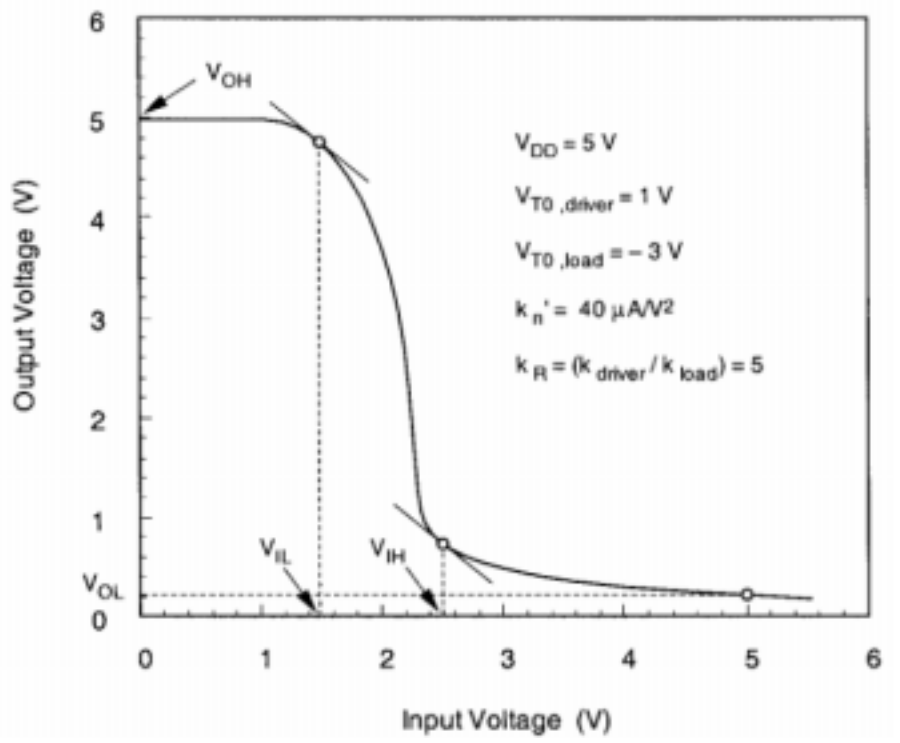


Figure 5.11 (a) Inverter circuit with saturated enhancement-type nMOS load. (b) Inverter with linear enhancement-type load.

Depletion-load nMOS inverter

- Slightly more complicated
  - Channel implant to adjust the threshold voltage
- Advantages
  - Sharp VTC transition better noise margins
  - Single power supply
  - Smaller overall layout area
  - Reduce standby (leakage) current
- The circuit diagram
  - Consisting
    - A nonlinear load resistor, depletion MOSFET, $V_{T0,load}<0$
    - A nonideal switch (driver) , enhancement MOSFET, $V_{T0,load}>0$
  - The load transistor
    - $V_{GS}=0$, always on
  -



$$V_{T,load} = V_{T0,load} + r\left(\sqrt{|2\phi_F| + V_{out}} - \sqrt{|2\phi_F|}\right)$$

When the output voltage is small, $V_{out} < V_{DD} + V_{T,load}$

The load transistor is in saturation region

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot \left[-V_{T,load}(V_{out})\right]^2 = \frac{k_{n,load}}{2} \cdot \left|V_{T,load}(V_{out})\right|^2$$

For larger output voltage level, $V_{out} > V_{DD} + V_{T,load}$

The load transistor operates in the linear region

$$I_{D,load} = \frac{k_{n,load}}{2} \cdot \left[2\left|V_{T,load}(V_{out})\right| \cdot (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2\right]$$

Calculation of V_{OH}, V_{OL}, V_{IL}, V_{iH}

When V_{in} is smaller than $V_{T0} \Rightarrow$ driver $\rightarrow$ off, load $\rightarrow$ linear region

zero drain current, $V_{OH} = V_{DD}$

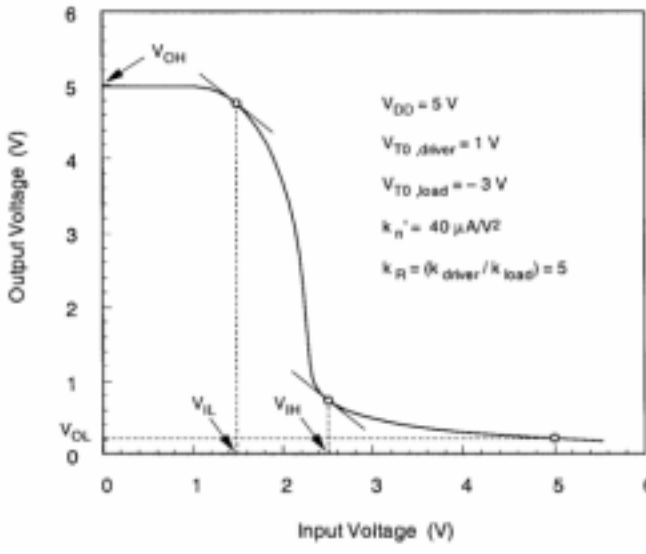
$$I_{D,load} = \frac{k_{n,load}}{2} \cdot \left[2\left|V_{T,load}\left(V_{OH}\right)\right| \cdot \left(V_{DD} - V_{OH}\right) - \left(V_{DD} - V_{OH}\right)^2 \right] = 0$$

To calculate the output low V_{OL}

assume, $V_{in} = V_{OH} = V_{DD} \Rightarrow$ driver $\rightarrow$ linear region, load $\rightarrow$ saturation region

$$\frac{k_{driver}}{2} \cdot \left[2 \cdot \left(V_{OH} - V_{T0}\right) \cdot V_{OL} - V_{OL}^2 \right] = \frac{k_{load}}{2} \cdot \left[-V_{T,load}\left(V_{OL}\right) \right]^2$$

$$V_{OL} = V_{OH} - V_{T0} - \sqrt{\left(V_{OH} - V_{T0}\right)^2 - \left(\frac{k_{load}}{k_{driver}}\right) \cdot \left|V_{T,load}\left(V_{OL}\right)\right|^2}$$



Calculation of V_{OH}, V_{OL}, V_{IL}, V_{IH}

Calculation of V_{IL}

The driver $\Rightarrow$ saturation region, the load $\Rightarrow$ linear region

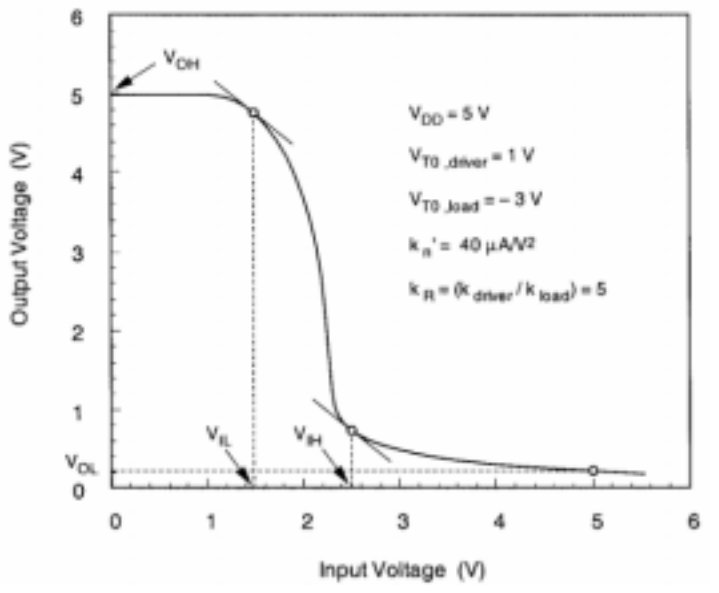
$$\frac{k_{driver}}{2}\cdot\left(V_{in}-V_{T0}\right)^2=\frac{k_{load}}{2}\cdot\left[2\left|V_{T,load}\left(V_{out}\right)\right|\cdot\left(V_{DD}-V_{out}\right)-\left(V_{DD}-V_{out}\right)^2\right]$$

Differential both sides with respect to V_{in}

$$k_{driver}\cdot\left(V_{in}-V_{T0}\right)=\frac{k_{load}}{2}\cdot\left[\begin{array}{l}2\left|V_{T,load}\left(V_{out}\right)\right|\left(-\frac{dV_{T,load}}{dV_{out}}\right)+2\left(V_{DD}-V_{out}\right)\left(-\frac{dV_{T,load}}{dV_{out}}\right)\\-2\left(V_{DD}-V_{out}\right)\left(-\frac{dV_{T,load}}{dV_{out}}\right)\end{array}\right]$$

sbustitute dV_{out}/dV_{in} = -1

$$V_{IL}=V_{T0}+\left(\frac{k_{load}}{k_{driver}}\right)\cdot\left[V_{out}-V_{DD}+\left|V_{T,load}\left(V_{out}\right)\right|\right]$$



Calculation of V_{IH}

The driver $\Rightarrow$ linear region, the load $\Rightarrow$ saturation region

$$\frac{k_{driver}}{2}\cdot\left[2\cdot\left(V_{in}-V_{T0}\right)\cdot V_{out}-V_{out}^2\right]=\frac{k_{load}}{2}\cdot\left[-V_{T,load}\left(V_{out}\right)\right]^2$$

Differential both sides with respect to V_{in}

$$k_{driver}\cdot\left[V_{out}+\left(V_{in}+V_{T0}\right)\left(\frac{dV_{out}}{dV_{in}}\right)-V_{out}\left(\frac{dV_{out}}{dV_{in}}\right)\right]=k_{load}\cdot\left[-V_{T,load}\left(V_{out}\right)\right]\cdot\left(\frac{dV_{T,load}}{dV_{out}}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)$$

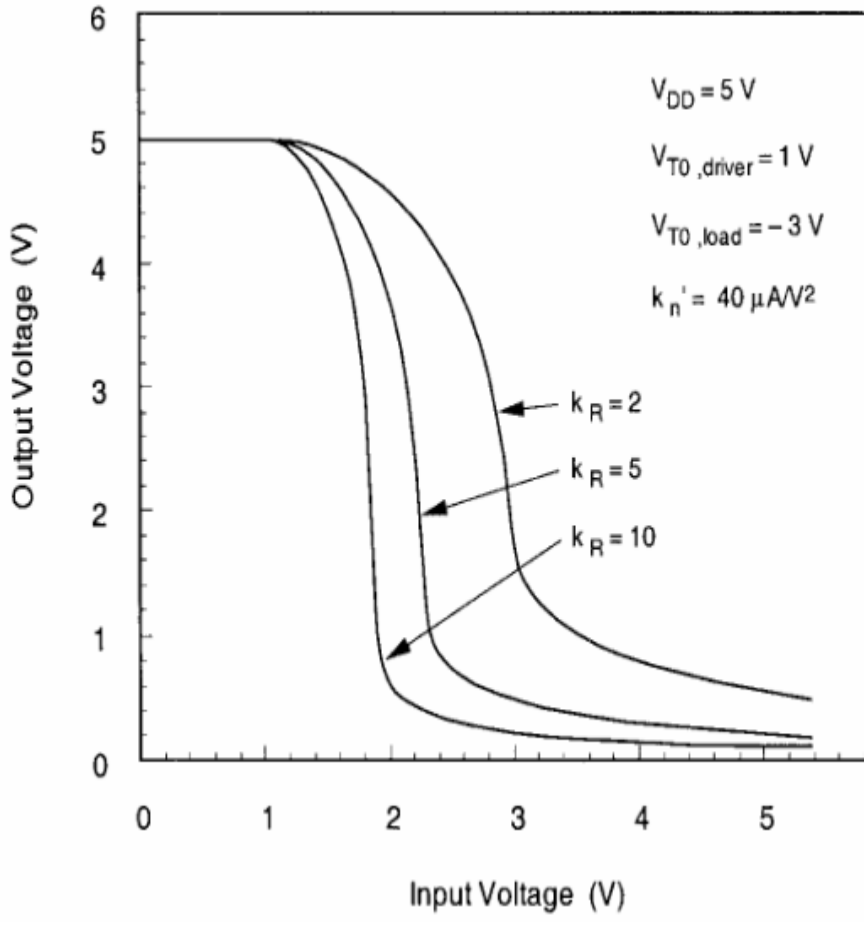
sbustitute dV_{out}/dV_{in} = -1

$$V_{IH}=V_{T0}+2V_{out}+\left(\frac{k_{load}}{k_{driver}}\right)\cdot\left[-V_{T,load}\left(V_{out}\right)\right]\cdot\left(\frac{dV_{T,load}}{dV_{out}}\right)$$

$$\frac{dV_{T,load}}{dV_{out}}=\frac{\gamma}{2\sqrt{\left|2\phi_F\right|+V_{out}}}$$

VTC of depletion load inverters

- The general shape of the inverter VTC, and ultimately, the noise margins, are determined by
  - The threshold voltage of the driver and the load
    - Set by the fabrication process
  - The driver-to-load ratio $k_R=(k_{driver}/k_{load})$
    - Determined by the *(W/L)* ratios of the driver and the load transistor
- One important observation
  - A sharp VTC transition and larger noise margins can be obtained with relative small driver-to-load ratios
    - Much small area occupation



Design of depletion-load inverters

- The designable parameters in the inverter circuit are
  - The power supply voltage V_{DD}
    - Being determined by other external constrains
    - Determining the output level high $V_{OH}=V_{DD}$
  - The threshold voltages of the driver and the load
    - Being determined by the fabrication process
  - The (W/L) ratios of the driver and the load transistor
    - $$k_R = \frac{k_{driver}}{k_{load}} = \frac{\left|V_{T,load}(V_{OL})\right|^2}{2(V_{OH}-V_{T0})V_{OL}-V_{OL}^2}, k_R = \frac{k'_{n,driver}\cdot\left(\frac{W}{L}\right)_{driver}}{k'_{n,load}\cdot\left(\frac{W}{L}\right)_{load}}, k_R = \frac{\left(\frac{W}{L}\right)_{driver}}{\left(\frac{W}{L}\right)_{load}}$$
    - Since the channel doping densities are not equal
      - The channel electron mobilities are not equal
      - $K'_{n,load} \neq k'_{n,driver}$
- The actual sizes of the driver and the load transistor are usually determined by other constrains
  - The current-drive capability
  - The steady state power dissipation
  - The transient switching speed

Power consideration

- The steady-state DC power consumption
  - Input voltage low
    - The driver off, $V_{out}=V_{OH}=V_{DD}$
    - No DC power dissipation
  - Input voltage high, $V_{in}\approx V_{DD}$ and $V_{out}=V_{OL}$
    -

$$I_{DC}\left(V_{in}=V_{DD}\right)=\frac{K_{load}}{2}\cdot\left[-V_{T,load}\left(V_{OL}\right)\right]^2$$

$$=\frac{K_{driver}}{2}\cdot\left[2\cdot\left(V_{OH}-V_{T0}\right)\cdot V_{OL}-V_{OL}^2\right]$$

Assume the input voltage level low 50% operation time and high during the other 50%

$$P_{DC}=\frac{V_{DD}}{2}\cdot\frac{k_{load}}{2}\cdot\left[-V_{T,load}\left(V_{OL}\right)\right]^2$$

Area consideration

- Figure (a)
  - Sharing a common n+ diffusion region
    - Saving silicon area
  - Depletion mode
    - Threshold voltage adjusted by a donor implant into the channel
  - $(W/L)_{driver} > (W/L)_{load}$, ratio about 4
- Figure (b)
  - Buried contact
    - Reducing area
    - For connecting the gate and the source of the load transistor
      - The polysilicon gate of the depletion mode transistor makes a direct ohmic with the n+ source diffusion
      - The contact window on the intermediate diffusion area can be omitted

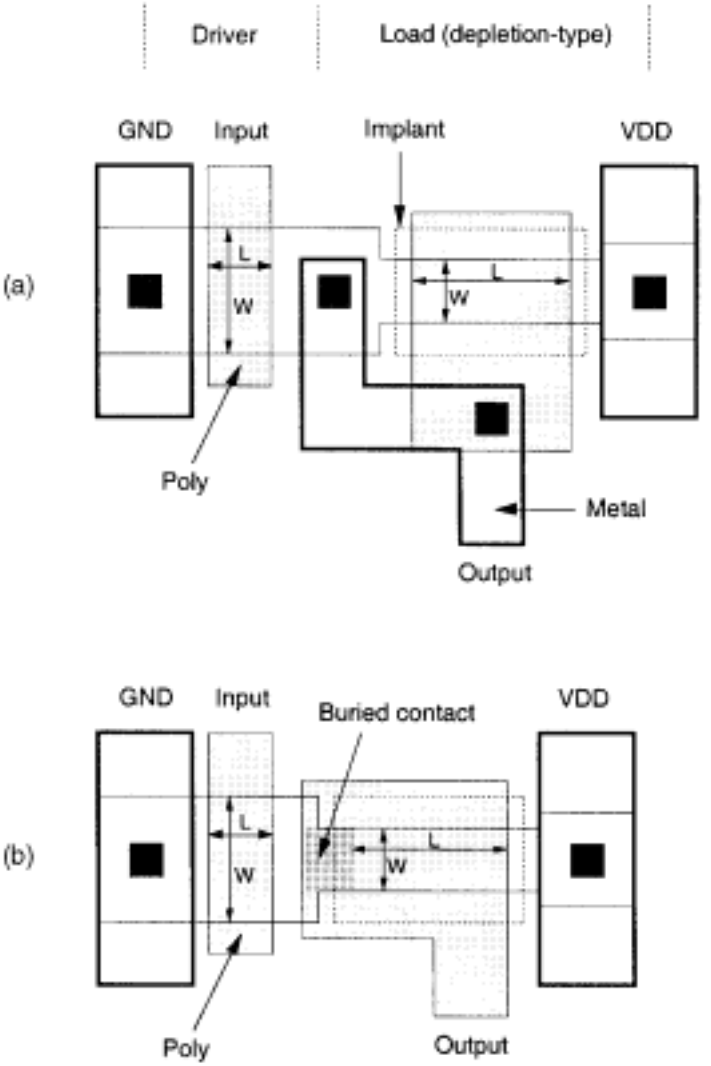
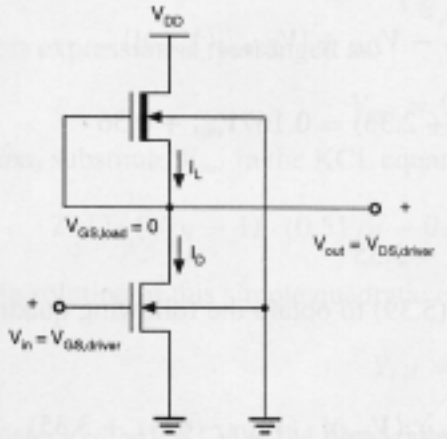


Figure 5.15 Sample layout of depletion-load inverter circuits (a) with output contact on diffusion and (b) with buried contact.

Example 5.3 (1)

the following depletion-load inverter circuit:



$V_{DD} = 5$ V
$V_{T0,driver} = 1.0$ V
$V_{T0,load} = -3.0$ V
$(W/L)_{driver} = 2,\ (W/L)_{load} = 1/3$
$k_{n,driver}' = k_{n,load}' = 25\ \mu A/V^2$
$\gamma = 0.4\ V^{1/2}$
$\phi_F = -0.3$ V

First, the output high voltage is simply found according to (5.36) as $V_{OH} = V_{DD} = 5$ V.

To calculate the output low voltage V_{OL}, we must solve (5.33) and (5.38) simultaneously, using numerical iterations. We start the iterations by assuming that the output voltage is equal to zero, thus letting $V_{T,load} = V_{T0,load} = -3$ V. Solving (5.38) with this assumption yields a first-order estimate for V_{OL}.

$$V_{OL} = V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{T0})^2 - \left(\frac{k_{load}}{k_{driver}}\right) \cdot |V_{T,load}(V_{OL})|^2}$$

$$= 5 - 1 - \sqrt{(5-1)^2 - \left(\frac{1}{6}\right)|3|^2} = 0.192 \text{ V}$$

Now, the threshold voltage of the depletion-load device can be updated by substituting this output voltage into (5.33).

$$V_{T,load} = V_{T0,load} + \gamma\left(\sqrt{|2\phi_F| + V_{OL}} - \sqrt{|2\phi_F|}\right)$$

$$= -3 + 0.4\left(\sqrt{0.6 + 0.2} - \sqrt{0.6}\right) = -2.95 \text{ V}$$

Using this new value for $V_{T,load}$, we now recalculate V_{OL}, again according to (5.38).

$$V_{OL} = 0.186 \text{ V}$$

$$V_{T,load} = -2.95 \text{ V}$$

Example 5.3 (2)

this point, we can stop the iteration process since the threshold voltage of the load vice has not changed in the two significant digits after the decimal point. Continu- the iteration would not produce a perceptible improvement of V_{OL}.

The calculation of V_{IL} involves simultaneous solution of (5.33), (5.39), and 41), using numerical iterations. When the input voltage is equal to V_{IL}, we expect t the output voltage is slightly lower than the output high voltage, V_{OH}. As a first- ler approximation, assume that $V_{out} = V_{OH} = 5$ V for $V_{in} = V_{IL}$. Then, the thresh- l voltage of the load device can be estimated as $V_{T,load}(V_{out} = 5\text{ V}) = -2.36$ V. bstituting this value into (5.41) gives V_{IL} as a function of the output voltage V_{out}.

$$V_{IL}(V_{out}) = V_{T0} + \frac{k_{load}}{k_{driver}} \cdot [V_{out} - V_{DD} + |V_{T,load}(V_{out})|]$$

$$= 1 + \left(\frac{1}{6}\right)(V_{out} - 5 + 2.36) = 0.167V_{out} + 0.56$$

is expression can be rearranged as

$$V_{out} = 6V_{IL} - 3.35$$

w, substitute this into the KCL equation (5.39) to obtain the following quadratic uation for V_{IL}:

$$\frac{k_{driver}}{2} \cdot (V_{IL} - V_{T0})^2 = \frac{k_{load}}{2} \cdot [2|V_{T,load}(V_{out})| \cdot (V_{DD} - 6V_{IL} + 3.35) - (V_{DD} - 6V_{IL} + 3.35)^2]$$

$$2 \cdot (V_{IL} - 1)^2 = \frac{1}{3} \cdot [2 \cdot 2.36 \cdot (5 - 6V_{IL} + 3.35) - (5 - 6V_{IL} + 3.35)^2]$$

The solution of this second-order equation yields two possible values for V_{IL}.

$$V_{IL} = \begin{cases} 0.98\text{ V} \\ \underline{\underline{1.36\text{ V}}} \end{cases}$$

Note that V_{IL} must be larger than the threshold voltage V_{T0} of the driver transis hence, $V_{IL} = 1.36$ V is the physically correct solution. The output voltage leve this point can also be found as

$$V_{out} = 6 \cdot 1.36 - 3.35 = 4.81\text{ V}$$

which significantly improves our initial assumption of $V_{out} = 5$ V. At this point, threshold voltage of the load transistor must be recalculated, in order to update value. Substituting $V_{out} = 4.81$ V into (5.33) yields $V_{T,load} = -2.38$ V. We obse that this value is only slightly higher (by 20 mV) than the threshold voltage va used in the previous calculations. For practical purposes, we can terminate the merical iteration at this stage and accept $V_{IL} = 1.36$ V as a fairly accurate estim

To calculate V_{IH}, we first have to find the numerical value of $(dV_{T,load}/V$ using (5.45). When the input voltage is equal to V_{IH}, the output voltage is expe to be relatively low. As a first-order approximation, assume that the output volt

Example 5.3 (3)

vice can also be estimated as $V_{T,load}(V_{out} = 0.2\ \text{V}) = -2.95\ \text{V}$. Thus,

$$\frac{dV_{T,load}}{dV_{out}} = \frac{\gamma}{2\sqrt{|2\phi_F| + V_{out}}} = \frac{0.4}{2\sqrt{0.6 + 0.2}} = 0.22$$

This value can now be used in (5.44) to find V_{IH} as a function of the output voltage.

$$V_{IH}(V_{out}) = V_{T0} + 2V_{out} + \frac{k_{load}}{k_{driver}} \cdot \left[-V_{T,load}(V_{out})\right] \cdot \left(\frac{dV_{T,load}}{dV_{out}}\right)$$

$$= 1 + 2V_{out} + \left(\frac{1}{6}\right) \cdot 2.95 \cdot 0.22 = 2V_{out} + 1.1$$

This expression is rearranged as:

$$V_{out} = 0.5\ V_{IH} - 0.55$$

Next, substitute V_{out} in the KCL equation (5.42), to obtain

$$2 \cdot [2 \cdot (V_{IH} - 1) \cdot (0.5V_{IH} - 0.55) - (0.5V_{IH} - 0.55)^2] = \frac{1}{3} \cdot (2.95)^2$$

The solution of this simple quadratic equation yields two values for V_{IH}.

$$V_{IH} = \begin{cases} -0.35\ \text{V} \\ \underline{\underline{2.43\ \text{V}}} \end{cases}$$

where $V_{IH} = 2.43$ V is the physically correct solution. The output voltage level at this point is calculated as

$$V_{out} = 0.5 \cdot 2.43 - 0.55 = 0.67\ \text{V}$$

With this updated output voltage value, we can now reevaluate the load threshold voltage as $V_{T,load}(V_{out} = 0.67\ \text{V}) = -2.9\ \text{V}$, and the $(dV_{T,load}/V_{out})$ value as

$$\frac{dV_{T,load}}{dV_{out}} = 0.18$$

Note both of these values are fairly close to those used at the beginning of this iteration process. Repeating the iterative calculation will provide only a marginal improvement of accuracy, thus, we may accept $V_{IH} = 2.43\ \text{V}$ as a good estimate.

In conclusion, the noise margins for high signal levels and for low signal levels can be found as follows:

$$NM_H = V_{OH} - V_{IH} = 2.57\ \text{V}$$

CMOS inverter

- Complementary push-pull
  - High input ⇨nMOS driver, pMOS load
  - Low input ⇨pMOS driver, nMOS load
- Two important advantages
  - Virtually negligible steady state power dissipation
  - VTC exhibits a full output voltage swing between 0V and V_{DD}, transition is very sharp
- Latch up problem
  - Formation of two parasitic bipolar transistors
  - Preventing
    - Guard rings

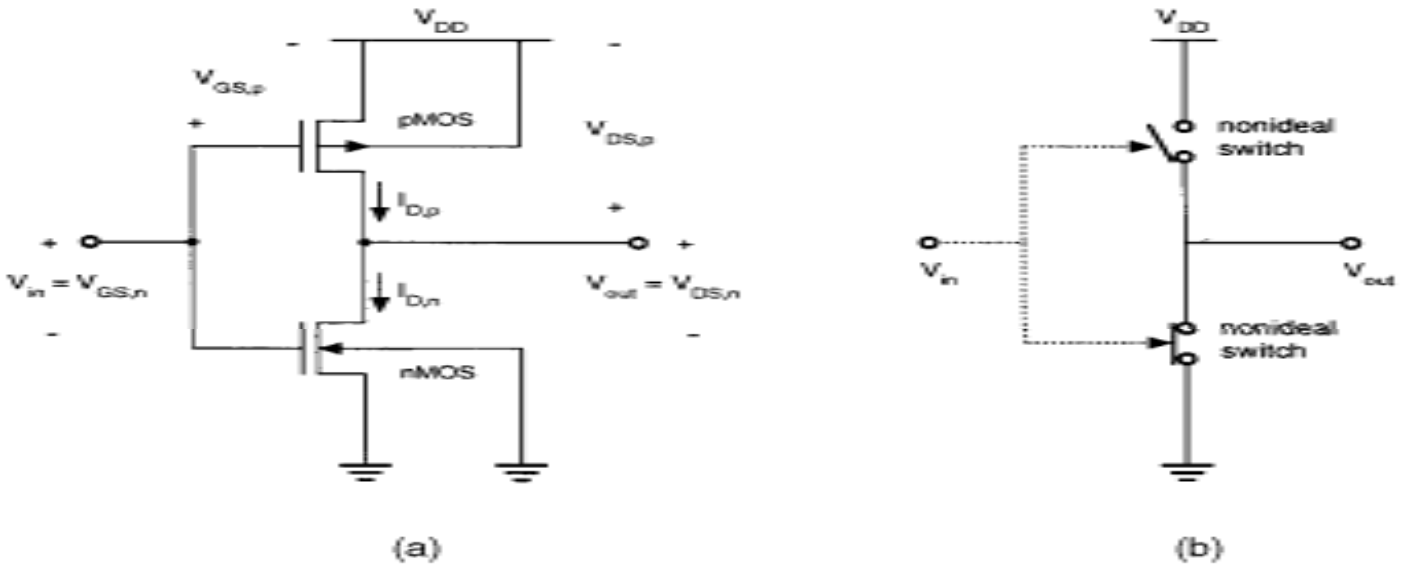


Figure 5.16 (a) CMOS inverter circuit. (b) Simplified view of the CMOS inverter, consisting of two complementary nonideal switches.

Circuit operation

- Region A: $V_{in}<V_{T0,n}$
  - nMOS off, pMOS on ⇨ $I_{D,n}=I_{D,p}=0$, $V_{out}=V_{OH}=V_{DD}$
- Region B: $V_{in}>V_{T0,n}$
  - nMOS saturation, the output voltagedecreases
  - The critical voltage V_{IL}, $(dV_{out}/dV_{in})=-1$ is located within this region
  - As the output further decreases ⇨pMOS enter saturation, boundary of region C
- Region C:
  - If nMOS saturation ⇨ $V_{DS,n}\geq V_{GS,n}-V_{T0,n} \Leftrightarrow V_{out} \geq V_{in}-V_{T0,n}$
  - If pMOS saturation ⇨ $V_{DS,n}\leq V_{GS,p}-V_{T0,p} \Leftrightarrow V_{out} \leq V_{in}-V_{T0,p}$
  - Both of these conditions for device saturation are illustrated graphically as shaded areas
- Region D: $V_{out}<V_{in}-V_{T0,p}$
  - The criical point V_{IH}
- Region E: $V_{in}>V_{DD}+V_{T0,p}$
  - $V_{out}=V_{OL}=0$

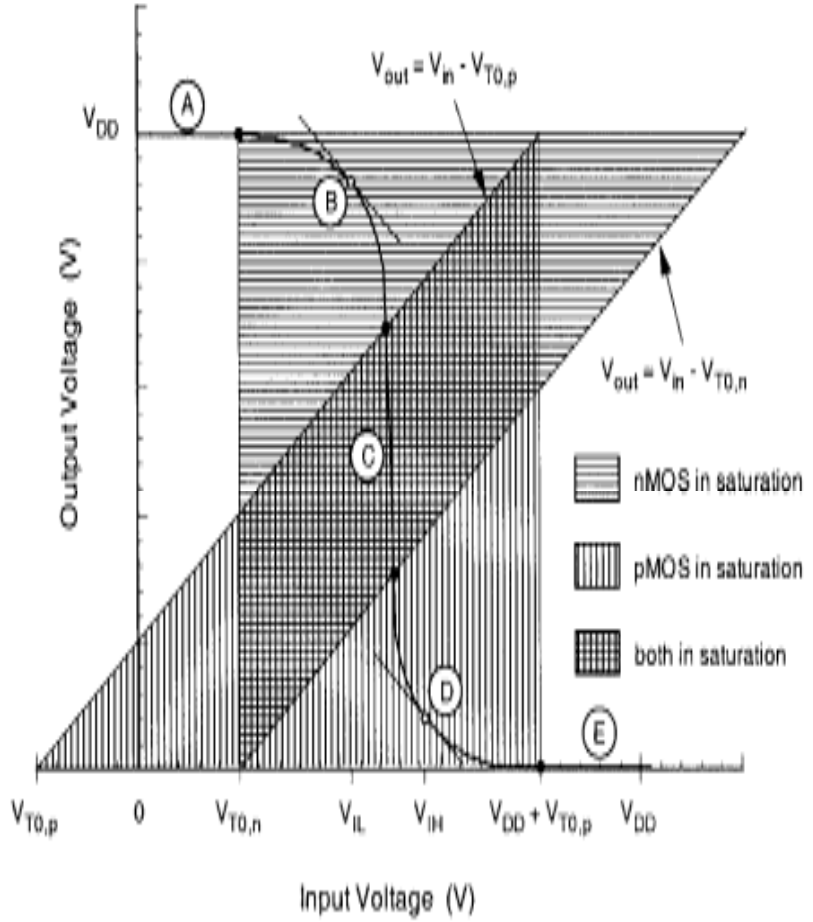


Figure 5.17 Operating regions of the nMOS and the pMOS transistors.

Circuit operation

- The nMOS and the pMOS transistors an be seen as nearly ideal switches
  - The current drawn from the power supply in both these steady state points region A and region E
    - Nearly equal to zero
    - The only current ⇨reverse biased S, D leakage current
  - The CMOS inverter can drive any load
    - Interconnect capacitance
    - Fan-out logic gates
    - Either by supplying current to the load, or by sinking current from the load

The steady-state input-out voltage characteristics

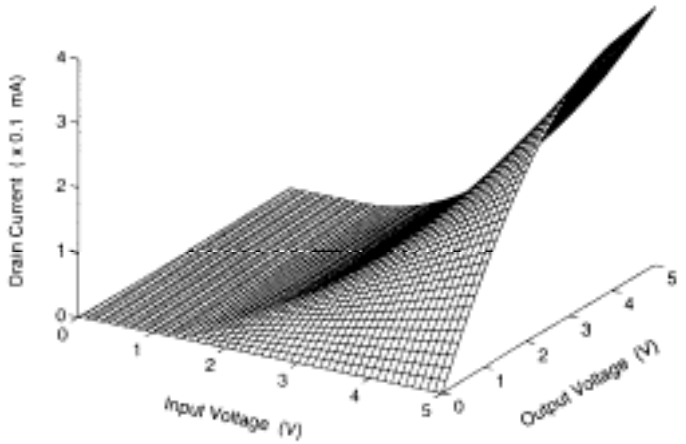


Figure 5.18 Current-voltage surface representing the nMOS transistor characteristics.

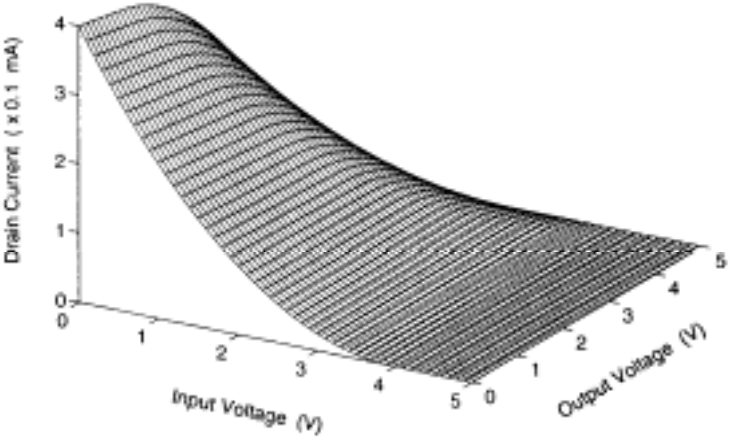


Figure 5.19 Current-voltage surface representing the pMOS transistor characteristics.

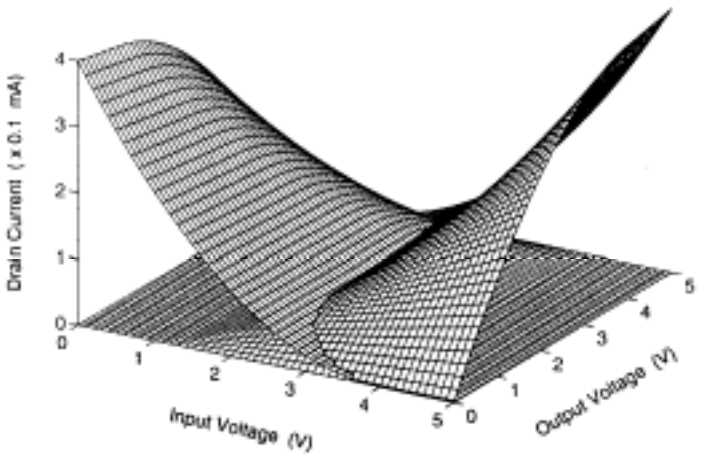


Figure 5.20 Intersection of the current-voltage surfaces shown in Figs. 5.18 and 5.19.

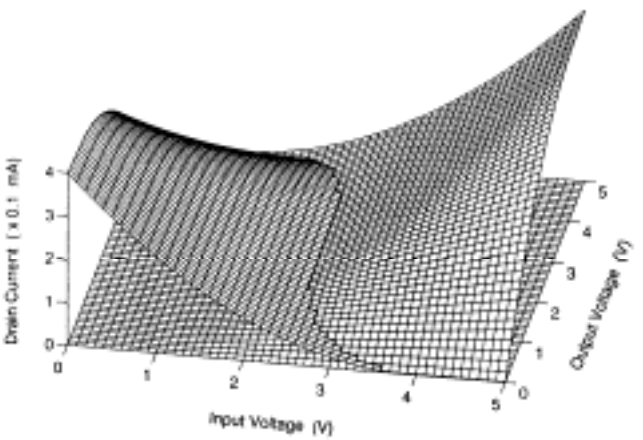


Figure 5.21 The intersecting current-voltage surfaces shown from a different viewing angle. Notice that projection of the intersection curve on the voltage plane gives the VTC.

Calculation of V_{IL}, V_{IH}

nMOS saturation, pMOS linear

$$\frac{k_n}{2}\cdot\left(V_{GS,n}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left[2\cdot\left(V_{GS,p}-V_{T0,p}\right)\cdot V_{DS,P}-V_{DS,p}^2\right]$$

$$\frac{k_n}{2}\cdot\left(V_{in}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left[2\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)\cdot\left(V_{out}-V_{DD}\right)-\left(V_{out}-V_{DD}\right)^2\right]$$

$$k_n\cdot\left(V_{in}-V_{T0,n}\right)=k_p\cdot\left[\left(V_{in}-V_{DD}-V_{T0,p}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)+\left(V_{out}-V_{DD}\right)-\left(V_{out}-V_{DD}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)\right]$$

substituting $V_{in}=V_{IL}$ *and* $(dV_{out}/dV_{in})=-1$

$$k_n\cdot\left(V_{IL}-V_{T0.n}\right)=k_p\cdot\left(2V_{out}-V_{IL}+V_{T0,p}-V_{DD}\right)$$

$$V_{IL}=\frac{2V_{out}+V_{T0,p}-V_{DD}+k_RV_{T0,n}}{1+k_R}\text{ where }k_R=\frac{k_n}{k_p}$$

nMOS linear, pMOS saturation

$$\frac{k_n}{2}\cdot\left[2\cdot\left(V_{GS,n}-V_{T0,n}\right)\cdot V_{DS,n}-V_{DS,n}^2\right]=\frac{k_p}{2}\cdot\left(V_{GS,p}-V_{T0,p}\right)^2$$

$$\frac{k_n}{2}\cdot\left[2\cdot\left(V_{in}-V_{T0,n}\right)\cdot V_{out}-V_{out}^2\right]=\frac{k_p}{2}\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)^2$$

$$k_n\cdot\left[\left(V_{in}-V_{T0,n}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)+V_{out}-V_{out}\cdot\left(\frac{dV_{out}}{dV_{in}}\right)\right]=k_p\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)$$

substiting $V_{in}=V_{IH}$ and $(dV_{out}/dV_{in})=-1$

$$k_n\cdot\left(-V_{IH}+V_{T0,n}+2V_{out}\right)=k_p\cdot\left(V_{IH}-V_{DD}-V_{T0,p}\right)$$

$$V_{IH}=\frac{V_{DD}+V_{T0,p}+k_R\cdot\left(2V_{out}+V_{T0,n}\right)}{1+k_R}$$

Calculation of V_{th}

The inveter th reshold voltage is defined as $V_{th} = V_{in} = V_{out}$

Since the CMOS inverter exhibits large noise margins and very sharp VTC transitio n the inverter t hreshold voltage emerges as an imporant parameter characteri zing the DC performanc e of the inverter

For $V_{in} = V_{out}$, both trans istor are in saturation mode

$$\frac{k_n}{2} \cdot \left(V_{GS,n} - V_{T0,n}\right)^2 = \frac{k_p}{2} \cdot \left(V_{GS,p} - V_{T0,p}\right)^2$$

$$\frac{k_n}{2} \cdot \left(V_{in} - V_{T0,n}\right)^2 = \frac{k_p}{2} \cdot \left(V_{in} - V_{DD} - V_{T0,p}\right)^2$$

$$Vin \cdot \left(1 + \sqrt{\frac{k_p}{k_n}}\right) = V_{T0,n} + \sqrt{\frac{k_p}{k_n}} \cdot \left(V_{DD} + V_{T0,p}\right)$$

$$V_{th} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot \left(V_{DD} + V_{T0,p}\right)}{\left(1 + \frac{1}{k_R}\right)}$$

If $V_{in} = V_{th}$, the output vol tage can actually attain any value between $\left(V_{th}\text{-}V_{T0,n}\right)$ and $\left(V_{th}\text{-}V_{T0,p}\right)$

Threshold voltage

- The Region C of VTC
  - Completely vertical
    - If the channel length modulation effect is neglected, i.e. if $\lambda=0$
  - Exhibits a finite slope
    - If $\lambda>0$
    - Fig 5.22 shows the variation of the inversion (switching) threshold voltage V_{th} as function of the transconductance ratio k_R

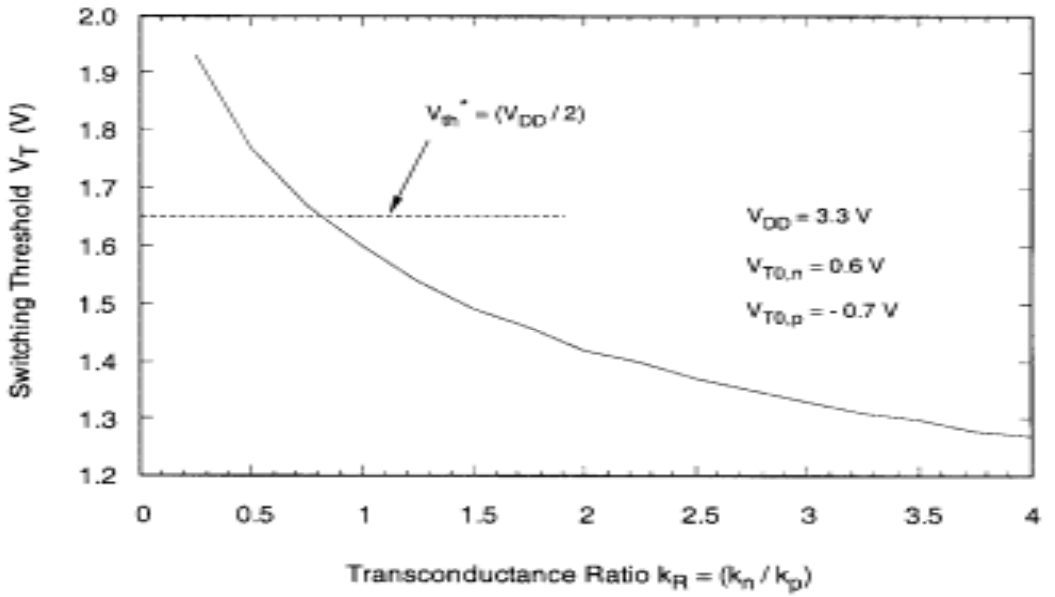


Figure 5.22 Variation of the inversion threshold voltage as a function of k_R.

VTC and power supply current

- If input voltage is either smaller than $V_{T0,n}$, or larger than $V_{DD}+V_{T0,p}$
  - Does not draw any significant current from the power supply
  - Except for small leakage current and subthreshold currents
- During low-to-high and high-to-low transitions
  - Regions B, C, and D
  - The current being drawn from the power source
  - Reaching its peak value when $V_{in}=V_{th}$ (both saturation mode)

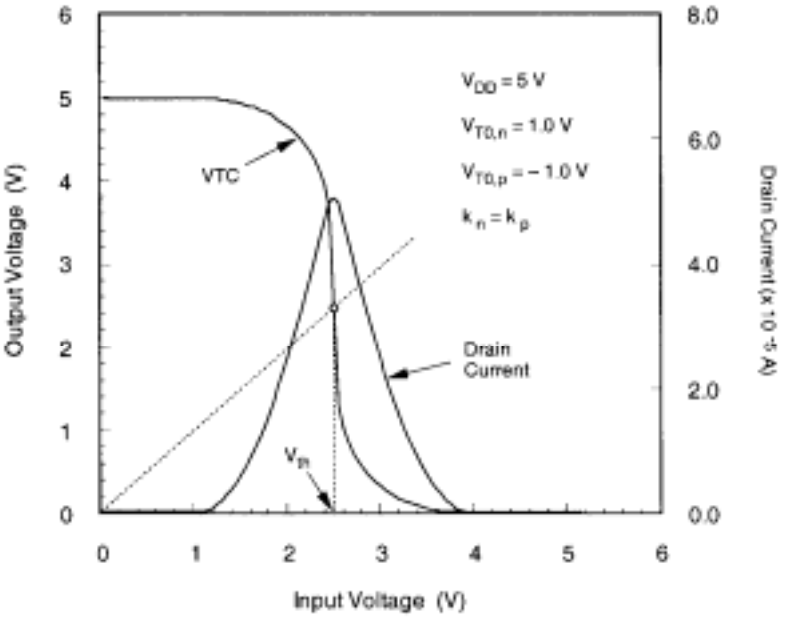


Figure 5.23 Typical VTC and the power supply current of a CMOS inverter circuit.

Design of CMOS inverters

$$\sqrt{\frac{1}{k_R}} = \frac{V_{th} - V_{T0,n}}{V_{DD} + V_{T0,p} - V_{th}} \Rightarrow k_R = \frac{k_n}{k_p} = \left(\frac{V_{DD} + V_{T0,p} + V_{th}}{V_{th} - V_{T0,n}} \right)^2$$

The switching threshold voltage of an ideal inverter is defined as $V_{th,ideal} = \frac{1}{2} \cdot V_{DD}$ s

substituting 5.74 in 5.73 $\Rightarrow \left(\frac{k_n}{k_p} \right)_{ideal} = \left(\frac{0.5_{VDD} + V_{T0,p}}{0.5V_{DD} + V_{T0,n}} \right)^2$

we can achieve complely symmetric input - output characteristics by setting $V_{T0} = V_{T0,n} = \left| V_{T0,p} \right| \Rightarrow \left(\frac{k_n}{k_p} \right)_{\substack{symmertric \\ inverter}} = 1$

$$\frac{k_n}{k_p} = \frac{\mu_n C_{OX} \cdot \left(\frac{W}{L} \right)_n}{\mu_p C_{OX} \cdot \left(\frac{W}{L} \right)_p} = \frac{\mu_n \cdot \left(\frac{W}{L} \right)_n}{\mu_p \cdot \left(\frac{W}{L} \right)_p}$$

assume t_{ox}, C_{ox} have the same value for *nMOS* and *pMOS*

$$\frac{\left(\frac{W}{L} \right)_n}{\left(\frac{W}{L} \right)_p} = \frac{\mu_p}{\mu_n} \approx \frac{230 cm^2 / V \cdot s}{580 cm^2 / V \cdot s} \Rightarrow \left(\frac{W}{L} \right)_p \approx 2.5 \left(\frac{W}{L} \right)_n$$

For a symmetric CMOS inverter with $V_{T0,n} = \left| V_{T0,p} \right|$ and $k_R = 1$

$$V_{IL} = \frac{1}{8} \cdot \left(3V_{DD} + 2V_{T0,n} \right), V_{IH} = \frac{1}{8} \cdot \left(5V_{DD} - 2V_{T0,n} \right)$$

$V_{IL} + V_{IH} = V_{DD}$, $NM_L = V_{IL} - V_{OL} = V_{IL}$, $NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH}$

$NM_L = N_{MH} = V_{IL}$

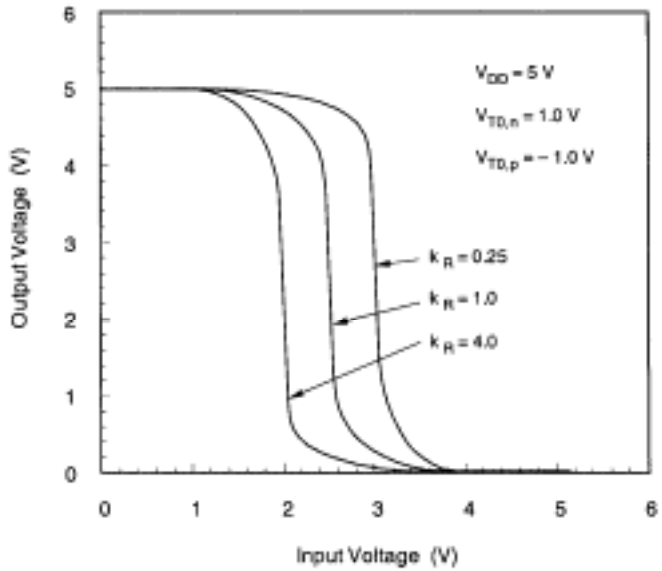


Figure 5.24 Voltage transfer characteristics of three CMOS inverters, with different nMOS-to-pMOS ratios.

Example 5.4

Consider a CMOS inverter circuit with the following parameters:

$V_{DD} = 3.3\ \text{V}$
$V_{T0,n} = 0.6\ \text{V}$
$V_{T0,p} = -0.7\ \text{V}$
$k_n = 200\ \mu\text{A/V}^2$
$k_p = 80\ \mu\text{A/V}^2$

Calculate the noise margins of the circuit. Notice that the CMOS inverter being considered here has $k_R = 2.5$ and $V_{T0,n} \neq |V_{T0,p}|$; hence, it is not a symmetric inverter.

First, the output low voltage V_{OL} and the output high voltage V_{OH} are found, using (5.54) and (5.55), as $V_{OL} = 0$ and $V_{OH} = 3.3\ \text{V}$. To calculate V_{IL} in terms of the output voltage, we use (5.62).

$$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + k_R V_{T0,n}}{1 + k_R}$$
$$= \frac{2V_{out} - 0.7 - 3.3 + 1.5}{1 + 2.5} = 0.57V_{out} - 0.71$$

Now substitute this expression into the KCL equation (5.59).

$$2.5(0.57V_{out} - 0.71 - 0.6)^2 = 2(0.57V_{out} - 0.71 - 3.3 + 0.7)(V_{out} - 3.3) - (V_{out} - 3.3)^2$$

This expression yields a second-order polynomial in V_{out}, as follows:

$$0.66V_{out}^2 + 0.05V_{out} - 6.65 = 0$$

Only one root of this quadratic equation corresponds to a physically correct solution for V_{out} (i.e., $V_{out} > 0$).

$$V_{out} = 3.14\ \text{V}$$

From this value, we can calculate the critical voltage V_{IL} as:

$$V_{IL} = 0.57 \cdot 3.14 - 0.71 = \underline{\underline{1.08\ \text{V}}}$$

To calculate V_{IH} in terms of the output voltage, use (5.67):

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + k_R \cdot (2V_{out} + V_{T0,n})}{1 + k_R}$$
$$= \frac{3.3 - 0.7 + 2.5(2V_{out} + 0.6)}{\quad} = 1.43V_{out} + 1.17$$

Next, substitute this expression into the KCL equation (5.64) to obtain a seco order polynomial in V_{out}.

$$2.5\left[2(1.43V_{out} + 1.17 - 0.6)V_{out} - V_{out}^2\right] = (1.43V_{out} - 1.43)^2$$
$$2.61V_{out}^2 + 6.94V_{out} - 2.04 = 0$$

Again, only one root of this quadratic equation corresponds to the physically cor solution for V_{out} at this operating point, i.e., when $V_{in} = V_{IH}$.

$$V_{out} = 0.27\ \text{V}$$

From this value, we can calculate the critical voltage V_{IH} as:

$$V_{IH} = 1.43 \cdot 0.37 + 1.17 = \underline{\underline{1.55\ \text{V}}}$$

Finally, we find the noise margins for low voltage levels and for high voltage le using (5.3) and (5.4).

$$NM_L = V_{IL} - V_{OL} = 1.08\ \text{V}$$
$$NM_H = V_{OH} - V_{IH} = 1.75\ \text{V}$$

Supply voltage scaling in CMOS inverters

- The static characteristics of the CMOS inverter allow significant variation of supply voltage without affecting the functionality of the basic inverter
- The CMOS inverter will continue to operate correctly with a supply voltage limit value
  - $V_{DD}^{\min} = V_{T0,n} + \left|V_{T0,p}\right|$
  - Correct inverter operation will be sustained if at least one of the transistors remains in conduction, for any given voltage
  - The exact shape of the VTC near e limit value is essentially determined by subthreshold conduction properties
- If the power supply voltage is reduced below the sum of the two threshold
  - The VTC will contain a region in which none of the transistors is conducting
  - The output voltage level is determine by the previous state of the output
  - The VTC exhibits a hysteresis behavior

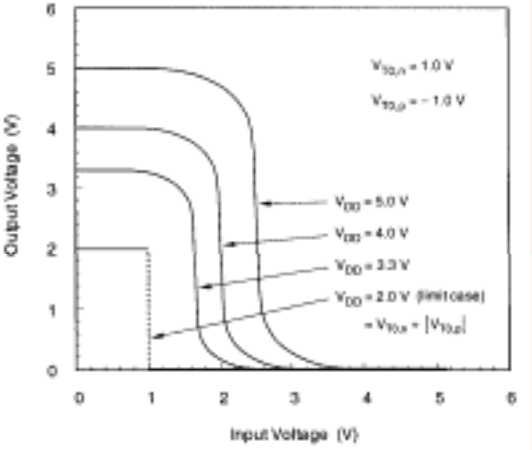


Figure 5.25 Voltage transfer characteristics of a CMOS inverter, obtained with different power supply voltage levels.

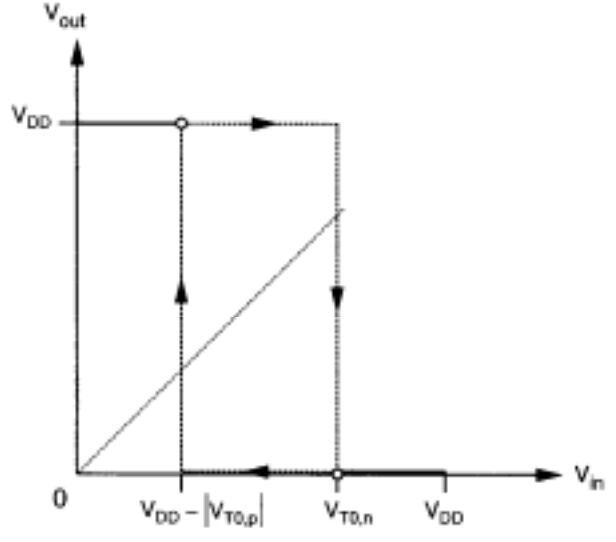


Figure 5.26 Voltage transfer characteristic of a CMOS inverter, operated with a supply voltage which is lower than the limit given in (5.85).

Power and area consideration

- Power consideration
  - DC power dissipation of the circuit is almost negligible
  - The drain current
    - Source and drain pn junction reverse leakage current
    - In short channel leakage current
    - Subthreshold current
  - However, that the CMOS inverter does conduct a significant amount of current during a switching event
- Area consideration

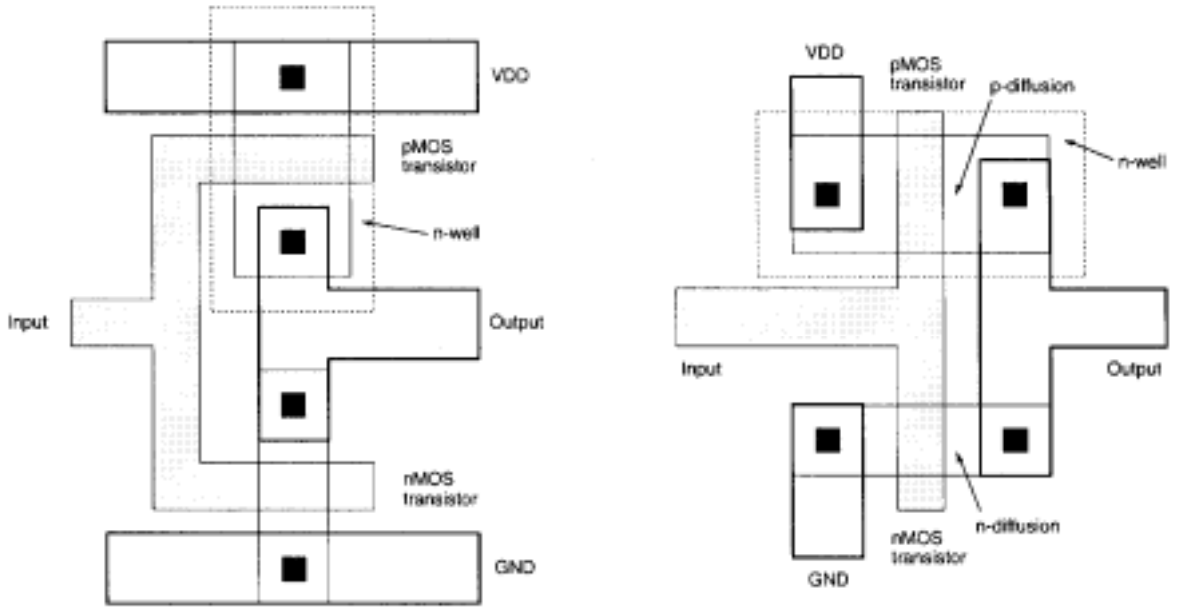


Figure 5.27 Two sample layouts of CMOS inverter circuits (for p-type substrate).