B.Tech.

THIRD SEMESTER EXAMINATION, 2008-09

Pulse and Digital Electronics **TEC-304**

Time : 3 Hours] *[Total Marks : 100*

*Note : (1) Attempt **all** questions.*

*(2) All question carry **equal** marks.*

(3) Be precise in your answer.

(4) No second answer book will be provided.

Q.1. Attempt any four parts of the following : **5 × 4 = 20**

Q.1. (a) What are the various parameters used to characterise logic families ? Explain.

Ans. (i) Speed of operation—The speed of a digital circuit is expressed in terms of propagation delay. It is defined as the time taken for the output of the gate to change after the I/P has been changed. There are two types of delay.

t_{PLH}—It is the propagation delay time in going from logic LOW to logic HIGH state.

t_{PHL}—It is the propagation delay time in going from propagation delay $= \frac{t_{PHL} + t_{PLH}}{2}$

(ii) Power Dissipation—Power dissipation is a measure of power consumed by logic gate when fully driven by all inputs. It is expressed in mW.

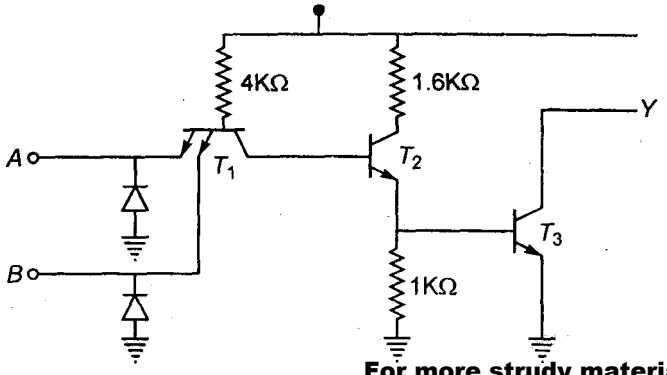
(iii) Fan In—The fan in of the gate is to no. of inputs connected to that gate without any decredation in voltage levels.

(iv) Fan Out—It is the maximum no. of logic gates that the gate can drive without any decredation in voltage levels.

(v) Noise Immunity—Noise immunity is the maximum noise voltage that may appear at the input of a logic gate without changing its logical state of its output. It is also known as noise margin.

Q.1(b) What is meant by open collector output of TTL gate ? What is its utility ? Explain its operation with the help of circuit diagram.

Ans. Open Collector Output of TTL Gate— Open collector output of TTL gate is the output when the collector of the LOW state output transistor is brought out directly to the output pin. There is no built in HIGH state output circuitry which allows two or more open-collector outputs to be connected without possible damage.



Two input TTL open collector output circuit

Q.1(c) What are the merits and demerits and ECL logic family with respect to TTL logic family?

Ans. Merits of ECL Logic Family with respect to TTL Logic Family—

(i) Emitters of transistors are coupled not allowing the transistors to go in saturation state.

(ii) It has higher no. of fan-out (25) as compared to TTL (10).

(iii) Propagation delay time for ECL family is very low.

(iv) OR & NOR gates can be constructed.

Demerits—

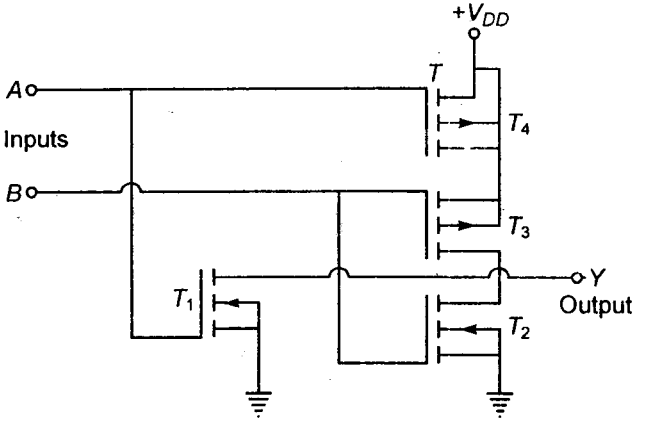
(i) The fan in for ECL family is low (5) as compared to TTL family (8).

(ii) ECL family has more power consumption than that of TTL family.

(iii) Noise immunity for TTL is much better than ECL.

Q.1(d) Explain the operation of a 2-input CMOS NOR gate.

Ans. 2 Input CMOS NOR Gate



Two input CMOS NOR Gate

Figure shows the typical diagram for CMOS NOR-gate. The circuit uses two *n*-type CMOS transistor T_1, T_2 and two *p*-type CMOS T_3 and T_4. A and B are the two Inputs for the circuit.

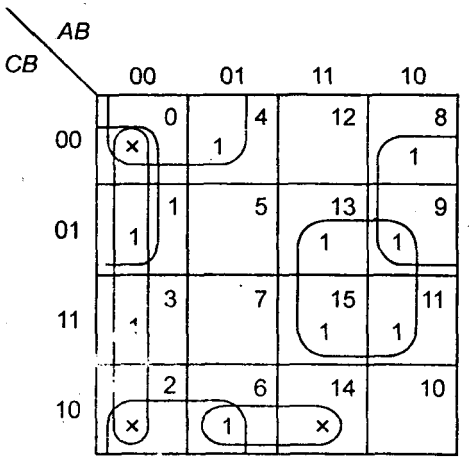
Consider $A = B = 1$, then T_1 and T_2 will be 'ON' and will act as closed switch. At the same instant T_3 and T_4 will be 'OFF'. Thus the output C will be zero (0).

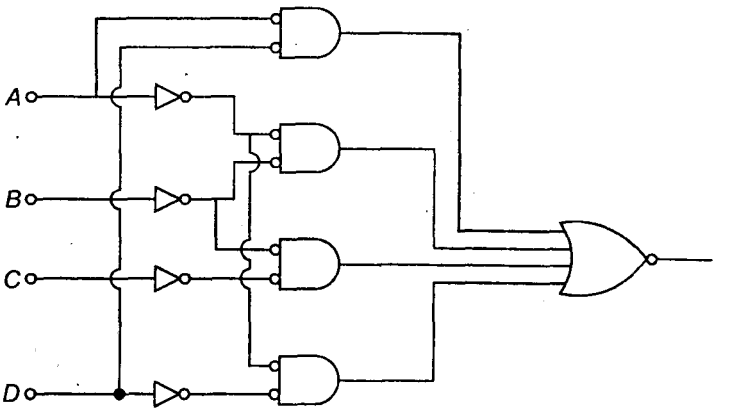
Truth table for CMOS NOR Gate—

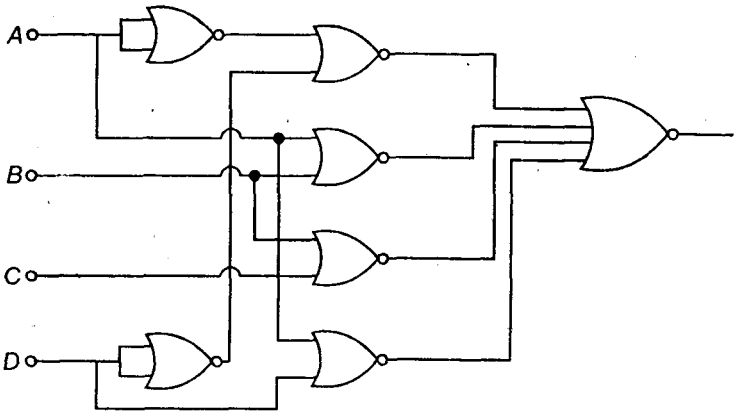
Inputs		Outputs
A	***B***	***Y***
0	0	1
0	1	0
1	0	0
1	1	0

Q.1(e) Simplify the following function using K-map and implement the result using universal gates only : $F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$

Ans. $F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$







$$F = \overline{A}\overline{B} + \overline{A}\overline{D} + AD + \overline{B}\overline{C}$$

$$= \overline{A}\overline{B} + \overline{B}\overline{C} + \overline{A}\overline{D} + AD$$

Q.1(f) Minimize the following Boolean function using tabulation method.

$$f(w, x, y, z) = \Sigma m(0, 1, 4, 5, 6, 7, 9, 11, 15) + \Sigma d(40, 14)$$

Ans. $f(w, x, y, z) = \Sigma m(0, 1, 4, 5, 6, 7, 9, 11, 15) + \Sigma d(40, 14)$

	Decimal number	Binary representation of each term
Index 0	0	0 0 0 0
	1	0 0 0 1
Index 1	4	0 1 0 0
	5	0 1 0 1
	6	0 1 1 0
Index 2	9	1 0 0 1
	10	1 1 0 0
	7	0 1 1 1
Index 3	11	1 0 1 1
	14	1 1 1 0
Index 4	15	1 1 1 1

Decimal number	First reduction
0, 1	0 0 0 –
0, 4	0 – 0 0
1, 5	0 – 0 1
1, 9	– 0 0 1 F
4, 5	1 1 0 –
4, 6	0 1 – 0
5, 7	0 1 – 1
6, 7	0 1 1 –
6, 14	– 1 1 0
9, 11	1 0 – 1 E
10, 11	1 0 1 –
10, 14	1 – 1 0
7, 15	– 1 1 1
11, 15	1 – 1 1 1
14, 15	1 1 1 –

Decimal number	Second reduction
0, 1, 4, 5	0 – 0 –
0, 4, 1, 5	0 – 0 – 0
4, 5, 6, 7	0 1 – –
4, 6, 5, 7	0 1 – – C
6, 7, 14, 15	– 1 1 –
6, 14, 7, 15	– 1 1 – B
10, 11, 14, 15	1 – 1 –
10, 14, 11, 15	1 – 1 – A

Prime implicant table :

	0	1	4	5	6	7	9	11	15
A								×	×
B××					×	×			×
C			×	×	×	×			
D×	⊗	×	×	×					
E							×	×	
F××		×					×		

So minimal. Sum of function

$$= B + D + F$$
$$= -11 - + 0 - 0 - + - 001$$
$$= xy + \bar{w}\,\bar{y} + \bar{x}\,\bar{y}\,z$$

Q.2. Attempt any four parts of the following : $5 \times 4 = 20$

Q.2. (a) Negate the unsigned binary number 00010101 and represent it in all four methods of negative binary number representation.

Ans. $(00010101)_2$

(i) $(10010101)_2$ (Signal mag method)

(ii) $-(11101010)_2$ (One's complement)

(iii) $-(11101011)_2$ (Two's complement)

(iv) $-(00010101)_2$

Q.2(b) Perform the subtraction on the following usigned binary numbers using the 2's complement of the subtrahend.

(i) 1011 – 110000

(ii) 11.11 – 0001.1110

Ans. (i) 1011 – 110000

Two's complement of $(110000) = 001111 + 1$

$$= 010000$$

$$1011 - 110000 = 1011 + 010000$$

$$= 011011$$

Since there is no carry.

So the answer will be $= -\{2\text{'s complement of } (01101)\}$

$$= -\{100100 + 1\} = -(100101)$$

(ii) 11.11 – 0001.1110

$$= 11.11 - 1.1110$$

Two's complement of 1.1110

$$= 0.0001 + 1 = 1.0001$$

$$11.11 - 1.1110 = 11.11 + 1.0001$$

$$= 100.1101$$

Since there exist carry.

Hence the answer will be $= 00.1101$

Q.2(c) Design a combinational circuit that compares two 3-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

Ans. Let two numbers are $A = A_2\ A_1\ A_0$

$$B = B_2\ B_1\ B_0$$

The two number are equal if all pairs of significant digits are equal

$$A_2 = B_2,\ A_1 = B_1,\ A_0 = B_0$$

when number are binary the digits are either 1 or 0 and equality relation of each-pair of bits can be expressed logically with an exclusive nor $\frac{0}{0}$

$$x_i = A_i B_i + A_i^1 \; B_i^1$$

for $i = 0, 1, 2$

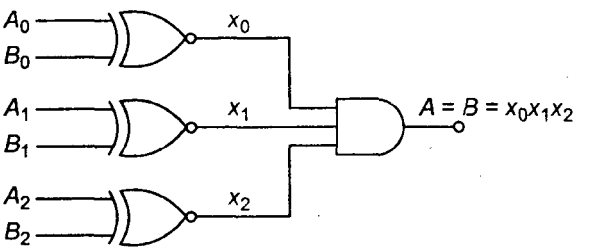
for $(A = B) = x_2 \; x_1 \; x_0$

where $x_0 = A_0 B_0 + A_0^1 + B_0^1$

$$x_1 = A_1 B_1 + A_1^1 B_1^1$$

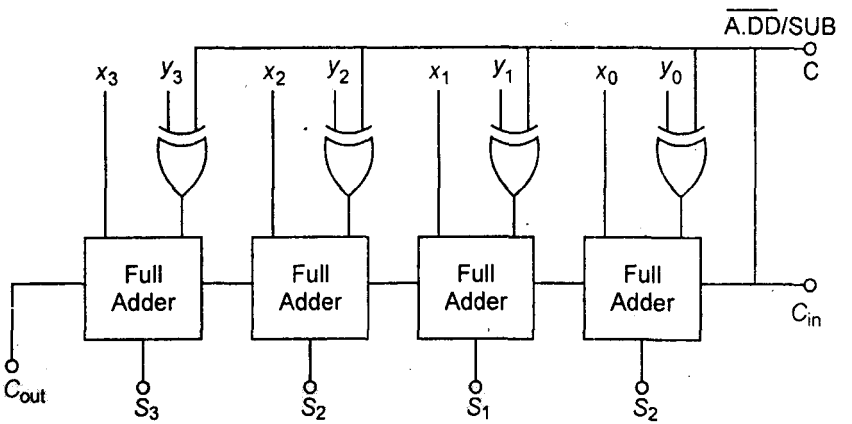
$$x_2 = A_2 B_2 + A_2^1 B_2^1$$

$$A = B = x_2 \; x_1 \; x_0$$



Q.2(d) Draw a 4-bit adder-subtractor circuit and explain its operation.

Ans. The four bit parallel binary adder-subtractor ckt. is shown in figure. It performs the operation of both addition and subtraction. It has two 4 bit inputs $x_3 \; x_2 \; x_1 \; x_0$ and $y_3 \; y_2 \; y_1 \; y_0$.



We can't perform the two operations simultaneously. So we need one control signal to perform this operation. The $\overline{ADD}/SUB$ control line, connected with c_{in} of LSB of the full adder, is used to perform the operations of addition and subtraction. The XOR gates are used as controlled invertors. From the XOR gate truth table we may know that when one of the inputs is low the output is the same value of the other input and when one of the inputs is the complement of the other input.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

When $C = 1$ *i.e.*, $\overline{ADD} / SUB = 1$

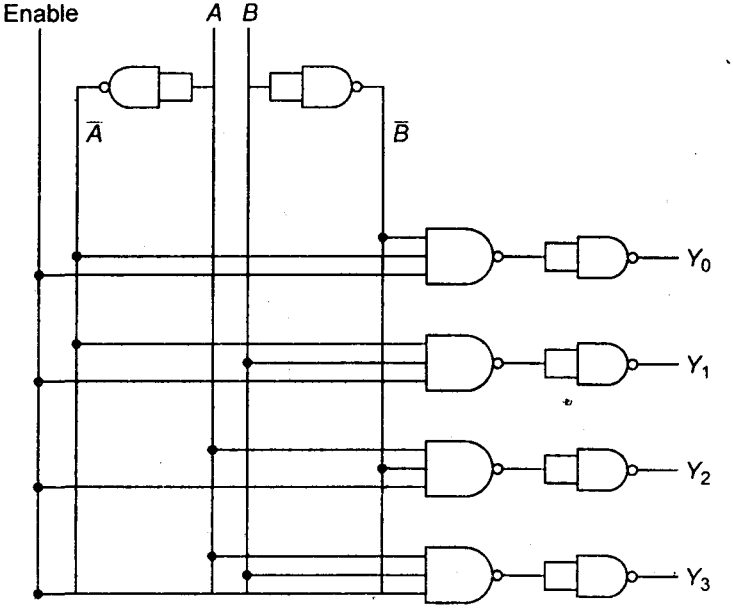
If $\overline{ADD} / SUB = 1$ then *XOR* gate produces the is complement of y_0, y_1, y_2, y_3. Since 1 is given to c_{in}. It is added to the complemented output of *XOR* gate hence making its 2's complement. The 2's complemented y_3, y_2, y_1, y_0 will be added to x_3, x_2, x_1, x_0 to produce the sum. This sum $S_3, S_2, S_1 S_0$ is the difference of the two binary numbers.

When $C = 0$ *i.e.*, $\overline{ADD} / SUB = 0$

Now the controlled inverter is transferred y_3, y_2, y_1, y_0 4-bit to full adder, this 4 bit is added with $x_3\ x_2\ x_1\ x_0$ to produce sum and carry.

Q.2(e) Draw the logic diagram of a 2 to 4 line decoder using NOR gates only with enable input.

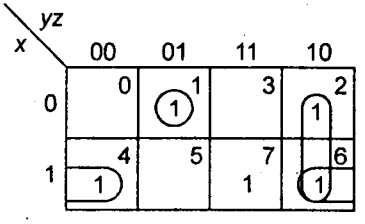
Ans.



Q.2(f) Implement the following two Boolean functions with a PLA.

$F_1(x, y, z) = \Sigma m(1, 2, 4, 6)$ $F_2(x, y, z) = \Sigma m(0, 1, 6, 7)$

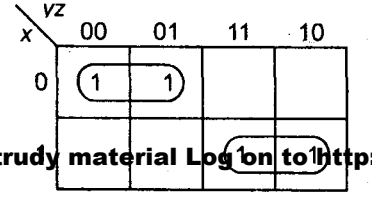
Ans. $F_1(x, y, z) = \Sigma m(1, 2, 4, 6)$

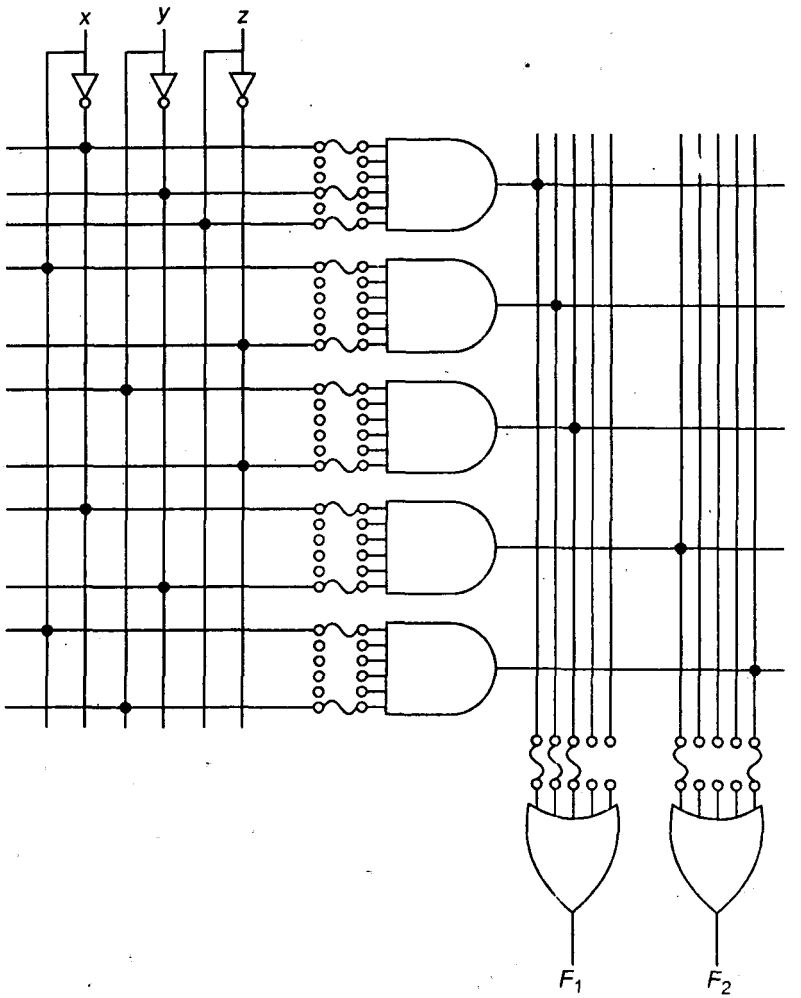


$$F_1 = \bar{x}\,\bar{y}\,z + x\bar{z} + y\bar{z}$$

$$f_2(x, y, z) = \Sigma m(0, 1, 6, 7)$$

$$F_2 = \bar{x}\,\bar{y} + xy$$





Q.3. Attempt any two parts of the following : $10 \times 2 = 20$

Q.3. (a) Explain the difference among a boolean equation, a state equation, a characteristic equation and a flip flop input equation.

Ans. Boolean Equation—Boolean equation for a gate may be defined as the equation relating input and output terms.

State equation—State equation is defined as the equation that gives the value of next state of a flip flop. While its present state is known.

Characteristic Equation—Characteristic equation is a relationship between inputs and outputs of a combinational circuit.

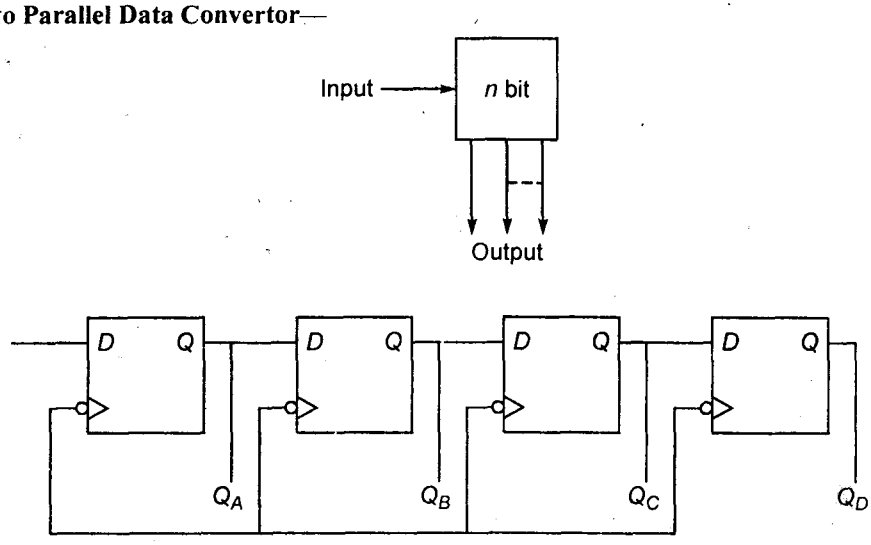
Flip Flop Input Equation—This equation is the relationship between input and output of a flip flop.

Q.3(b) What is the difference between serial and parallel transfer ? Explain how to convert serial data to parallel and parallel data to serial. What types of register is needed ?

Ans. If a register shifts 1 bit at a time for each clock pulse then it is called serial shifting of data.

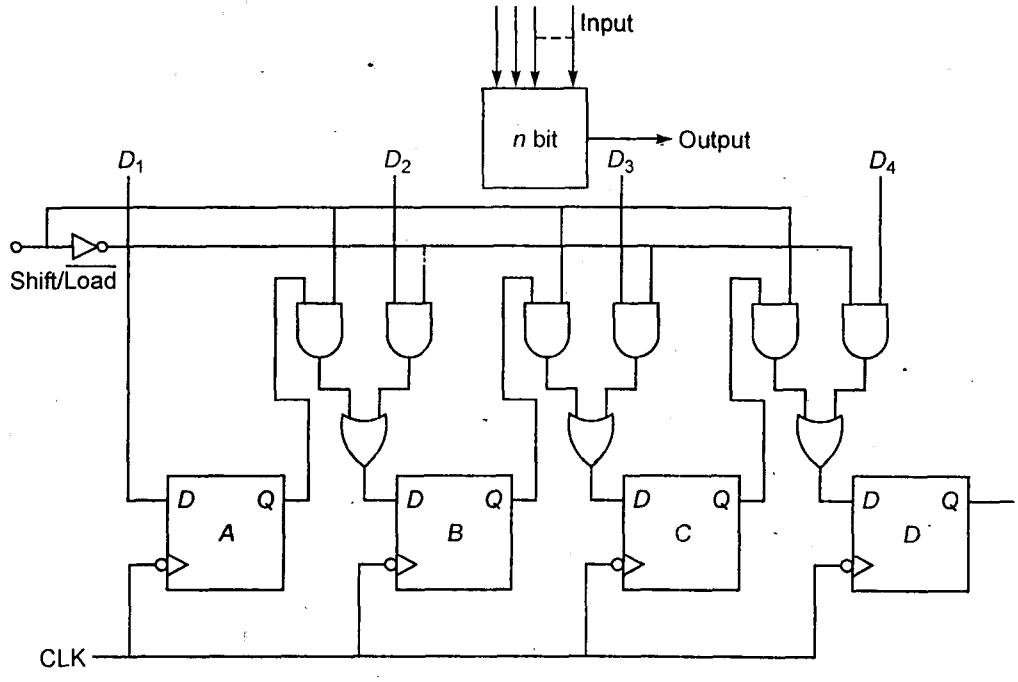
In parallel data shifting all the data input is shifted simultaneously during one clock pulse. Hence the parallel shifting of data is much faster than the serial data shifting.

Serial to Parallel Data Convertor—



Serial to Parallel data convertor

Parallel to Serial Data Convertor—

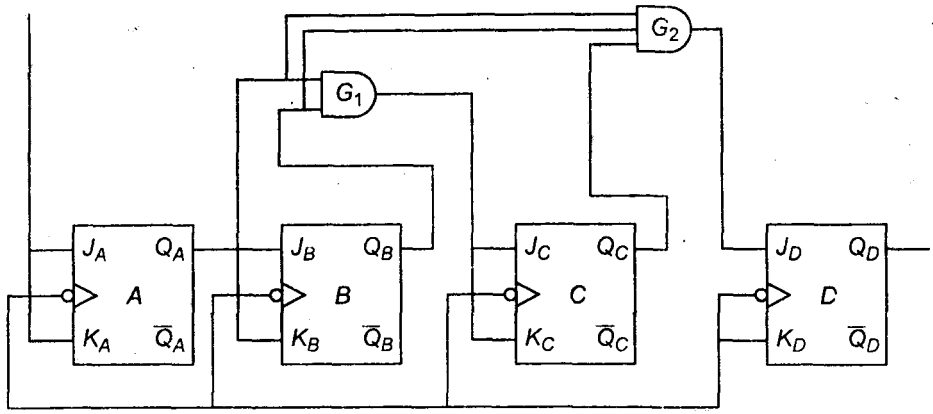


Parallel to serial data convertor

In this register data is entered simultaneously into each of its flip flops of parallel lines.

Q.3(c) Design a 4 bit synchronous binary counter using J-K flip-flops.

Ans. Figure shows a schematic diagram for a 4 bit synchronous counter. As the counter is implemented with negative edge triggered flip flops, the transitions occur at the negative edge of the clock.



Logic Diagram for 4 bit synchronous counter

The following table shows the count sequence of 4 bit synchronous counter from this truth table.

Count	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Q.4. Attempt any two parts of the following : **$10 \times 2 = 20$**

(a) Write short notes on the following :

(i) Random Access Memories

(ii) Memory Organization

Ans. (i) Random Access Memory—We can access the data randomly from any location of memory. The access time for each content is same for all the locations. It is also known as Read and write memory. We can read the data from the specific location of memory and also write the data into a specific memory location.

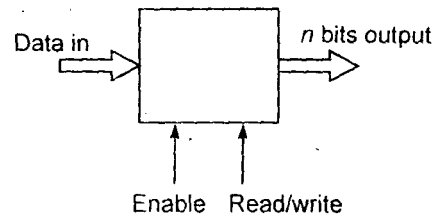


Figure shows the block diagram of RAM.

The two categories of RAM are :

(i) Static RAM (SRAM)

(ii) Dynamic RAM (DRAM)

Static RAM uses flip flops AS storage elements and dynamic RAM uses capacitors as storage elements.

Both static and dynamic RAM will loss stored data when the power is removed. So the RAM is vollatile memory.

(ii) Memory Organization—The basic elements of semiconductor memory is a flip flop. The information is stored in binary form. There are no. of locations in a memory ship each location is meant for one word a digital information. The no. of locations and the no. of bits compromising the word vary from memory to memory. The size in a memory chip is specified by two no. M and N. Where

$M \rightarrow$ No. of locations

$N \rightarrow$ No. of bits of each location.

Each of M locations of memory is defined for unique address and therefore for accessing anyone of the M locations. P inputs are required where $2P = M$.

The no. of inputs required to store the data from each memory locations is N. One set of N lines is required for storing the data into the memory referred to as data inputs and another set of N lines is required for reading the data stored in the memory referred to as data output.

Q.4(b) A symmetrical square wave of peak-to- peak amplitude V and frequency f is applied to a high pass RC circuit. Show that the percentage tilt is given by

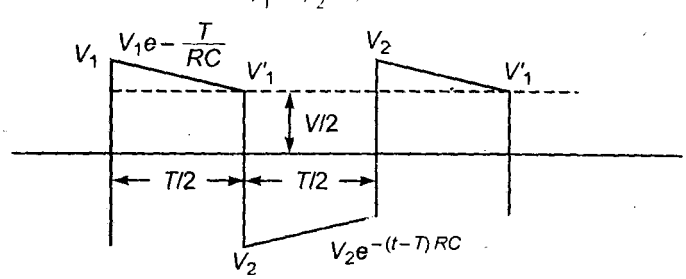
$$P = \frac{1 - e^{-\frac{1}{2}/RC}}{1 + e^{-\frac{1}{2}/RC}} \times 200\%$$

Ans.

$$V_1' = V_1 e^{T_1/RC}$$

$$V_2' = V_2 e^{T_2/RC}$$

$$V_1' - V_2' = V$$



A symmetrical sequences has $T_1 = T_2 = \frac{T}{2}$

Under these conditions both the above eqn. are identical, hence either of two equation are sufficient to find output

$$= V_1 e^{-T_1/RC} + V_1 = V \text{ (Using above conditions)}$$

Similarly, $$V_1' = \frac{V}{1 + e^{T/2RC}}$$

The effect of $RC\ N/W$ is to introduce a tilt in the waveform % tilt is defined by

$$P = \frac{V_1 - V_1'}{V/2} \times 100\%$$

$$= \frac{\left[\frac{V}{1 + e^{-T/2RC}} - \frac{V}{1 + e^{T/2RC}}\right]}{V/2} \times 100\%$$

$$= \left[\frac{\frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} - \frac{v}{1 + e^{T/2RC}}}{V/2}\right] \times 100\%$$

$$= \frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} \times 200\%$$

$$= \frac{1 - e^{-1/2fRC}}{1 + e^{-1/2fRC}} \times 200\%$$

Q.4(c) What are the various types of A/D converter ? Explain any one of them with a neat block diagram in detail.

Ans. Various A/D Convertor—Some types of A/D convertors are :

(i) Successive Approximation type ADC

(ii) Single Ramp type ADC

(iii) Dual Slope type ADC

(iv) Flash type ADC

(v) Delta modulation type ADC

Successive Approximation Type ADC —

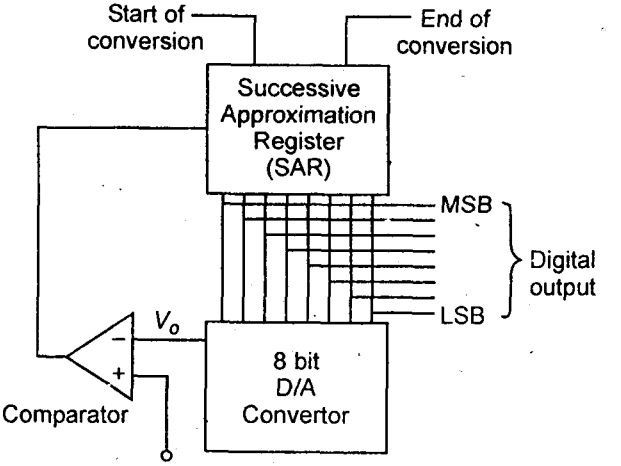
A successive approximation type ADC is shown in figure. It has 3 main parts are :

(i) Successive Approximation Register

(ii) Digital to Analog Convertor

(iii) Comparator

The main block of ckt is an 8 bit successive approximation register (SAR) whose o/p is applied to an 8 bit digital to analog convertor. Then the



Block Diagram of S/A Type TDC

analog o/p (V_0) of DAC is compared to an analog input signal V_{in} by the comparator. The o/p of the comparator is a serial data input to the SAR. Then SAR adjusts its digital o/p bits until it is equivalent to analog input V_{in}.

Q.5 Attempt any two part of the following : $10 \times 2 = 20$

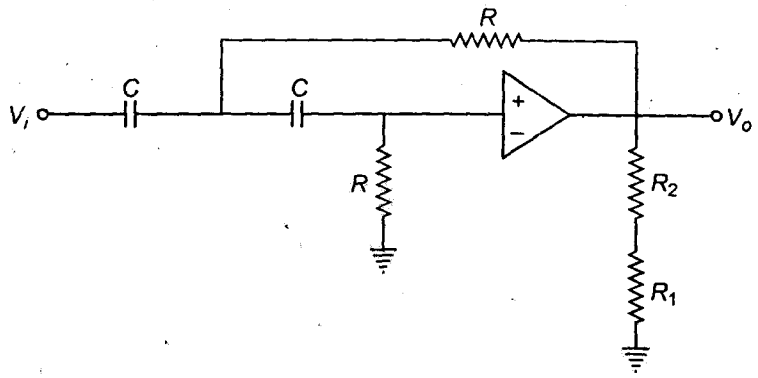
Q.5. (a) What do you mean by active filter ? Design an active second order high pass filter at a cut-off frequency of 2 kHZ.

Ans. Active filter—A filter is a ckt that is designed to pass a speacified band of frequency while attenuating all the signals outside that bond. It is a frequency selective ckt.

The filters are basically classified as active filters and passive filters. The passive filter *n/w* use only passive elements such as resistors, inductors, and capacitors.

On the other hand, active filter ckt use the active elements such as op amps transistor along with resistors, inductors, and capacitors.

Designing of 2 nd order high pass Filter—



$$\omega = \frac{1}{RC}$$

$$R = \frac{1}{2\pi fC}$$

$$= \frac{1}{2\pi \times 0.1 \times 10^{-6} \times 2 \times 10^3} = 7.96\ \text{K}\Omega$$

$$A_0 = 3 - a$$

$$a = \sqrt{2} = 1.414$$

$$A_0 = 3 - 1.414 = 1.586$$

$$R_1 = 20\,\text{K}\Omega$$

$$R_2 = (1.586 - 1) \times 20 \times 10^3$$

$$= 11.36\ \text{K}\Omega$$

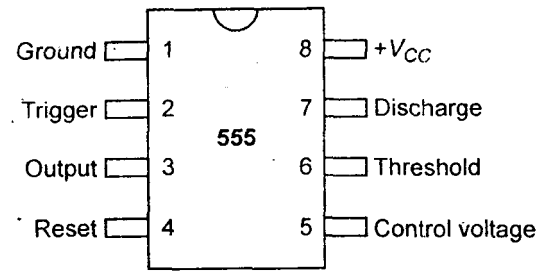
Q.5. (b) Describe with a neat sketch the function of each pin in 555 timer. Explain how will you connect it to perform as a monostable multivibrator ? Also draw the input and output waveforms of the circuit.

Ans.

Pin-1 : It is the ground pin.

Pin-2 : It is an input pin. The voltage given to this pin controls the state of output.

Pin-3 : Output is obtained at this pin.



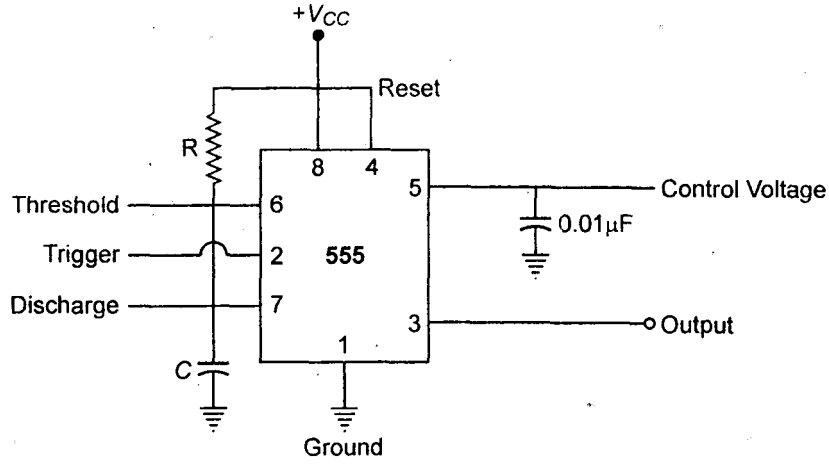
Pin-4 : This pin is used to reset the operation of flip flop.

Pin-5 : The width of output pulse is controlled by the voltage of this pin.

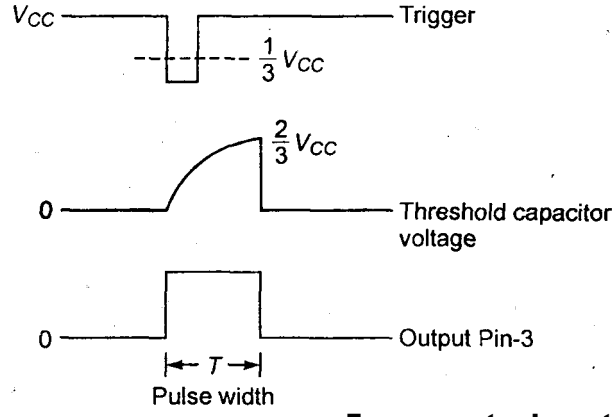
Pin-6 : By applying voltage on this pin the voltage across externally connected capacitor is varied.

Pin-7 : By this pin externally connected capacitor is discharged.

Pin-8 : This pin used to give V_{CC} to the *IC*.



IC-555 as monostable multivibrator



Input Output waveforms of - 555

Q.5(c) Describe an adjustable voltage IC regulator. Also draw the explain the typical connection diagram for the regulator.

Ans. Adjustable Regulators

A number of IC regulators (LM 317, LM 337, LM338 and LM350) are adjustable. These have maximum load currents from 1.5 to 5A. For instance, the LM317 is a three-terminal positive voltage regulator that can supply 1.5 A of load current over an adjustable output range of 1.25 of 37V. The ripple rejection is 80 dB. This means that the input ripple is 10,000 smalie at the output of the IC regulator.

Again, manufactures redefine the load and line regulation to suit the characteristics of the IC regulator. Here are definitions for load and line regulation used on the data sheets of adjustable regulators :

Load regulation = Percent change in V_{out} for a range in load current

Line regulation = Percent change in V_{out} per volt of input change

For instance, the data sheet of an LM317 lists typical load and line regulations :

Load regulation = 0.3% for I_L = 10 mA to 1.5A

Line regulation = 0.02% per volt

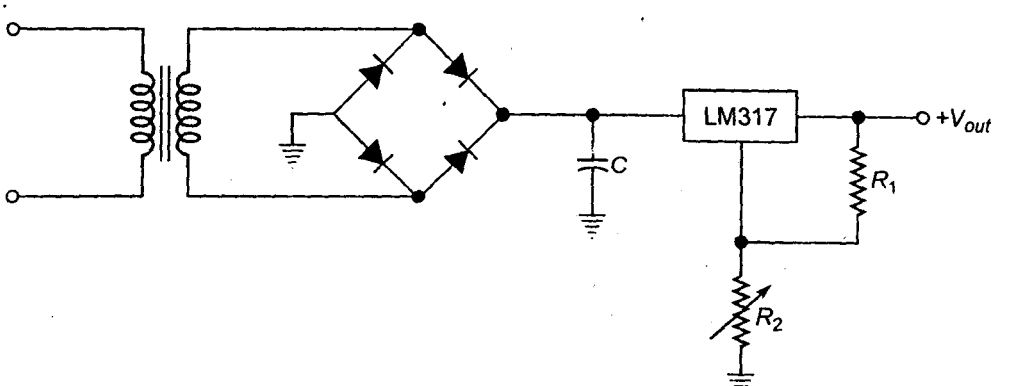
Since the output voltage is adjustable between 1.25 and 37V, it makes sense to specify the load regulation as a percent. For instance, if the regulated voltage is adjusted to 10V, the foregoing load regulation means that the output voltage will remain within 0.3 percent of 10V (or 30 mV) when the load current changes from 10 mA to 1.5A.

The line regulation is 0.02 percent per volt. This means that the output voltage changes only 0.02 percent for each volt of input change. If the regulated output is set at 10V and the input voltage increases by 3V, the output voltage will increase by 0.06 percent, equivalent to 60 mV.

Figure... shows an unregulated supply driving an LM317 circuit. The datesheet of ... gives this formula for output voltage :

$$V_{out} = \frac{R_1 + R_2}{R_1} V_{ref} + I_{ADJ} R_2 \qquad ...(1)$$

In this equation, V_{ref} has a value of 1.25 V and I_{ADJ} has a typical value of 50 μA. In Fig..., I_{ADJ} is the current flowing through the middle pin (the one between the input and the output pins). Because this current can change with temperature, load current, and other factors, a designer usually makes the first them in Eq.... much greater than the second. This is why we can use the following equation for all preliminary analyses of an LM317.



$$V_{out} = \frac{R_1 + R_2}{R_1} (1.25\ V) \qquad ...(2)$$

Ripple Rejection

The ripple rejection of an IC voltage regulator is high, from about 65 to 80 dB. This is a tremendous advantage because it means that we do not have to use bulky *LC* filters in the power supply to minimize the ripple. All we need is a capacitor-input filter that reduces the peak-to-peak ripple to about 10 percent of the unregulated voltage out of the power supply.

For instance, the LM7805 has a typical ripple rejection of 80 dB. If a bridge rectifier and a capacitor-input filter produce an unregulated output voltage of 10V with a peak-to-peak ripple of 1V, we can use an LM 7805 to produce a regulated output voltage of 5V with a peak-to-peak ripple of only 0.1 mV. Eliminating bulky *LC* filters in an unregulated power supply is a bonus that comes with *LC* voltage regulators.