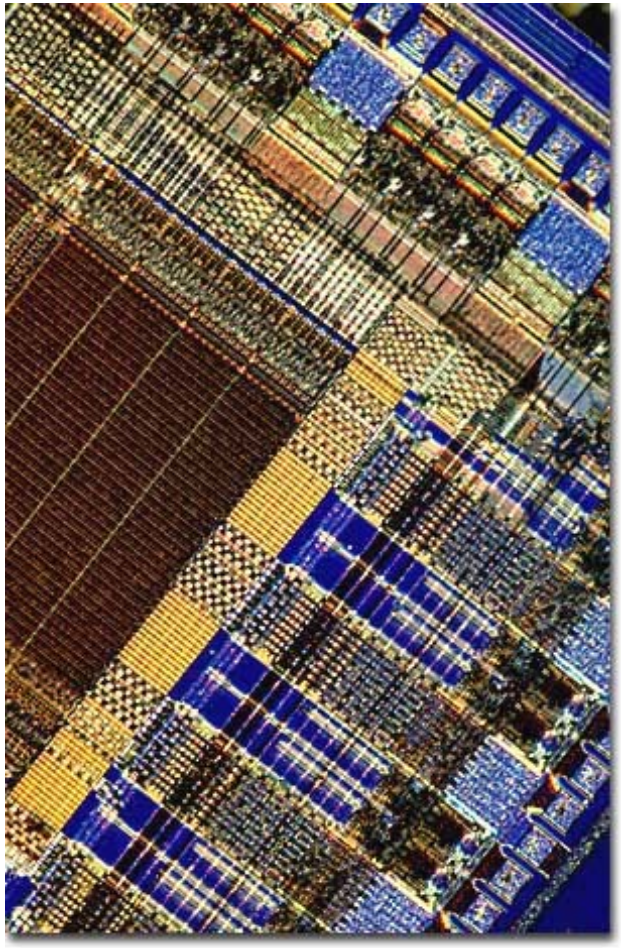
The McGraw-Hill Companies

CMOS Digital Integrated Circuits



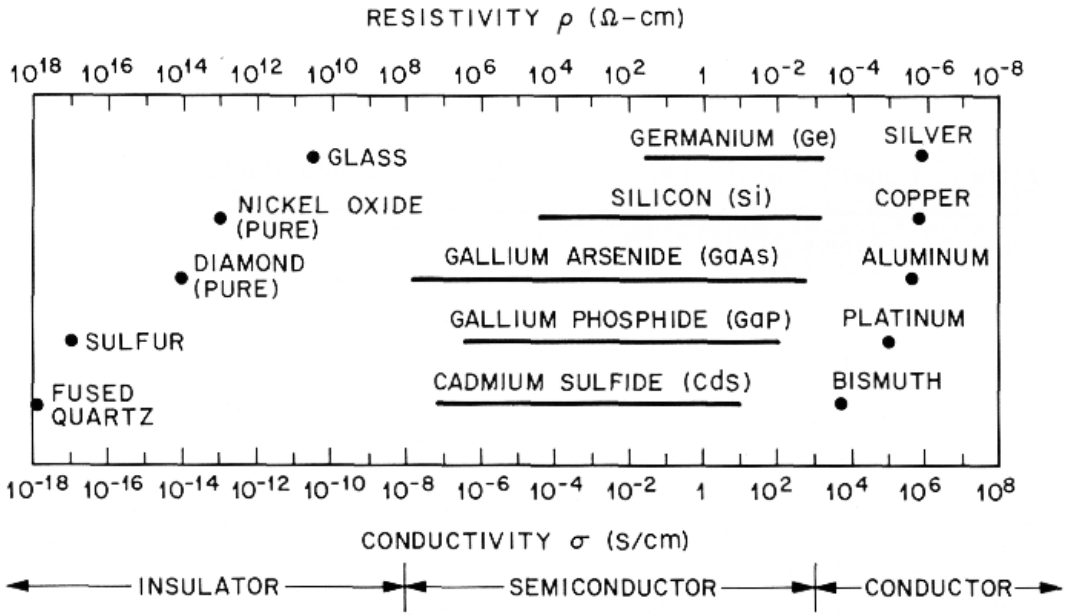
Chapter 2
Fabrication of MOSFETs

S.M. Kang and Y. Leblebici

Categories of Materials

Materials can be categorized into three main groups regarding their electrical conduction properties:

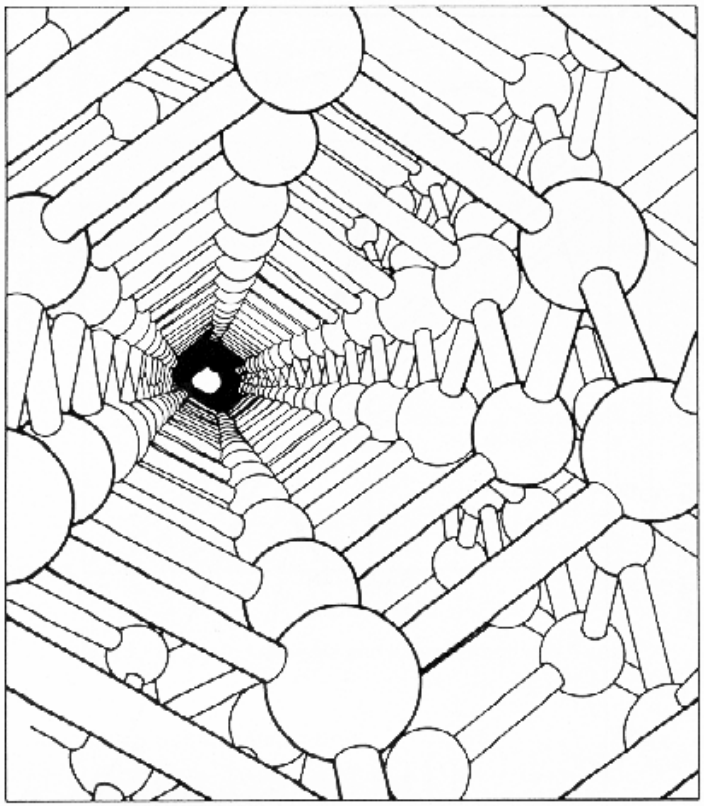
- **Insulators**
- **Conductors**
- **Semiconductors**



Semiconductors

While there are numerous semiconductor materials available, by far the most popular material is **Silicon**.

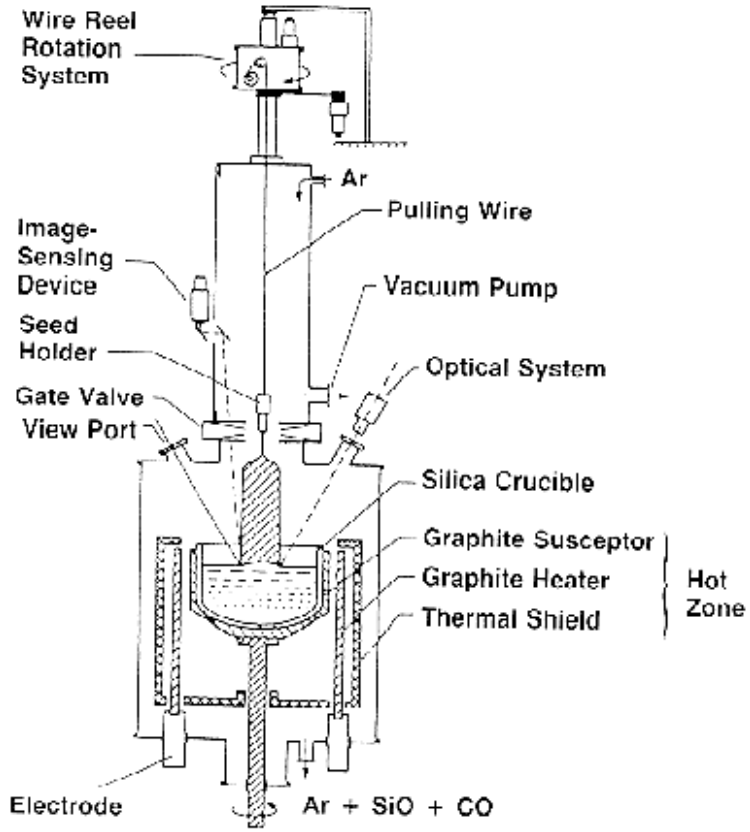
GaAs, InP and SiGe are compound semiconductors that are used in specialized devices.

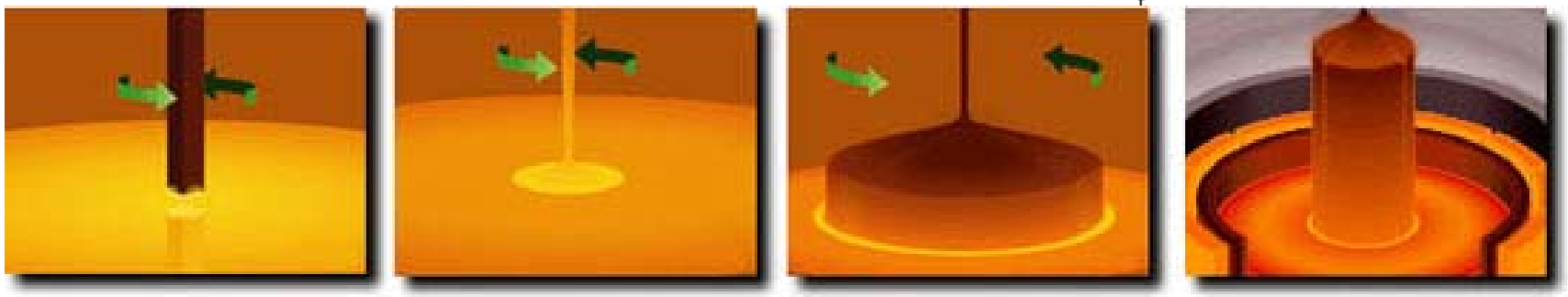


The success of a semiconductor material depends on how easy it is to process and how well it allows reliable high-volume fabrication.

Single Crystal Growth

Pure silicon is melted in a pot (1400C) and a small seed containing the desired crystal orientation is inserted into molten silicon and slowly (1mm/minute) pulled out.



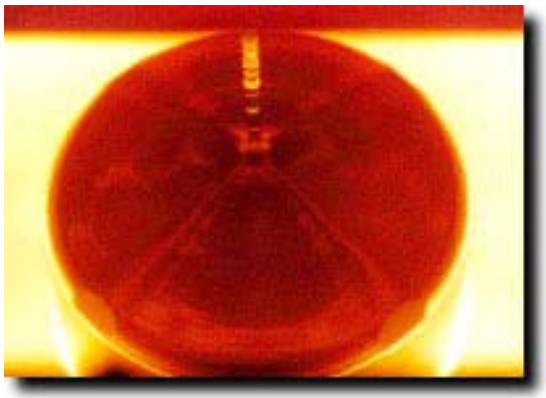


Single Crystal Growth

The silicon crystal (in some cases also containing doping) is manufactured (pulled) as a cylinder with a diameter of 8-12 inches.

Single Crystal Silicon Ingot

This cylinder is carefully sawed into thin disks (**wafers**). The wafers are later polished and marked for crystal orientation.

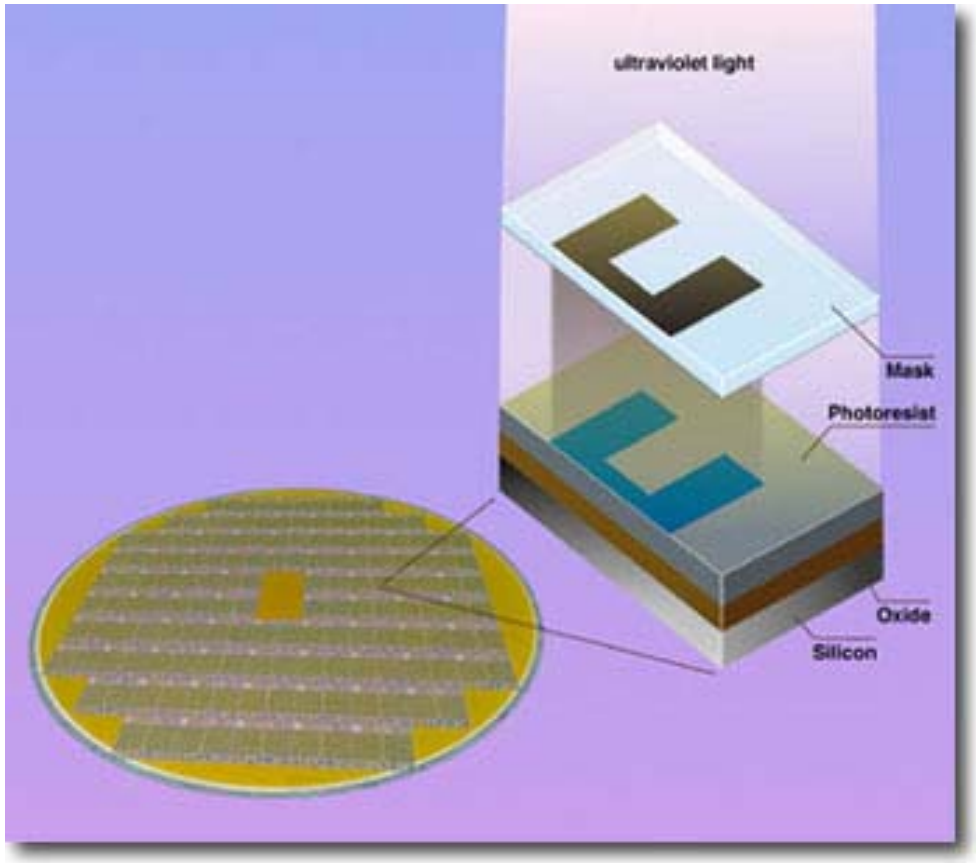


Inside CZ Puller
(MEMC)

Lithography

An IC consists of several layers of material that are manufactured in successive steps.

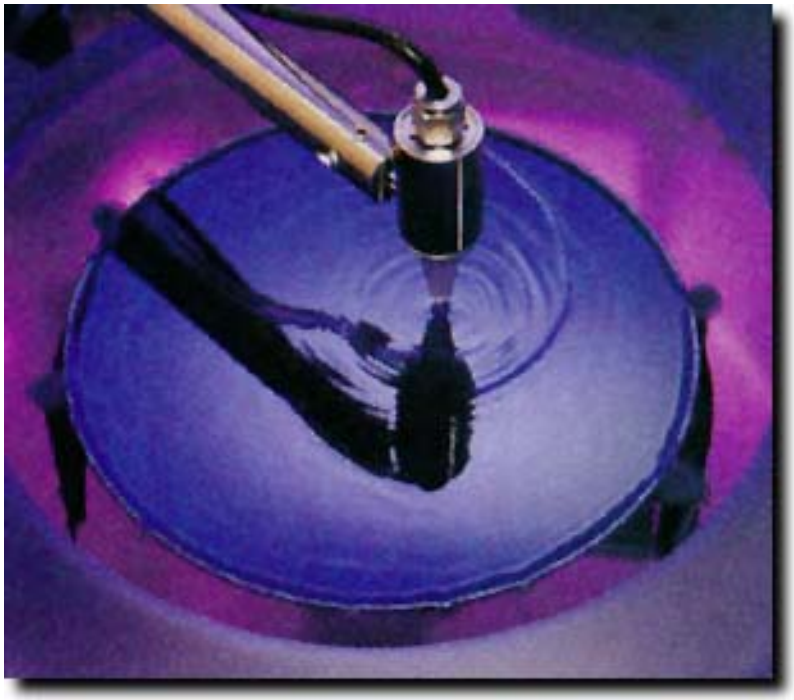
Lithography is used to selectively process the layers, where the 2-D mask geometry is copied on the surface.



Lithography

The surface of the wafer is coated with a photosensitive material, the **photoresist**. The mask pattern is developed on the photoresist, with UV light exposure.

Depending on the type of the photoresist (negative or positive), the exposed or unexposed parts of the photoresist change their property and become resistant to certain types of solvents.

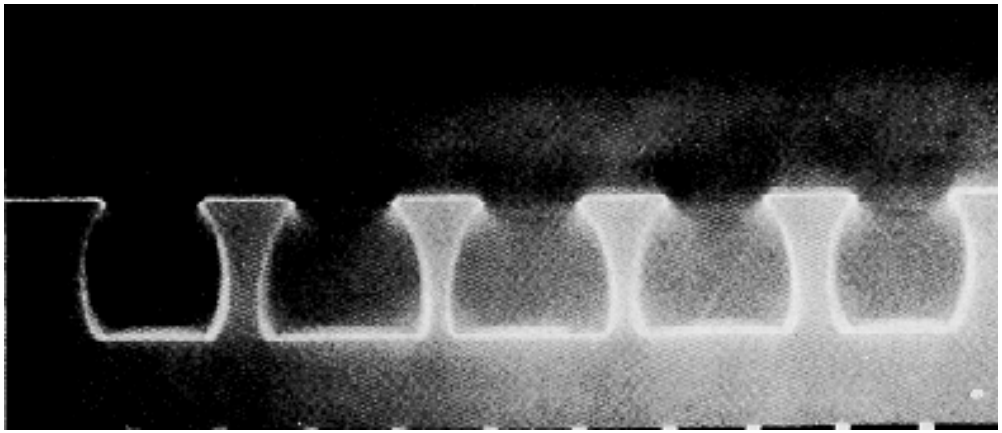


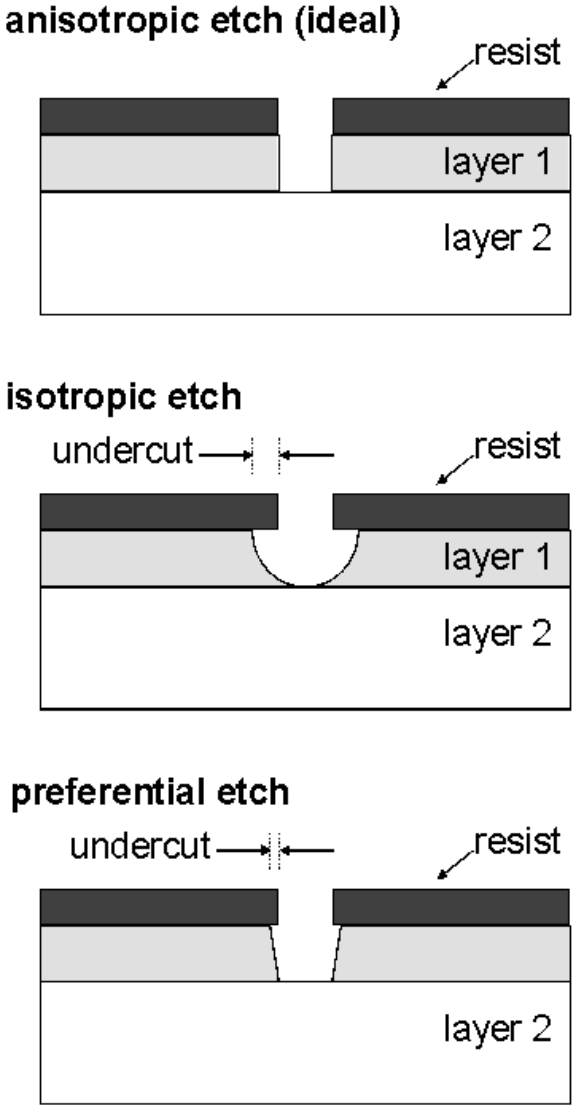
Photoresist Application
(Ontrak)

Subsequent processing steps remove the undeveloped photoresist from the wafer. The developed pattern (usually) protects the underlying layer from an etching process. The photoresist is removed after patterning on the lower layer is completed.

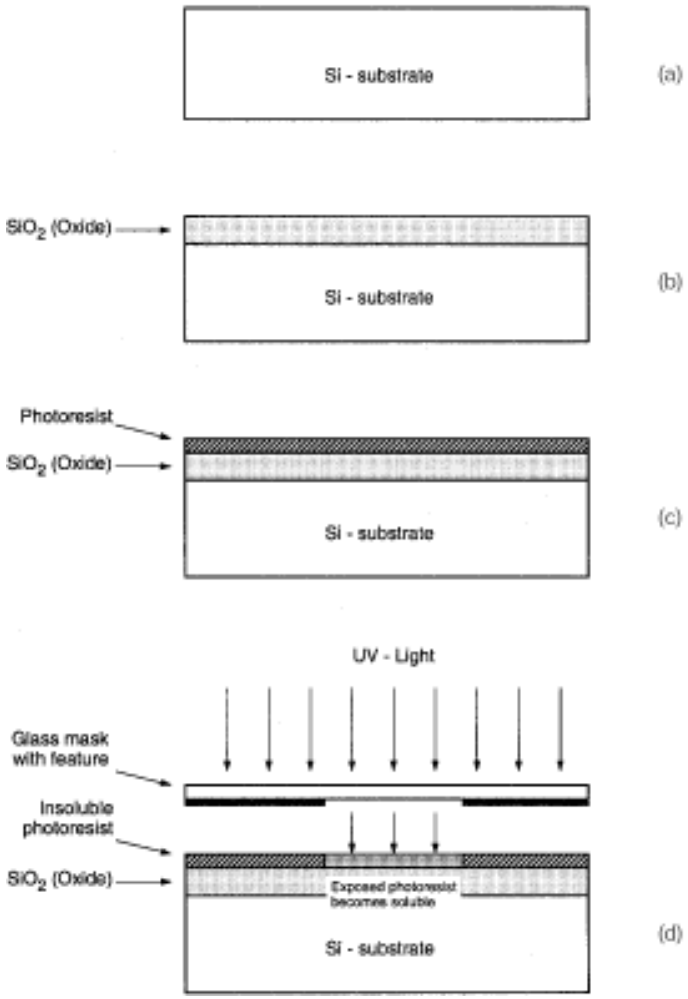
Etching

Etching is a common process to pattern material on the surface. Once the desired shape is patterned with photoresist, the unprotected areas are etched away, using wet or dry etch techniques.

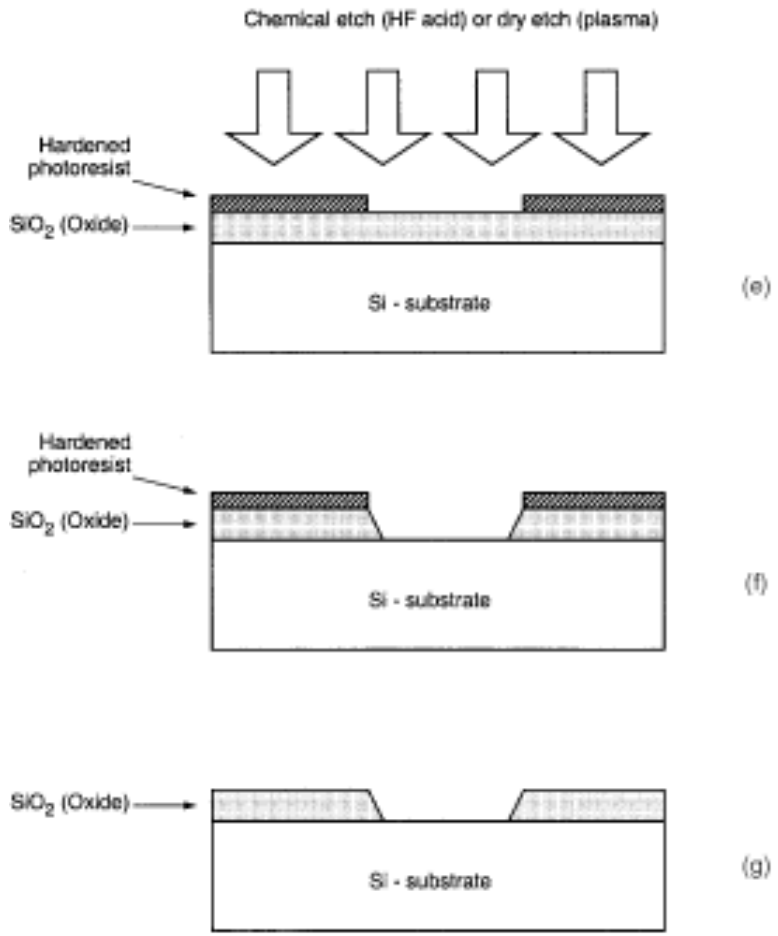




Patterning of Features on SiO_2



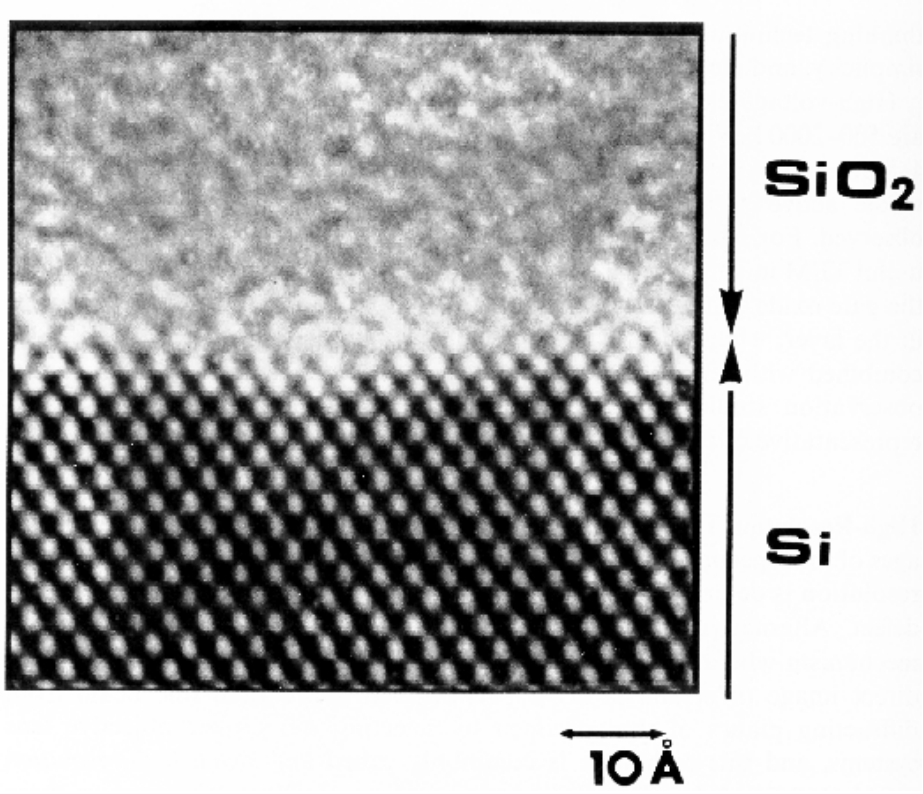
Patterning of Features on SiO_2



Oxide Growth / Oxide Deposition

Oxidation of the silicon surface creates a SiO_2 layer that acts as an insulator. Oxide layers are also used to isolate metal interconnections.

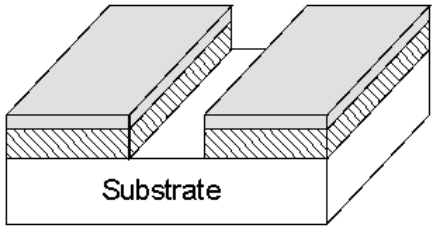
Oxidation Furnace
(Silicon Valley Group - Thermco Systems)



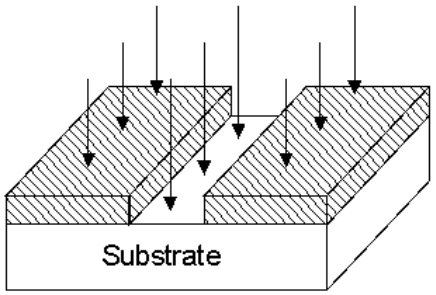
An annealing step is required to restore the crystal structure after thermal oxidation.

Ion Implantation

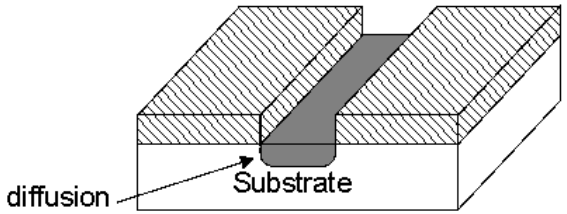
4. Etching



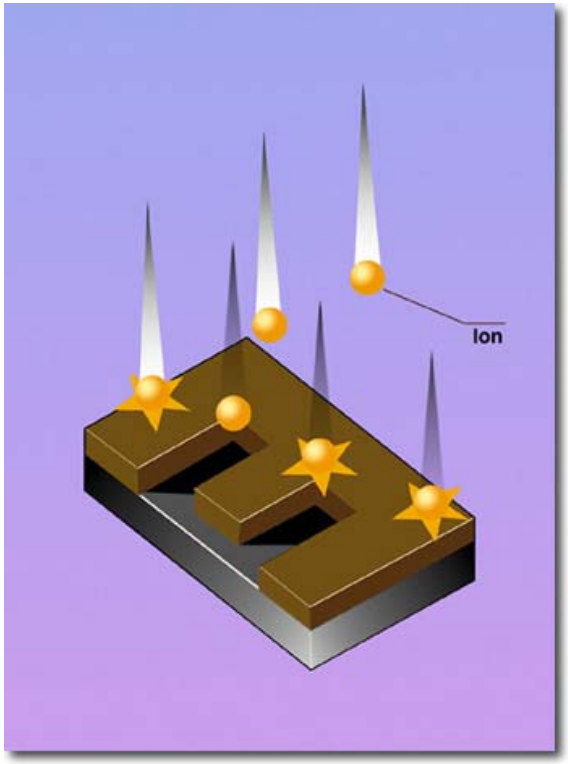
5. Ion implant



6. After doping



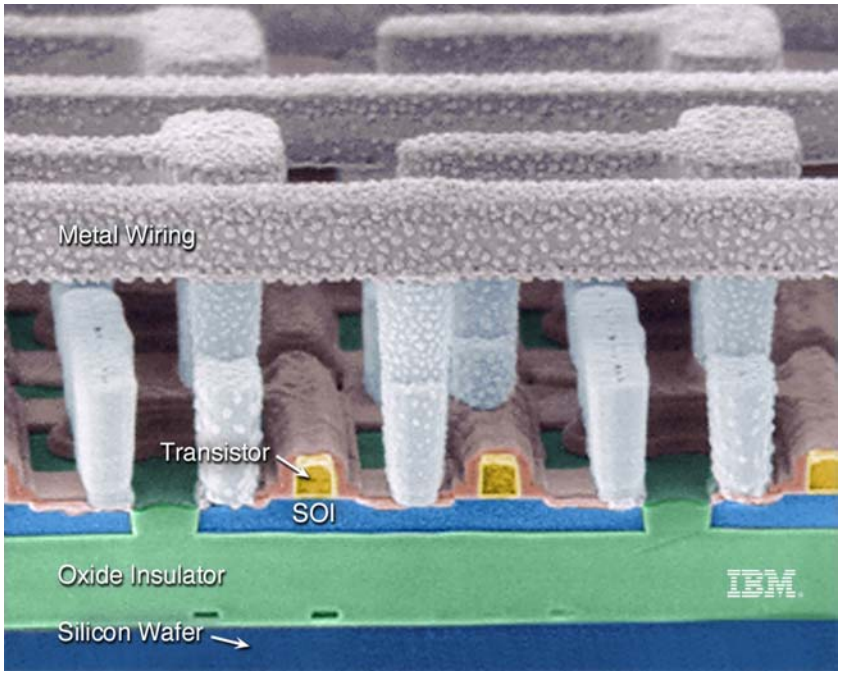
Ion implantation is used to add doping materials to change the electrical characteristics of silicon locally. The dopant ions penetrate the surface, with a penetration depth that is proportional to their kinetic energy.

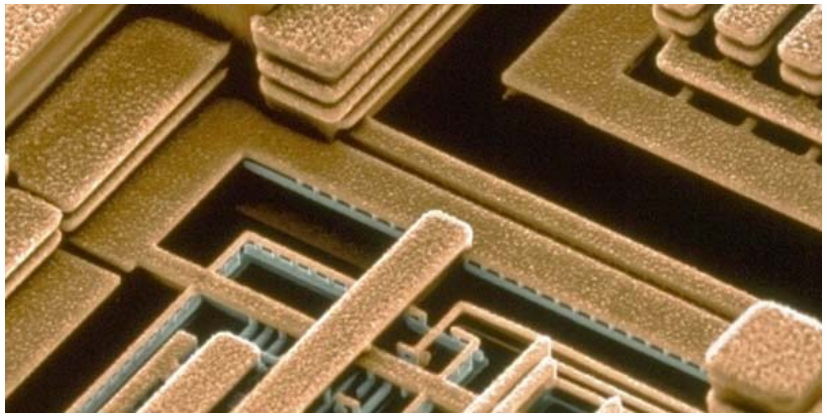


Thin Film Deposition

While some of the structures can be grown on silicon substrate, most of the other materials (especially metal and oxide) need to be deposited on the surface.

In most cases, the material that is deposited on the whole surface will be patterned and selectively etched.

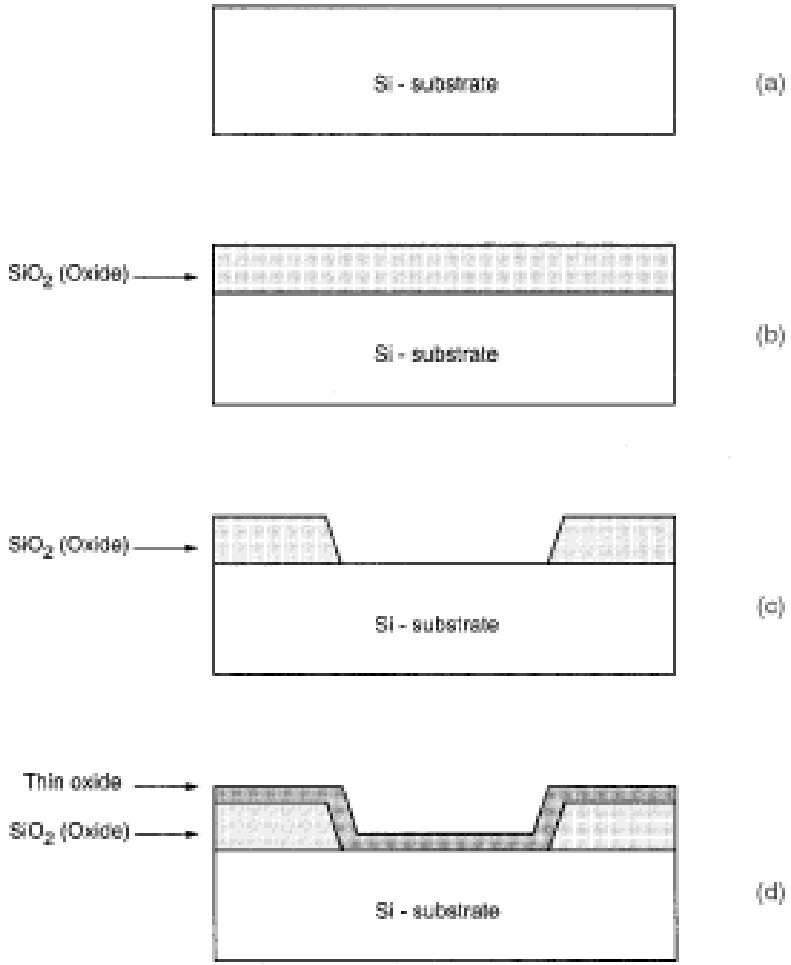




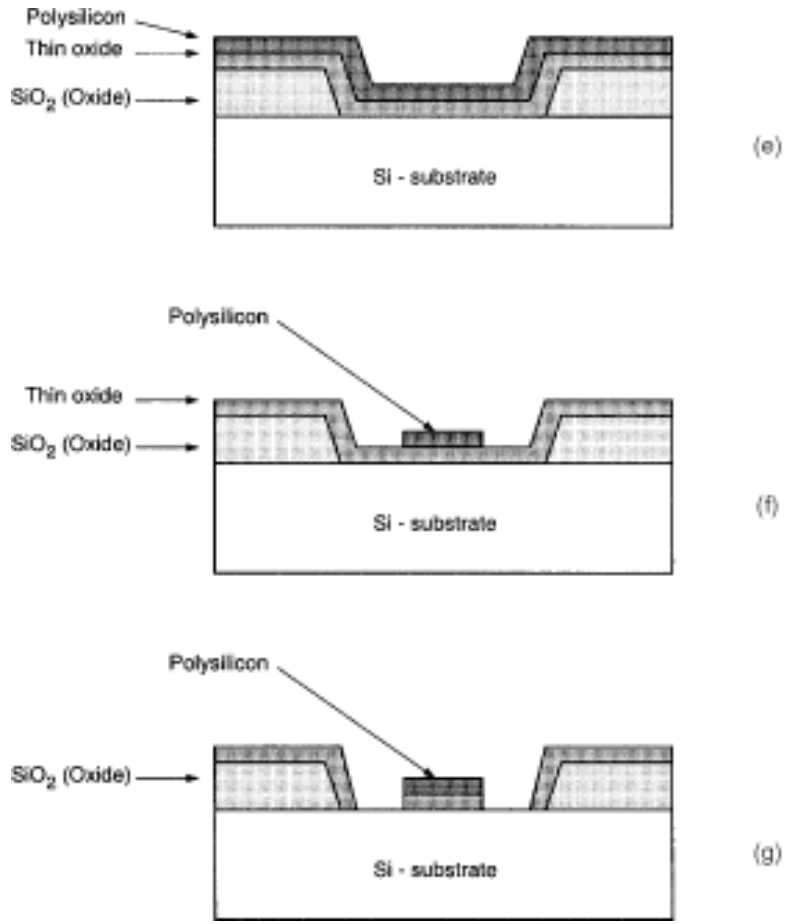
There are two main methods for thin film deposition:

- **PVD Physical Vapor Deposition**
- **CVD Chemical Vapor Deposition**

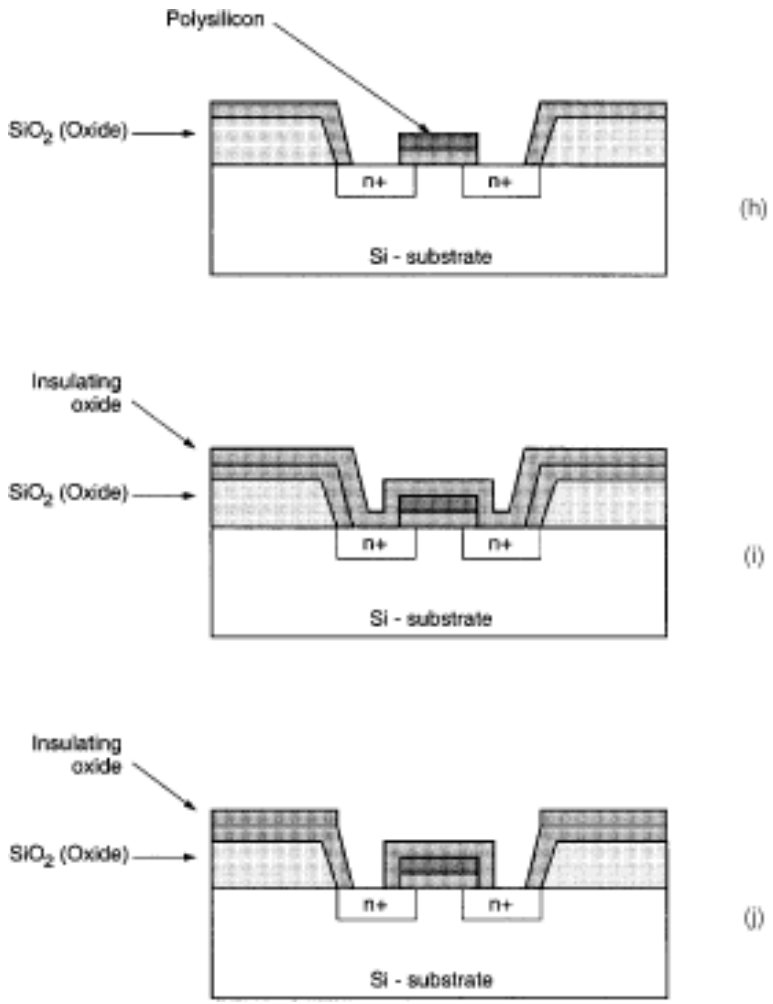
Fabrication of an nMOS Transistor



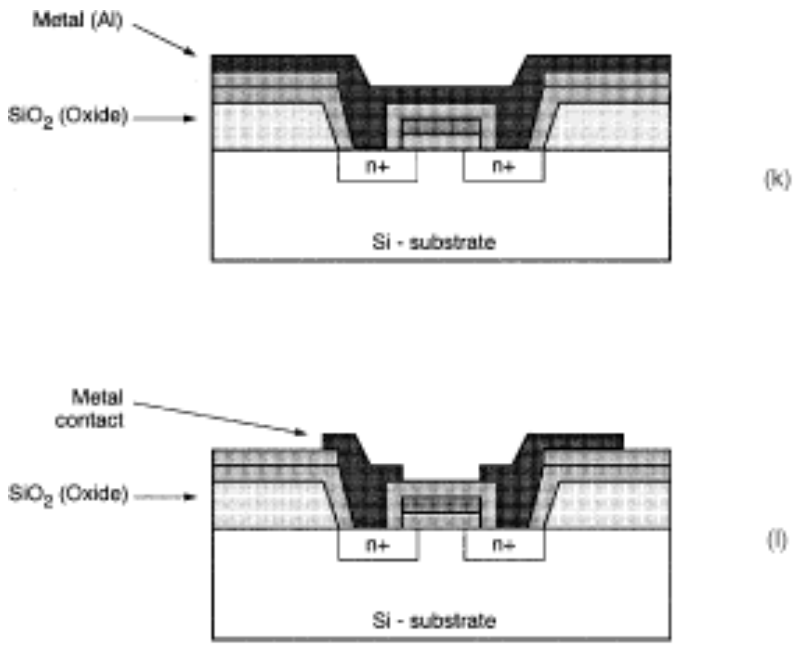
Fabrication of an nMOS Transistor



Fabrication of an nMOS Transistor

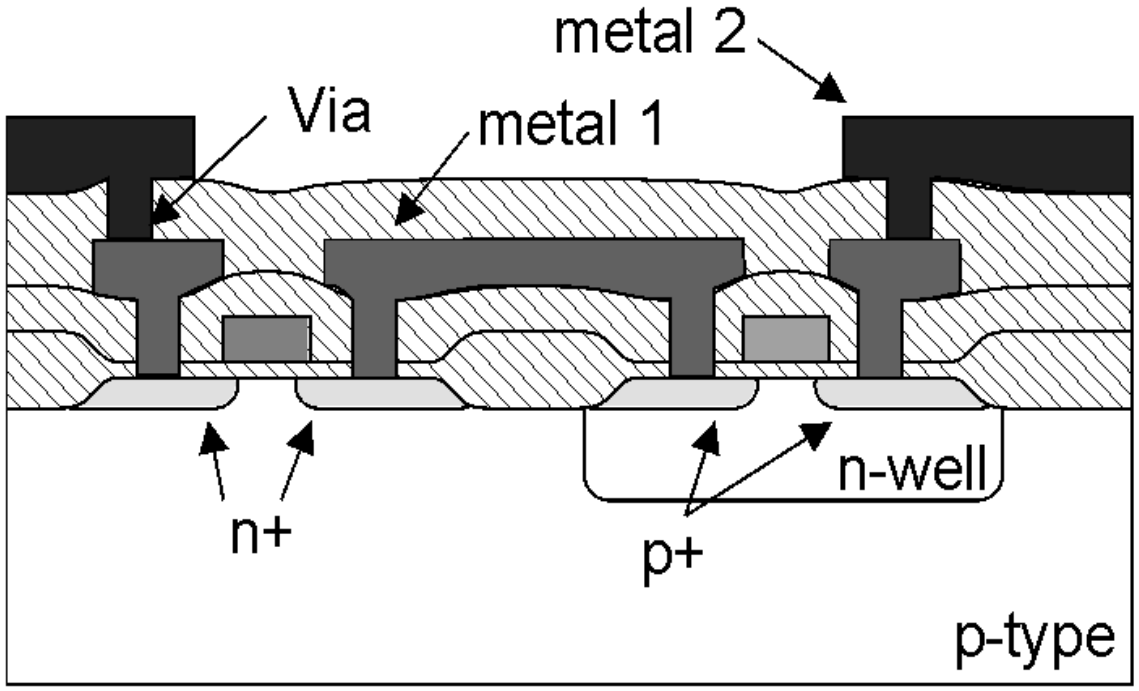


Fabrication of an nMOS Transistor

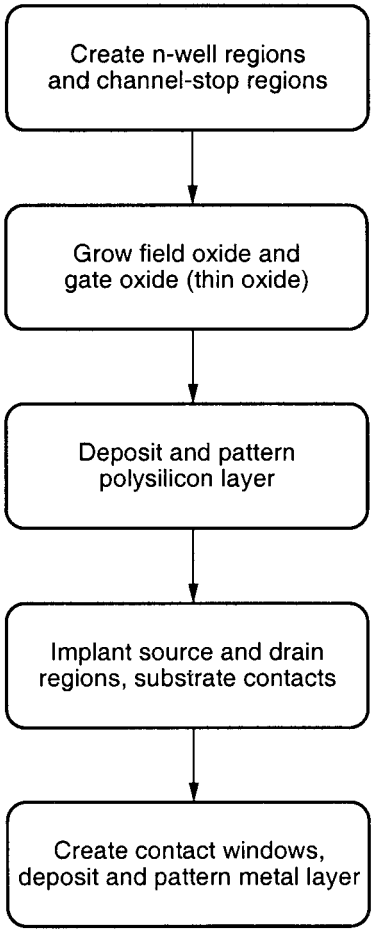


CMOS Process

The CMOS process allows fabrication of nMOS and pMOS transistors side-by-side on the same Silicon substrate.

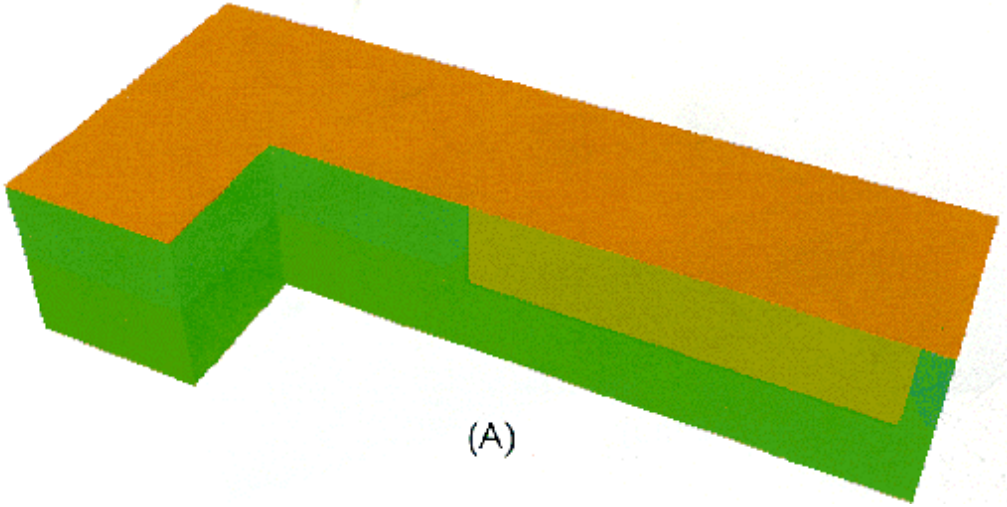


CMOS Process Flow

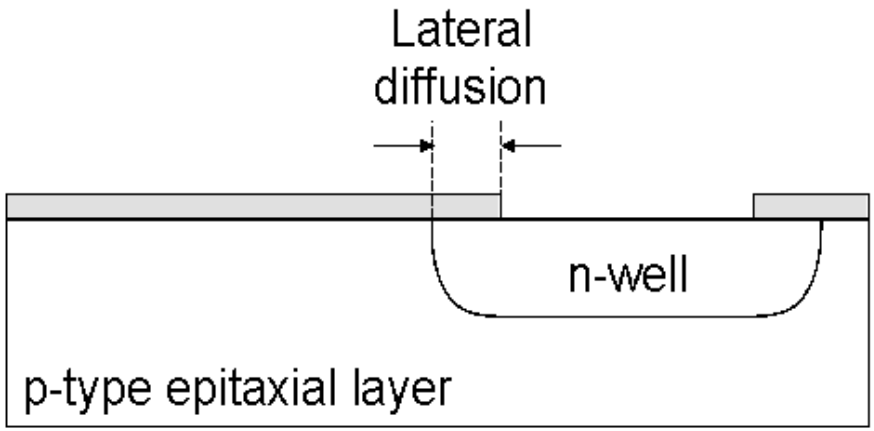


Well Creation

The first step of processing is to create a deeply implanted **n-well**.



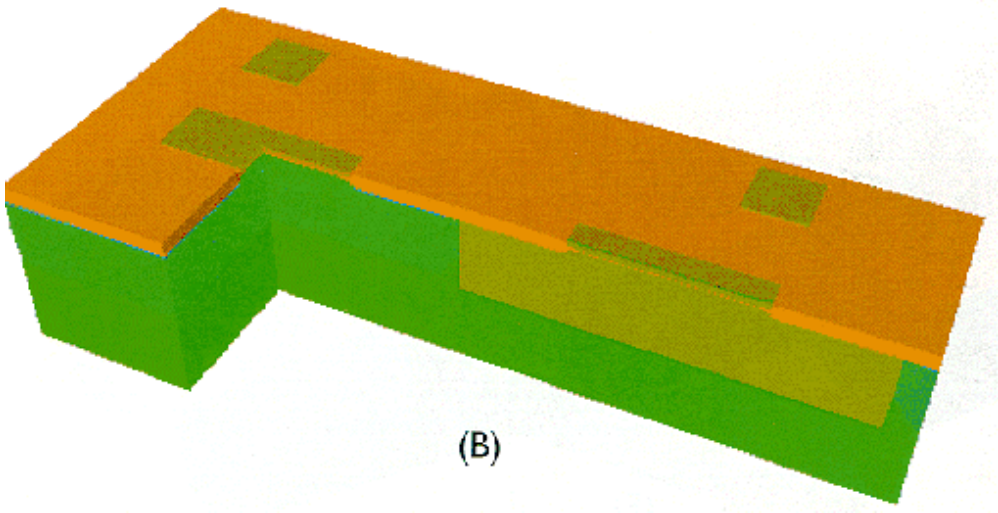
This is done either by diffusion or ion implantation.

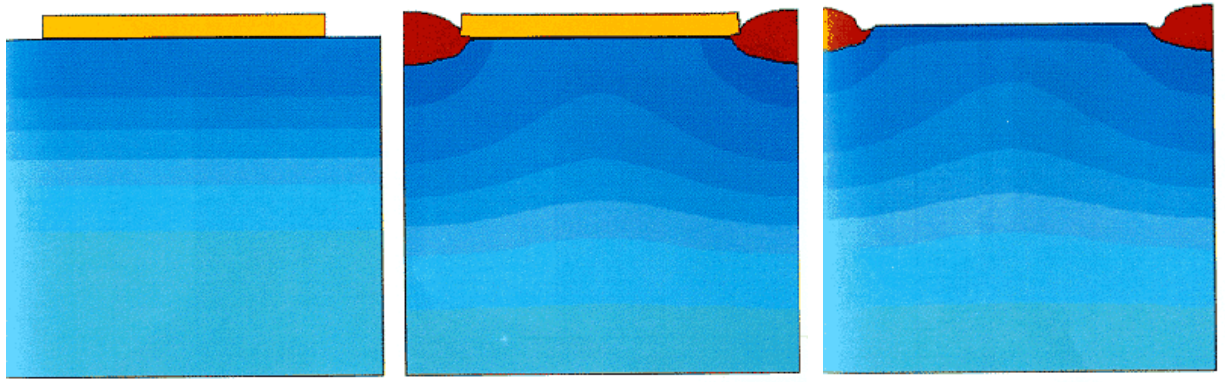


Definition of Active Areas

The next step is to define the **active** areas where the transistors will later be created.

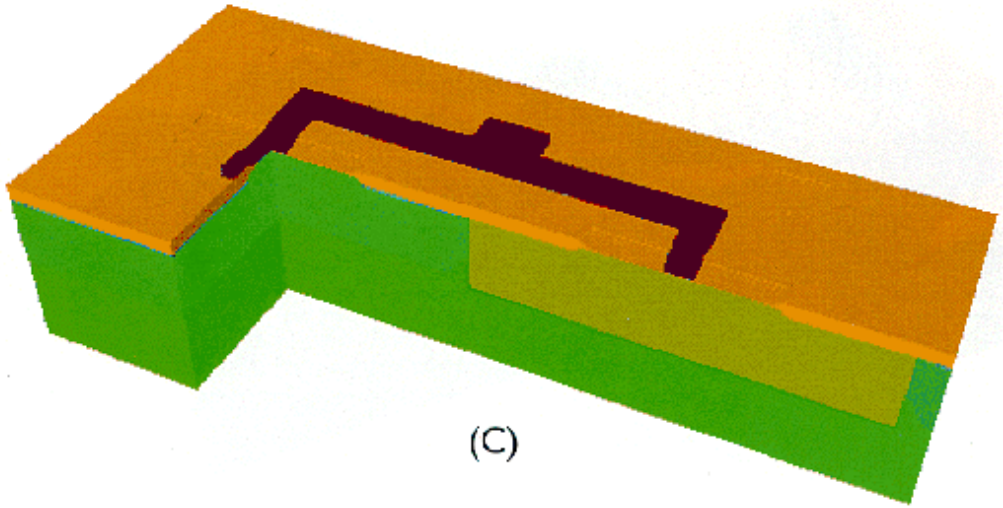
A thermal oxide is grown uniformly on the surface. Then the active areas are covered by nitride. A second thermal oxidation process grows thick silicon dioxide outside the active areas.



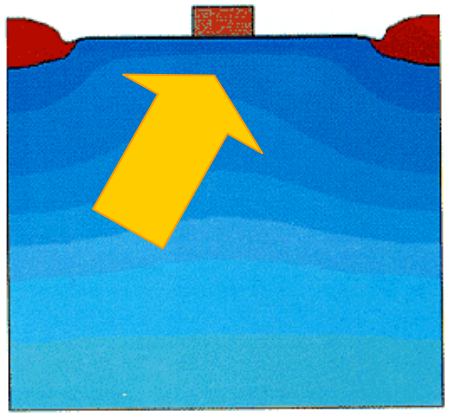


Polysilicon Deposition

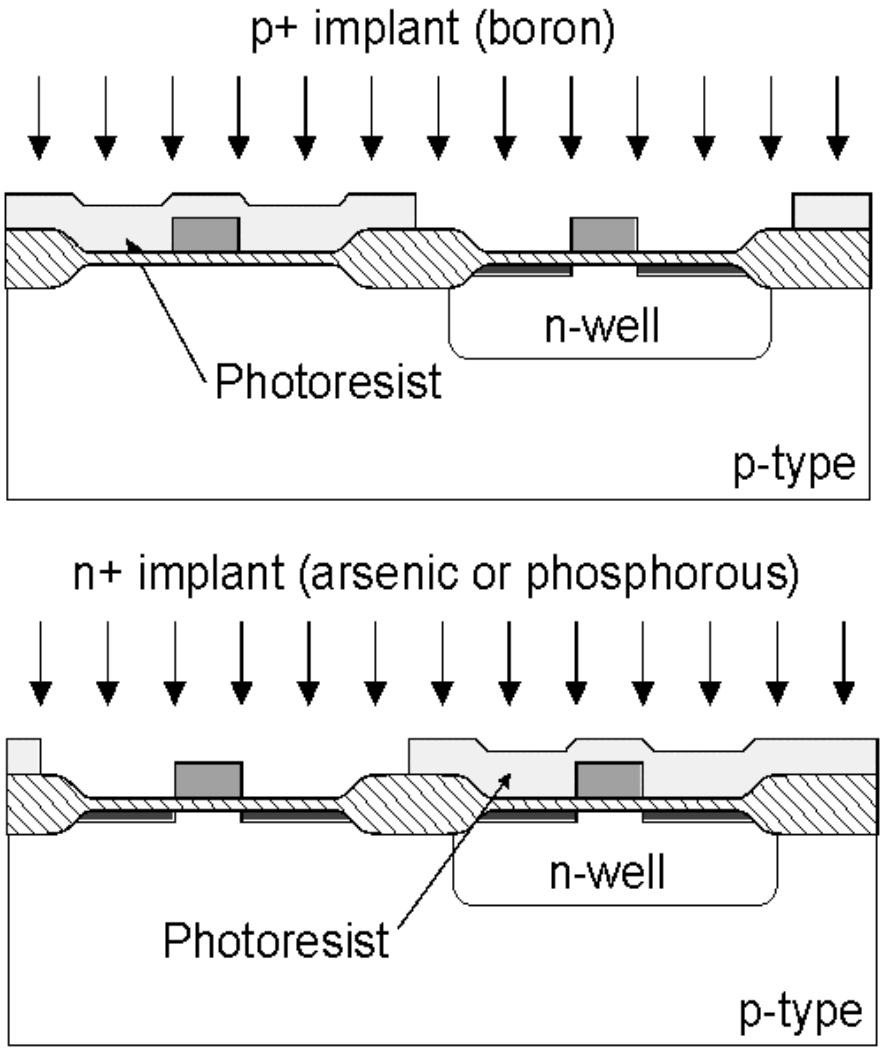
The entire surface is covered with a thin oxide layer (gate oxide).



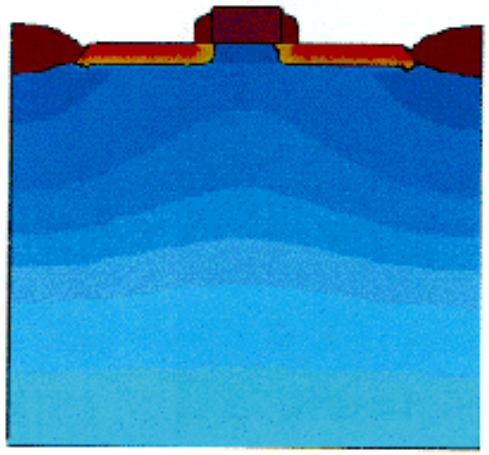
Polysilicon is deposited and patterned to form the gates of the nMOS and pMOS transistors.



Source/Drain Implantation

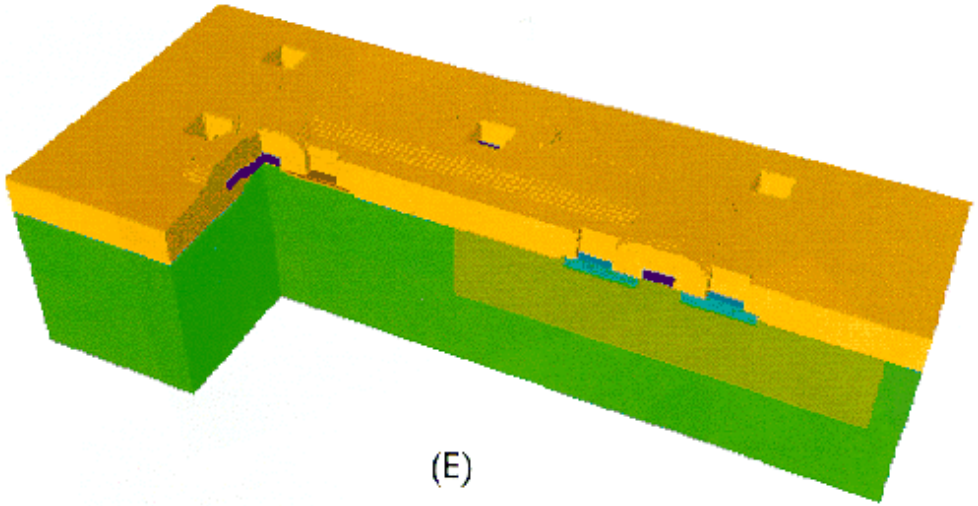


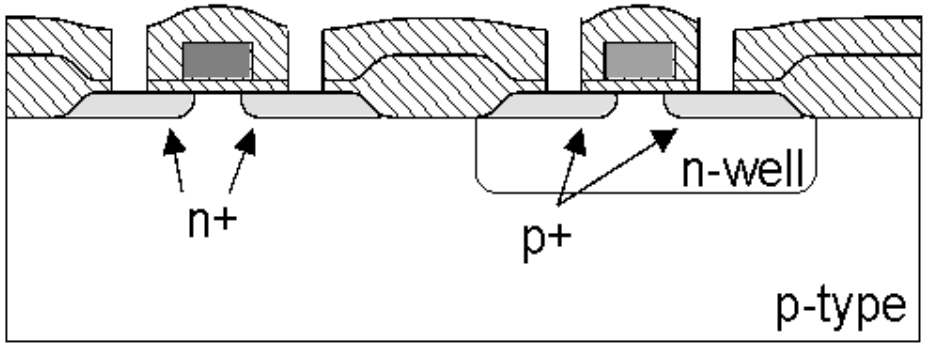
The drain and source regions of the nMOS and pMOS transistors are created by doping.

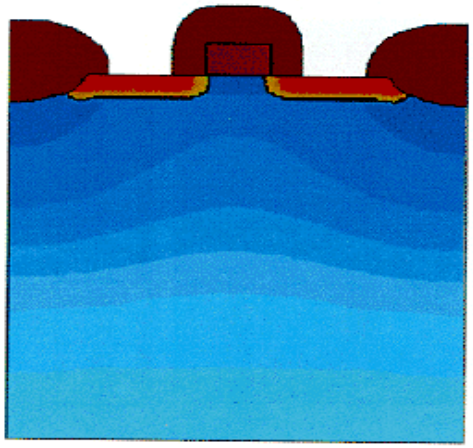


Oxide Deposition

The entire surface is covered with a field oxide and the contact holes are etched into this oxide to enable connection to the underlying layers.

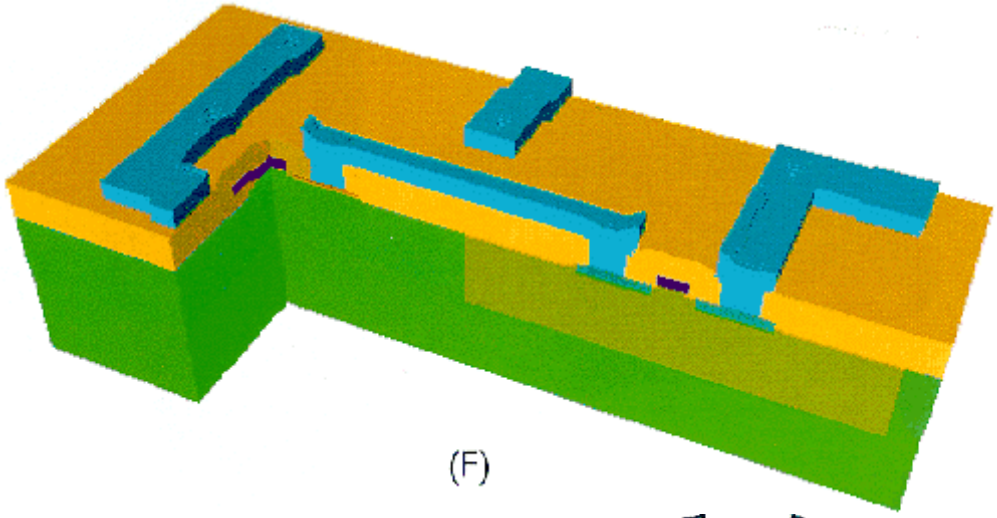




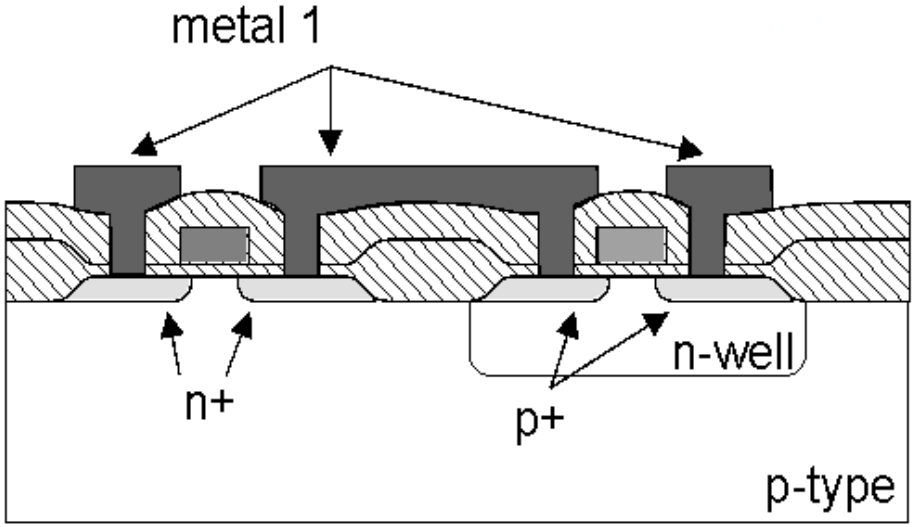


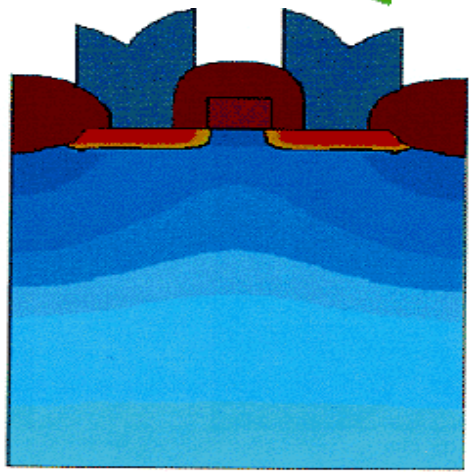
1st Level Metallization

The metal layer is deposited using a Physical Vapor Deposition (PVD) method, patterned, and etched.



(F)

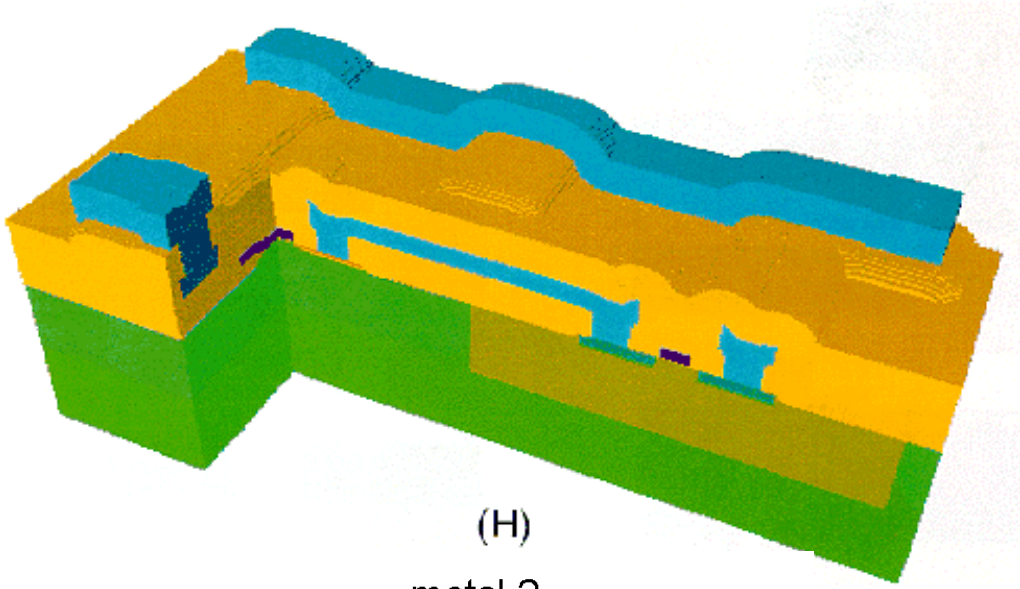




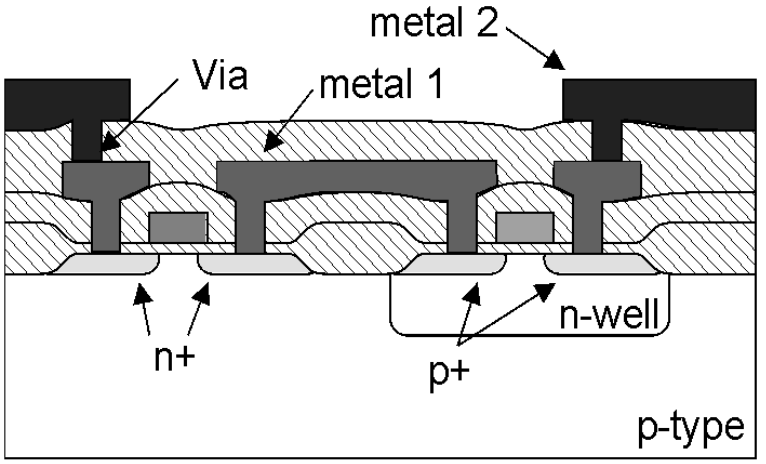
2nd Level Metallization

The entire surface is covered with a field oxide and the contact holes are etched into this oxide to enable connection to the underlying layers.

Then, the second (third, fourth, etc…) layer of metal can be deposited, patterned and etched according to the mask layout.



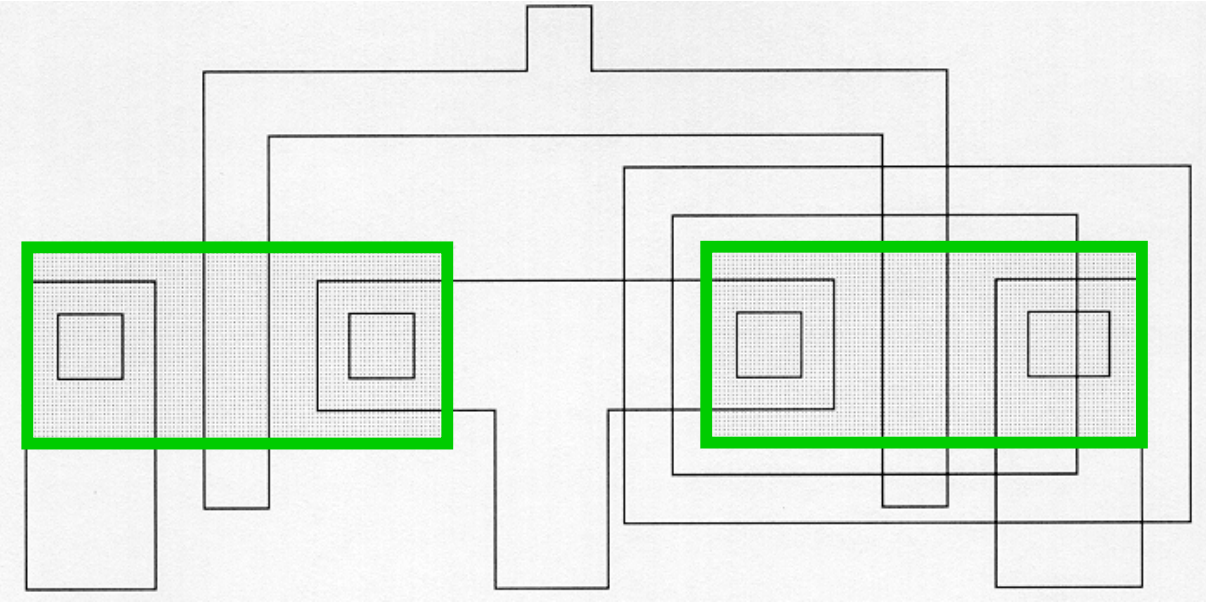
(H)

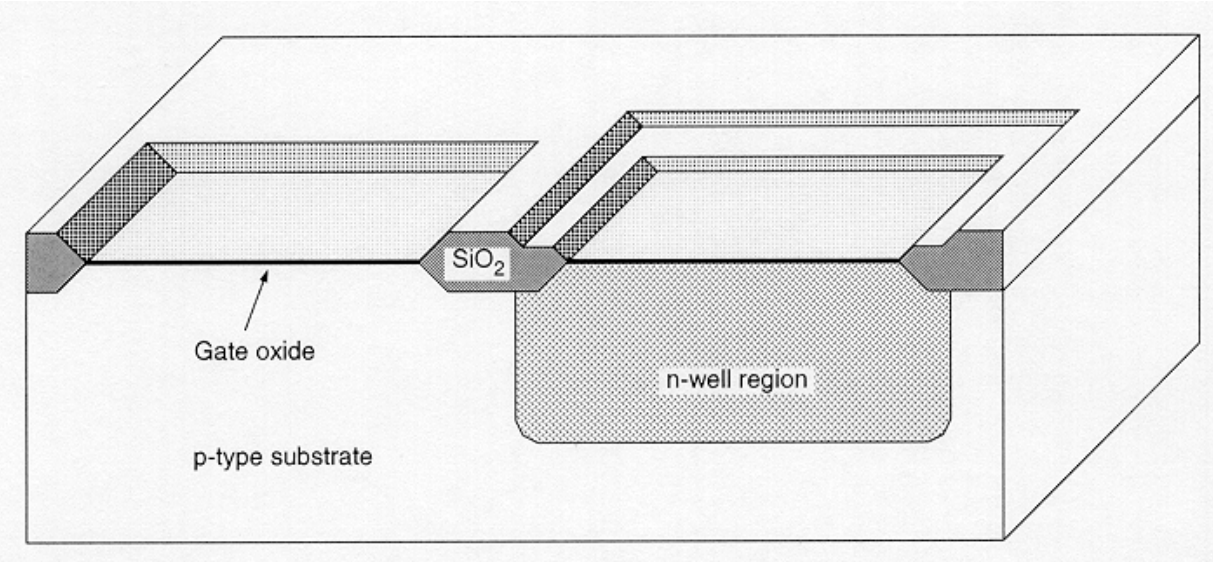


Lithography Masks

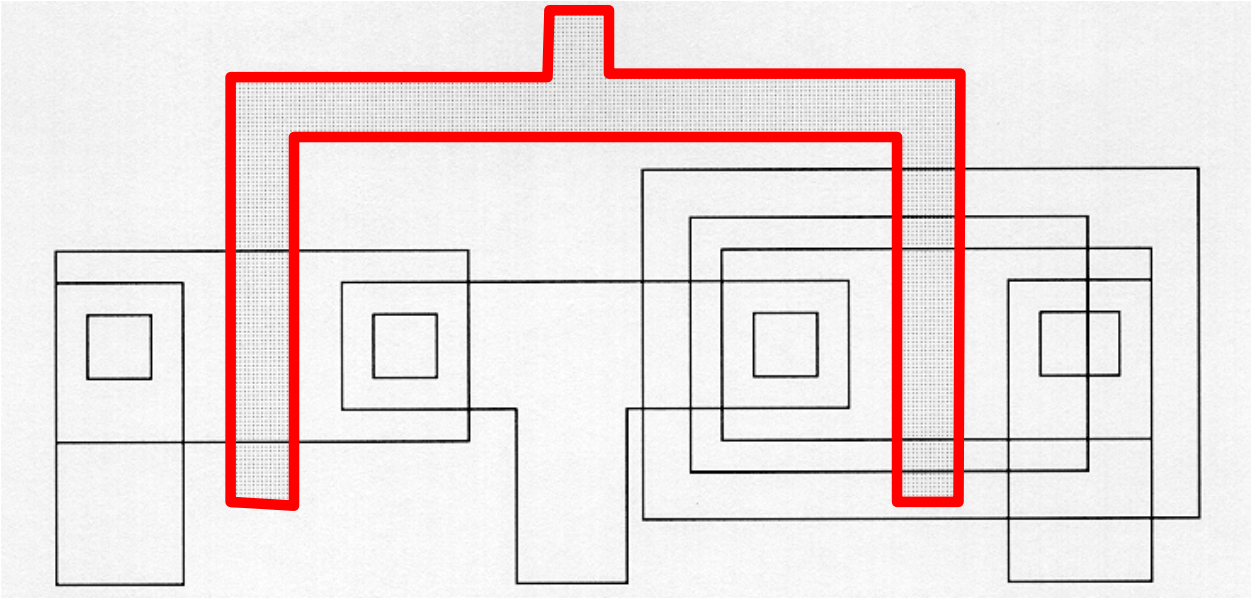
- Each lithography step during fabrication must be defined by a separate lithography mask.
- Each mask layer is drawn (either manually or using a design automation tool) according to the **layout design rules**.
- The combination (superposition) of all necessary mask layers completely defines the circuit to be fabricated.

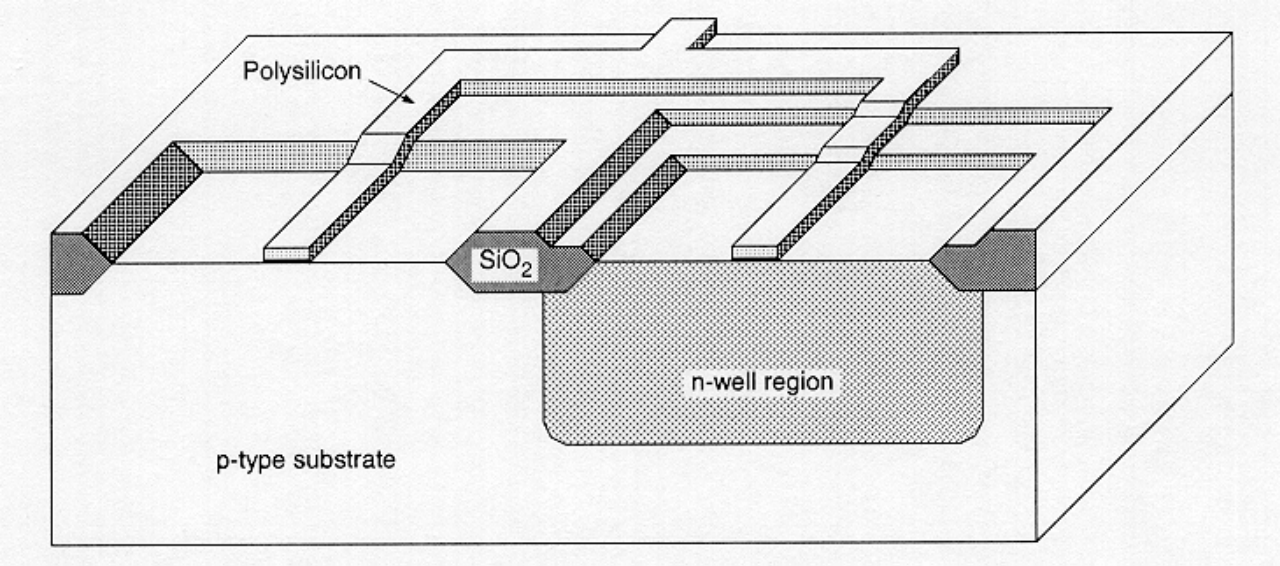
active



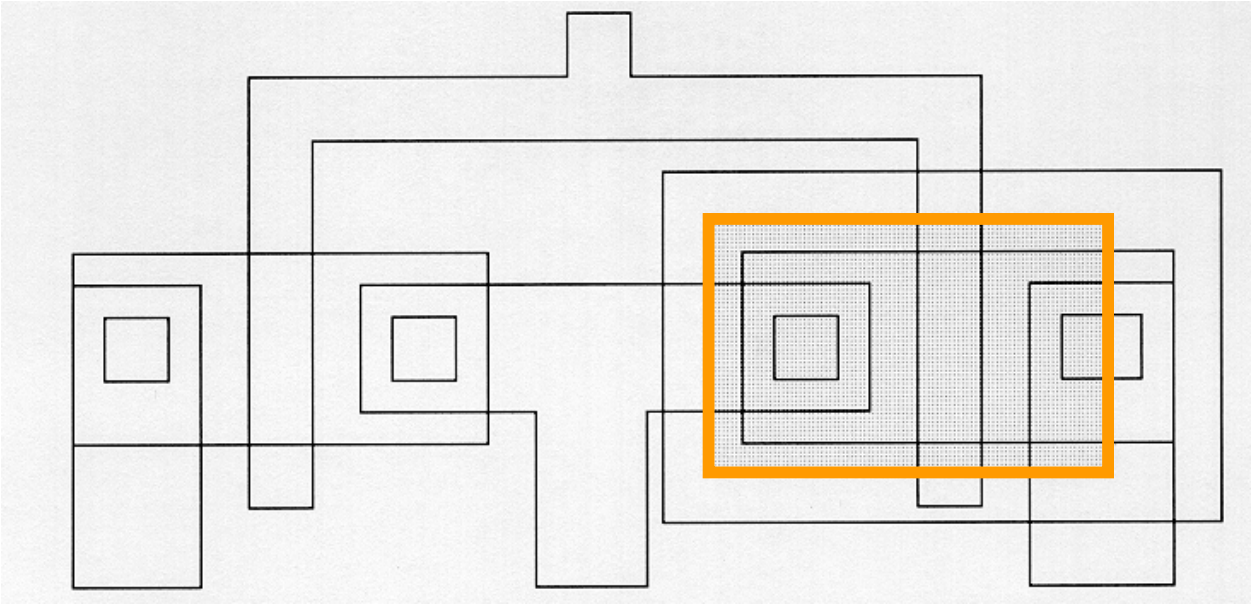


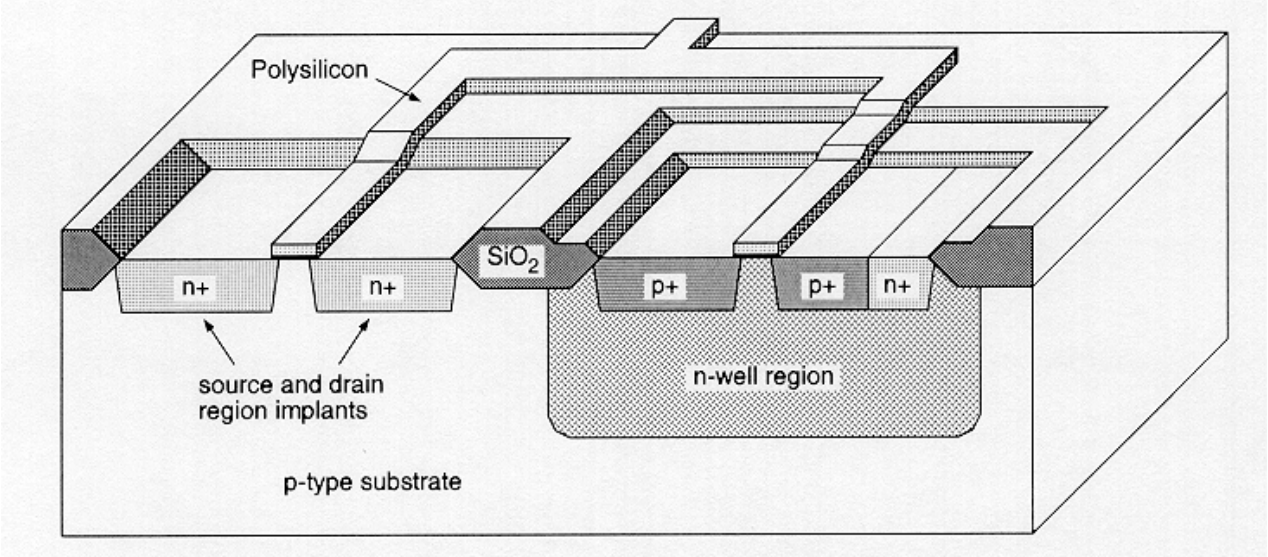
poly



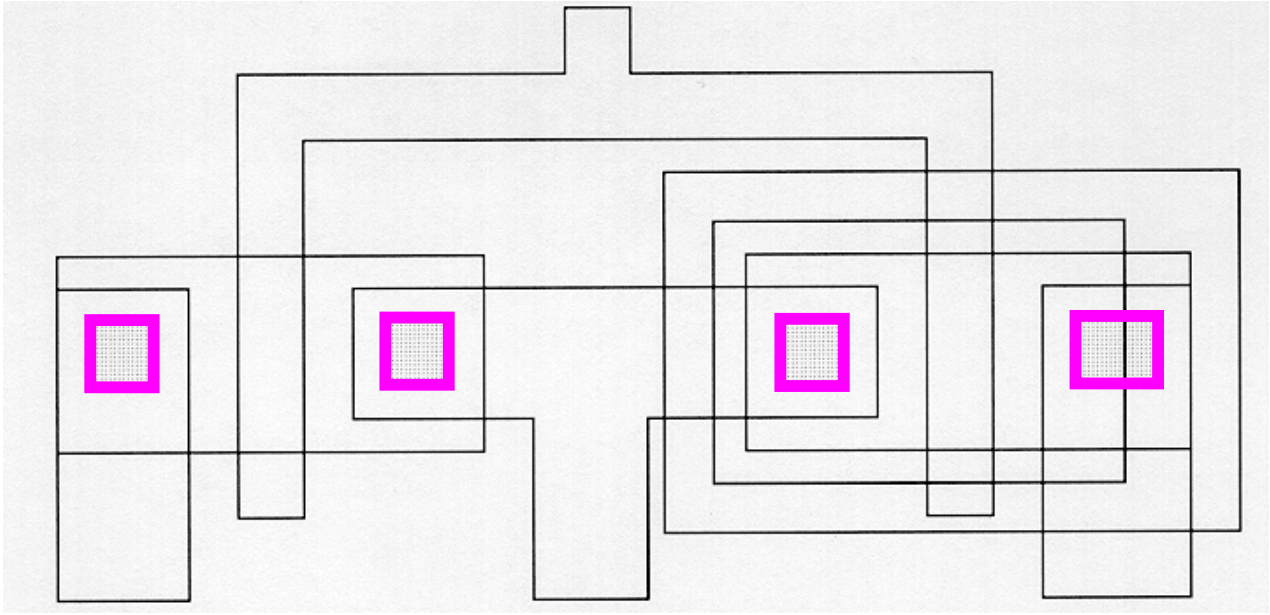


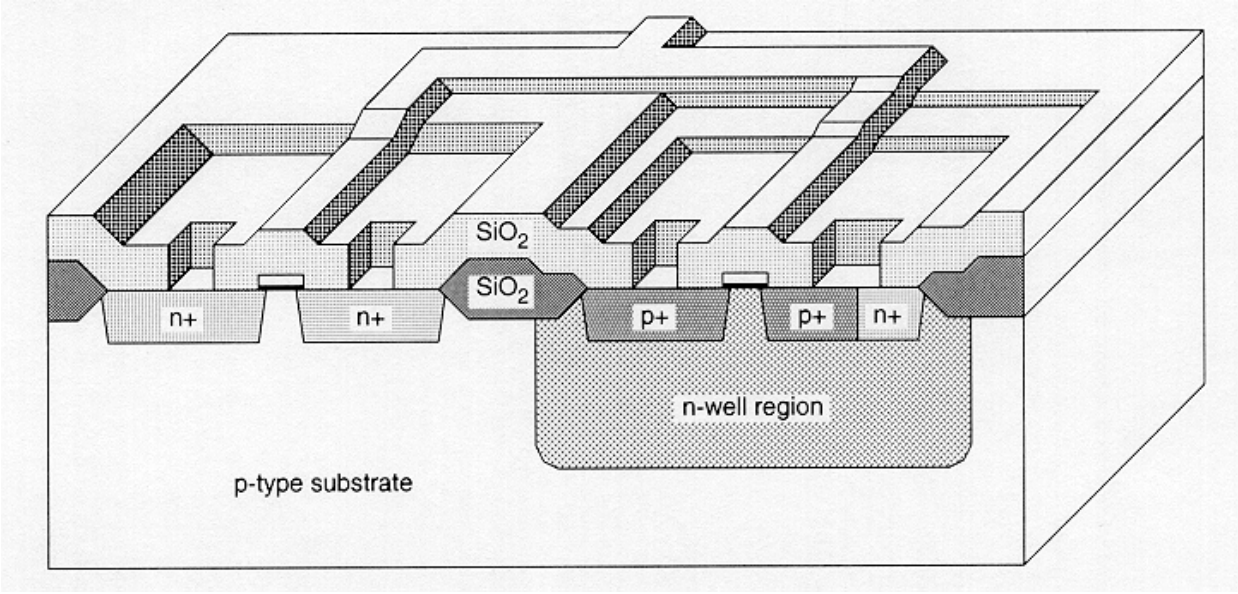
implant



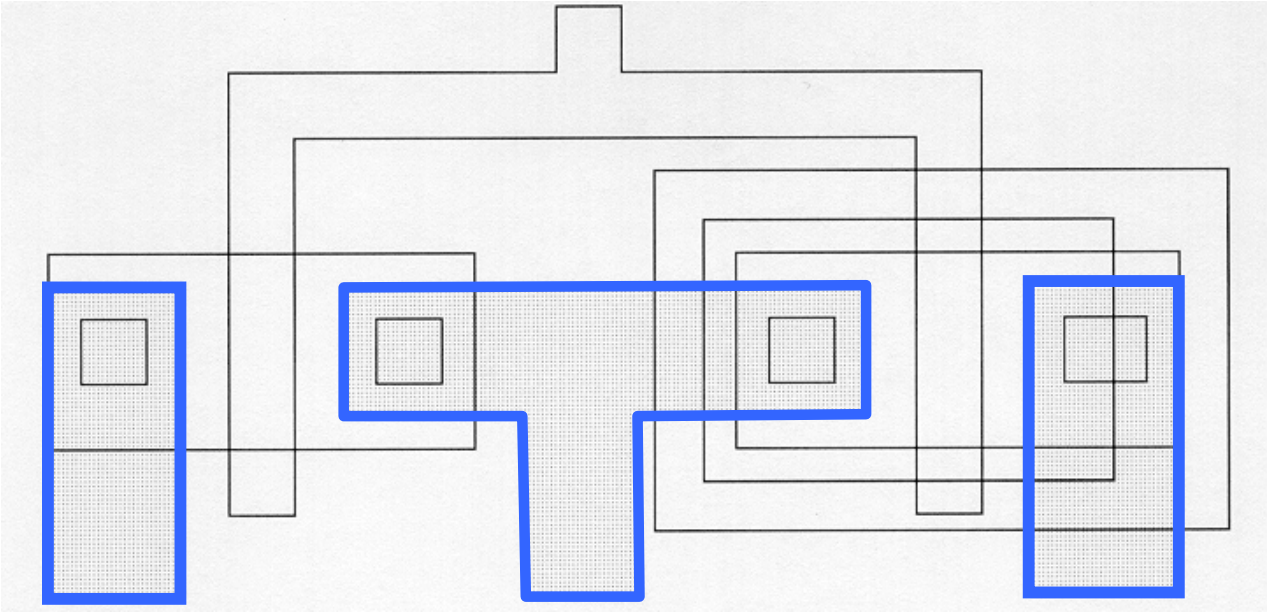

Polysilicon
SiO_2
n+
n+
p+
p+
n+
source and drain
region implants
n-well region
p-type substrate

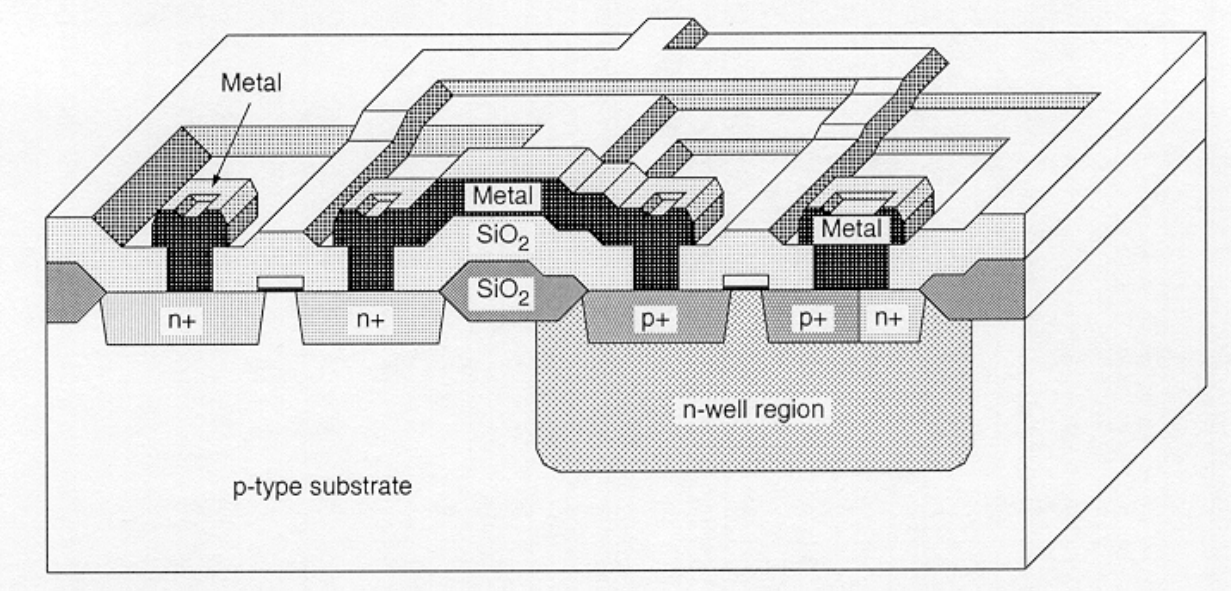
contacts



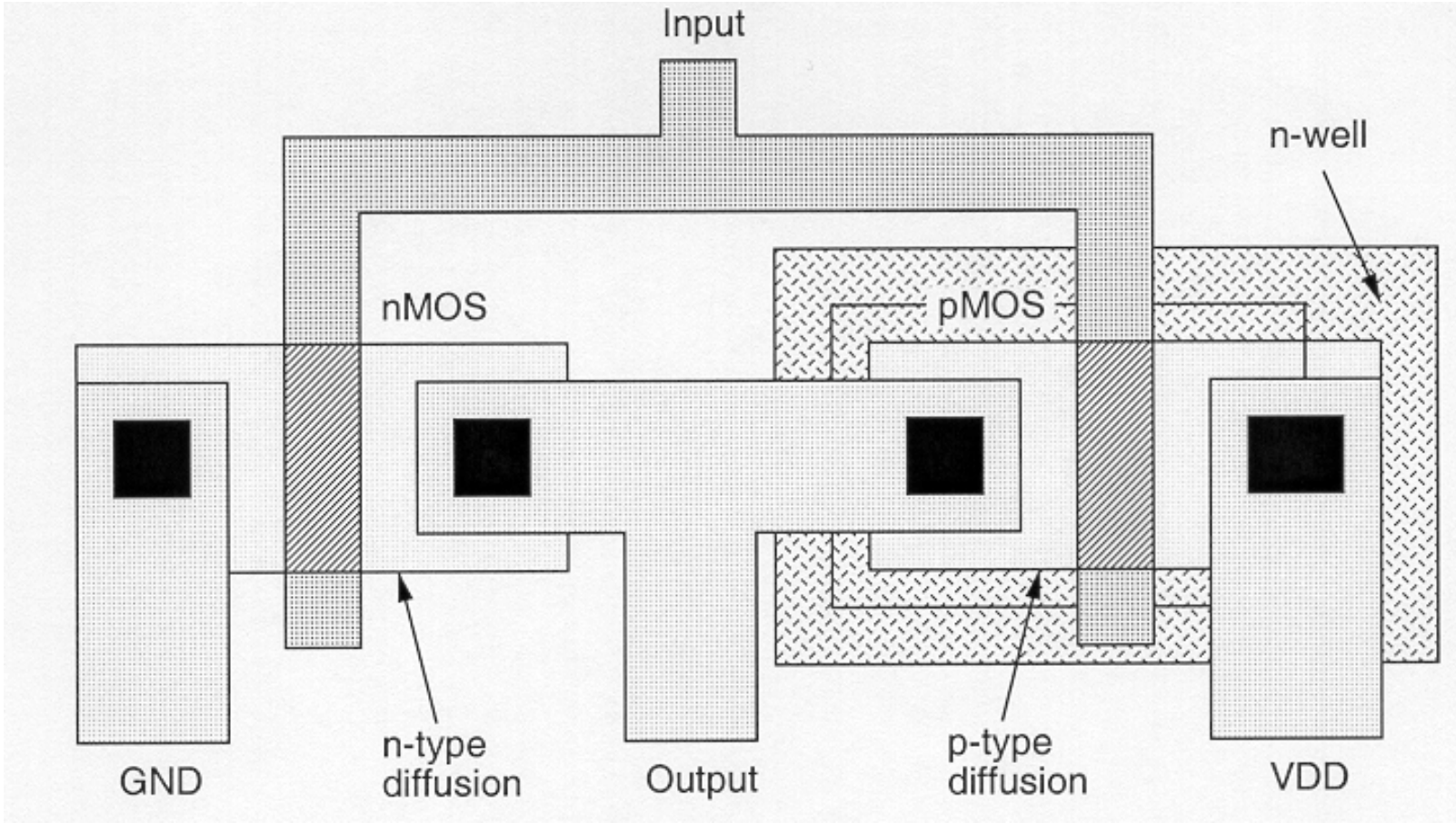


metal





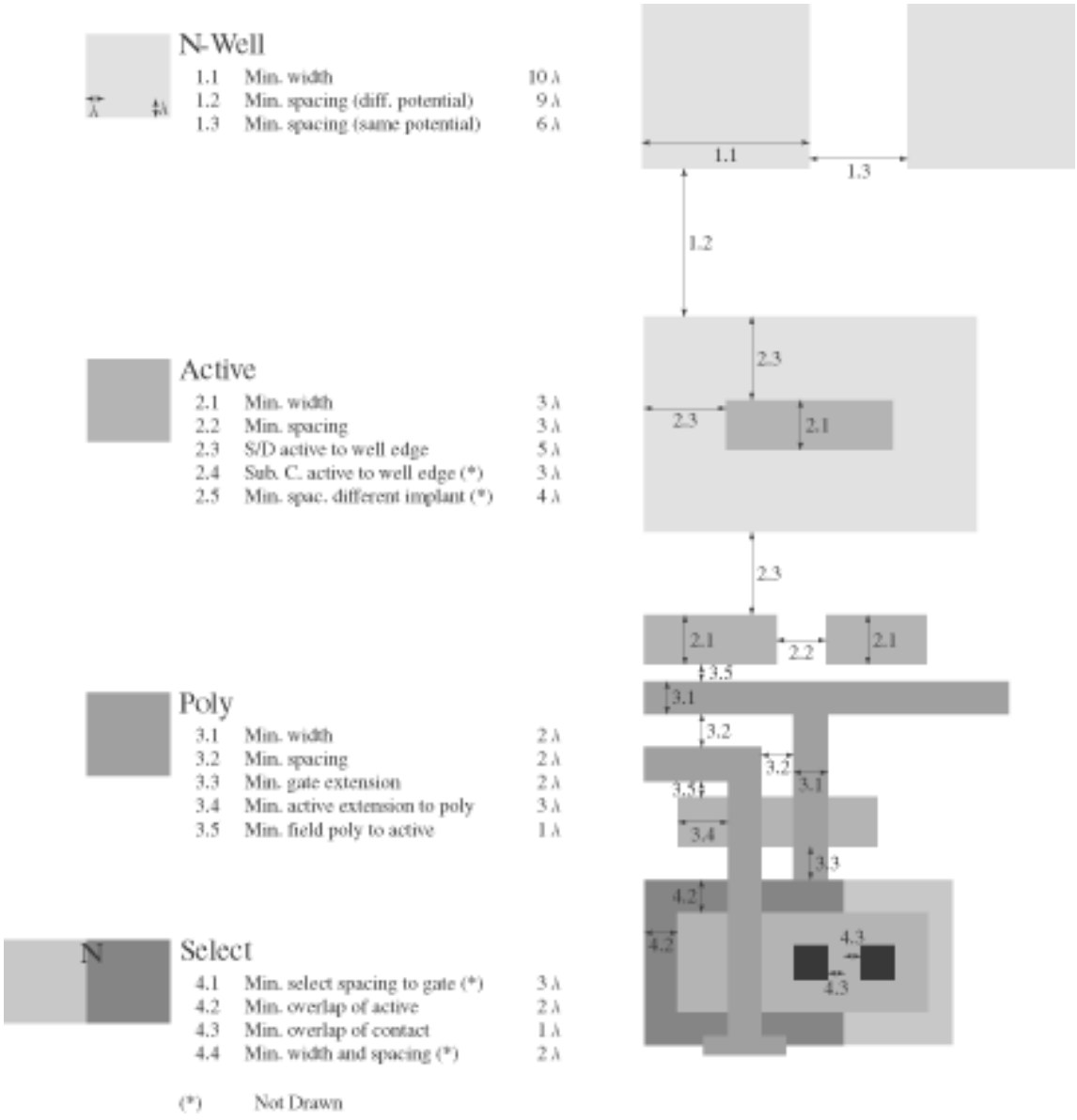
Composite Mask Layout



Layout Design Rules

- To allow reliable fabrication of each structure, the mask layers must conform to a set of geometric layout design rules.
- Usually, the rules (for example: minimum distance and/or separation between layers) are expressed as multiples of a scaling factor – lambda (λ).
- For each different fabrication technology, lambda factor can be different.

Layout Design Rules



N-Well

1.1	Min. width	10 λ
1.2	Min. spacing (diff. potential)	9 λ
1.3	Min. spacing (same potential)	6 λ

Active

2.1	Min. width	3 λ
2.2	Min. spacing	3 λ
2.3	S/D active to well edge	5 λ
2.4	Sub. C. active to well edge (*)	3 λ
2.5	Min. spac. different implant (*)	4 λ

Poly

3.1	Min. width	2 λ
3.2	Min. spacing	2 λ
3.3	Min. gate extension	2 λ
3.4	Min. active extension to poly	3 λ
3.5	Min. field poly to active	1 λ

Select

4.1	Min. select spacing to gate (*)	3 λ
4.2	Min. overlap of active	2 λ
4.3	Min. overlap of contact	1 λ
4.4	Min. width and spacing (*)	2 λ

(*) Not Drawn

Layout Design Rules

Contact

5.1	Exact contact size	2 λ
5.2	Min. poly overlap	1.5 λ
5.3	Min. spacing	2 λ
5.4	Min. spacing to gate	2 λ
6.1	Exact contact size	2 λ
6.2	Min. active overlap	1.5 λ
6.3	Min. spacing	2 λ
6.4	Min. spacing to gate	2 λ

Metal1

7.1	Min. width	3 λ
7.2.a	Min. spacing	3 λ
7.3	Min. overlap of any contact	1 λ

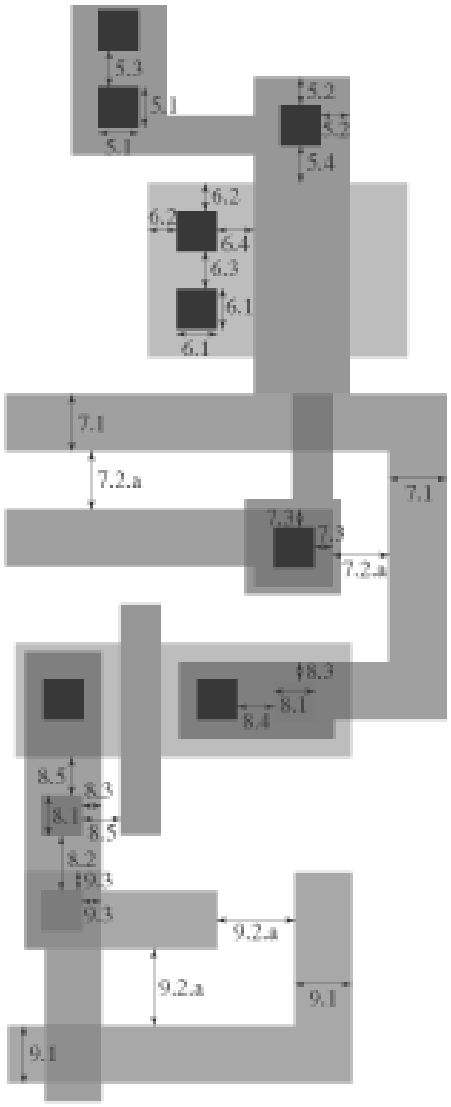
Via1

8.1	Exact size	2 λ
8.2	Min. spacing	3 λ
8.3	Min. overlap by metal1	1 λ
8.4	Min. spacing to contact	2 λ
8.5	Min. spac. to poly or act. edge	2 λ

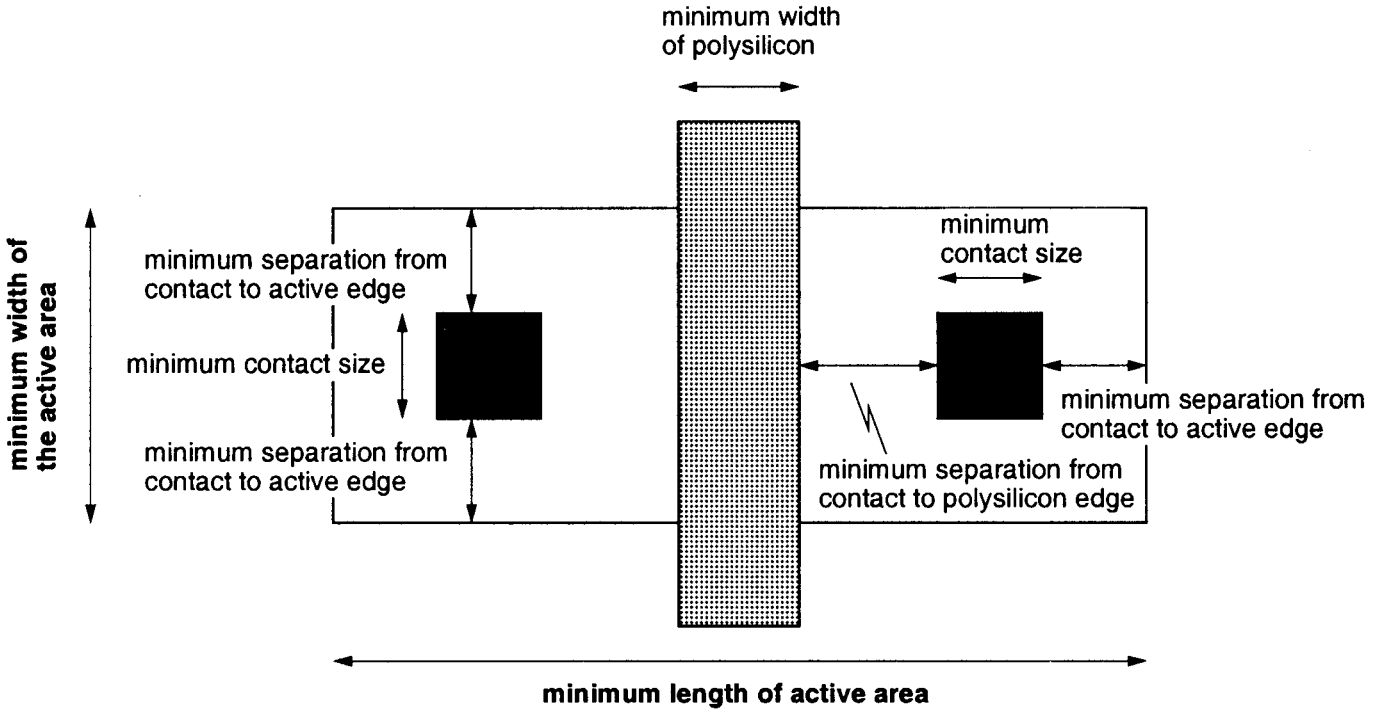
Metal2

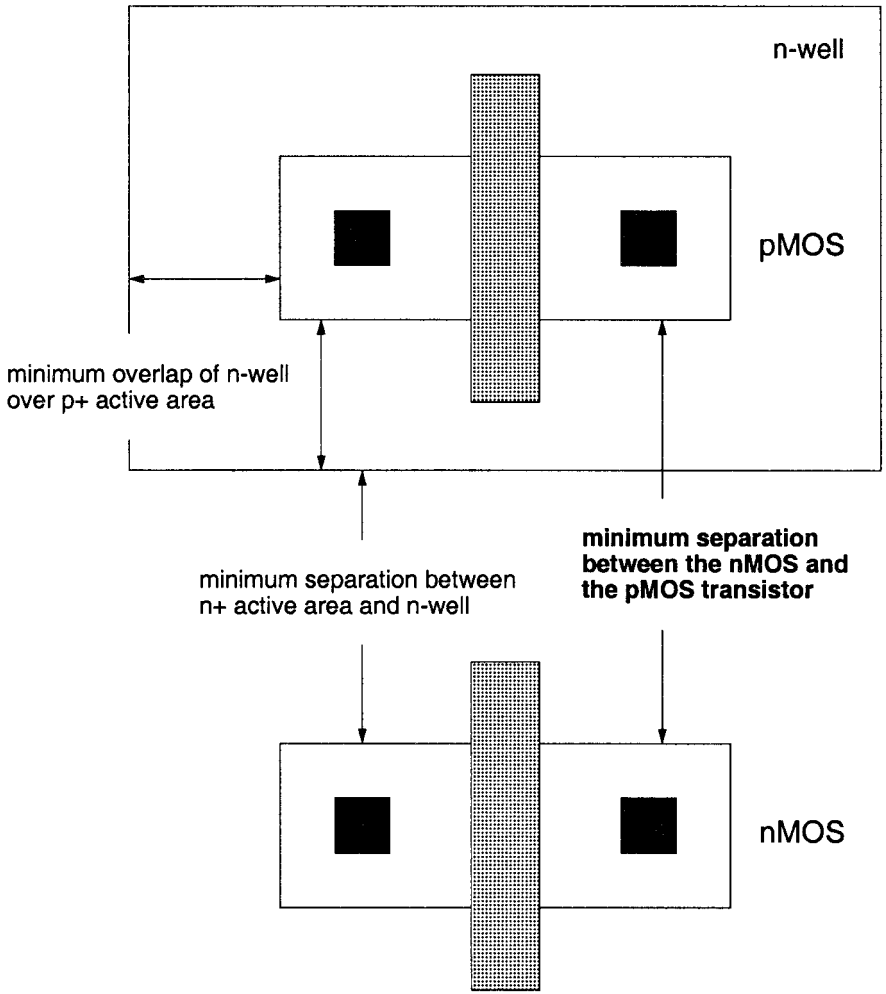
9.1	Min. width	3 λ
9.2.a	Min. spacing	4 λ
9.3	Min. overlap to via1	1 λ

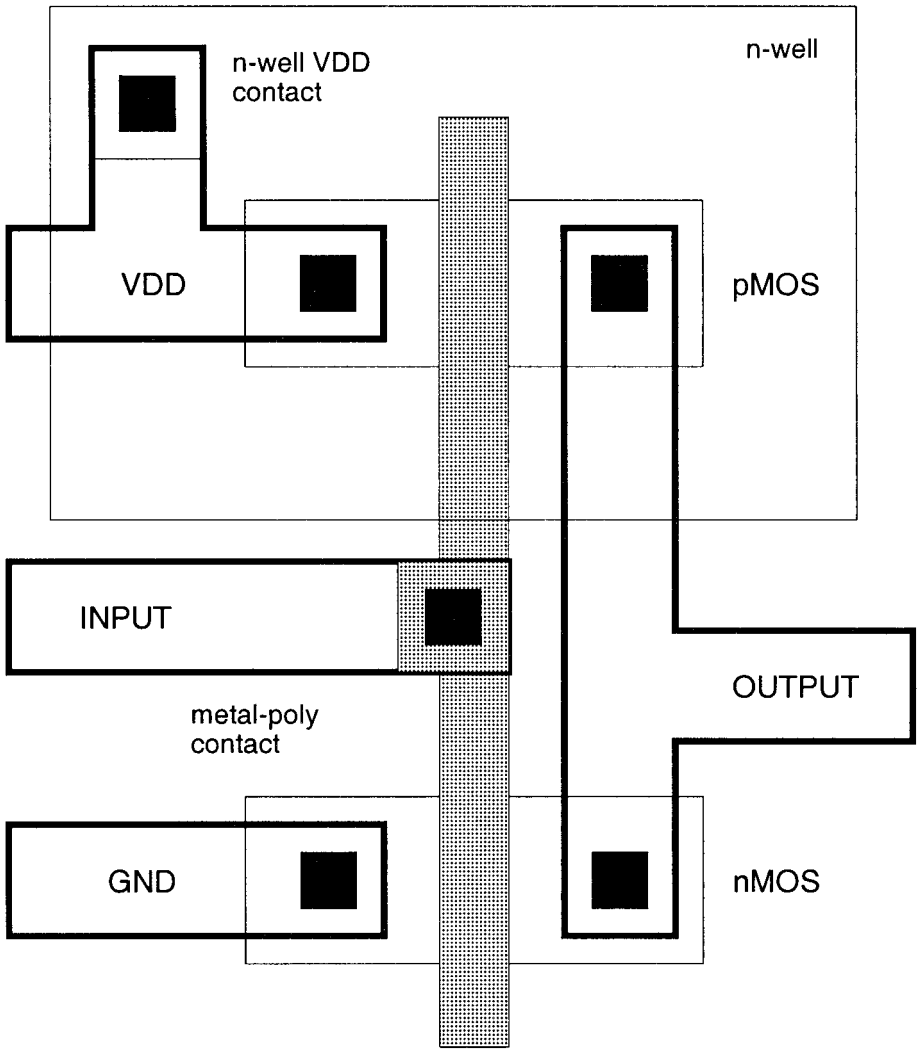
(*) Not Drawn



Layout Rules of a Minimum-Size MOSFET

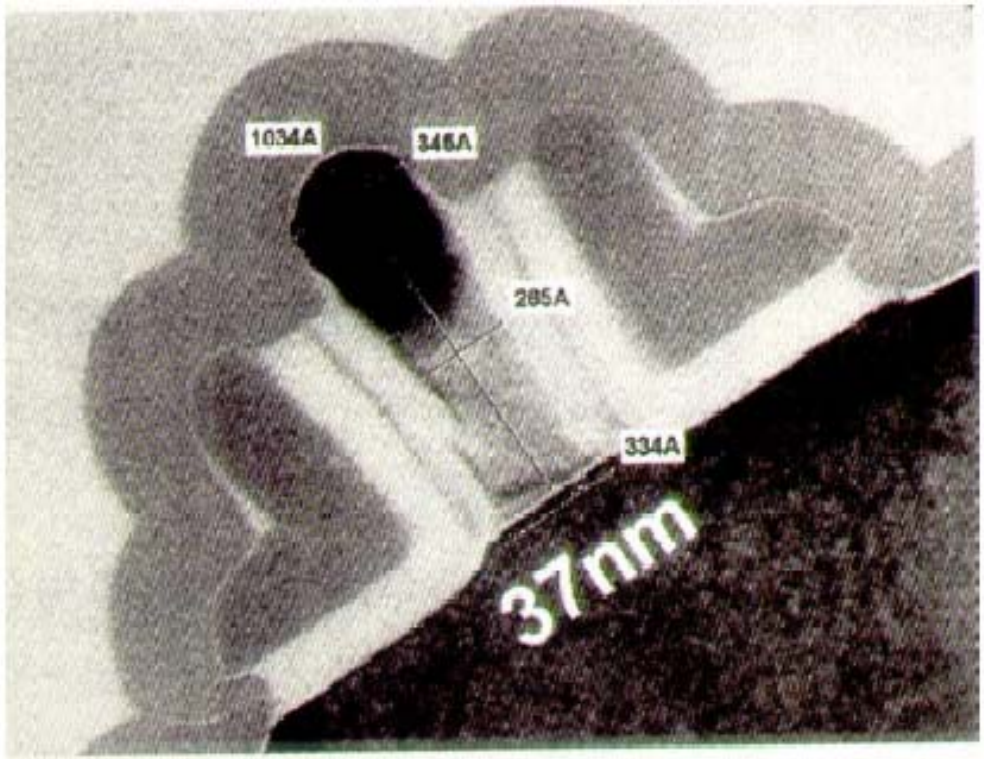



n-well
pMOS
minimum overlap of n-well
over p+ active area
minimum separation between
n+ active area and n-well
minimum separation
between the nMOS and
the pMOS transistor
nMOS


n-well VDD
contact
n-well
VDD
pMOS
INPUT
OUTPUT
metal-poly
contact
GND
nMOS

State-of-the-Art Examples

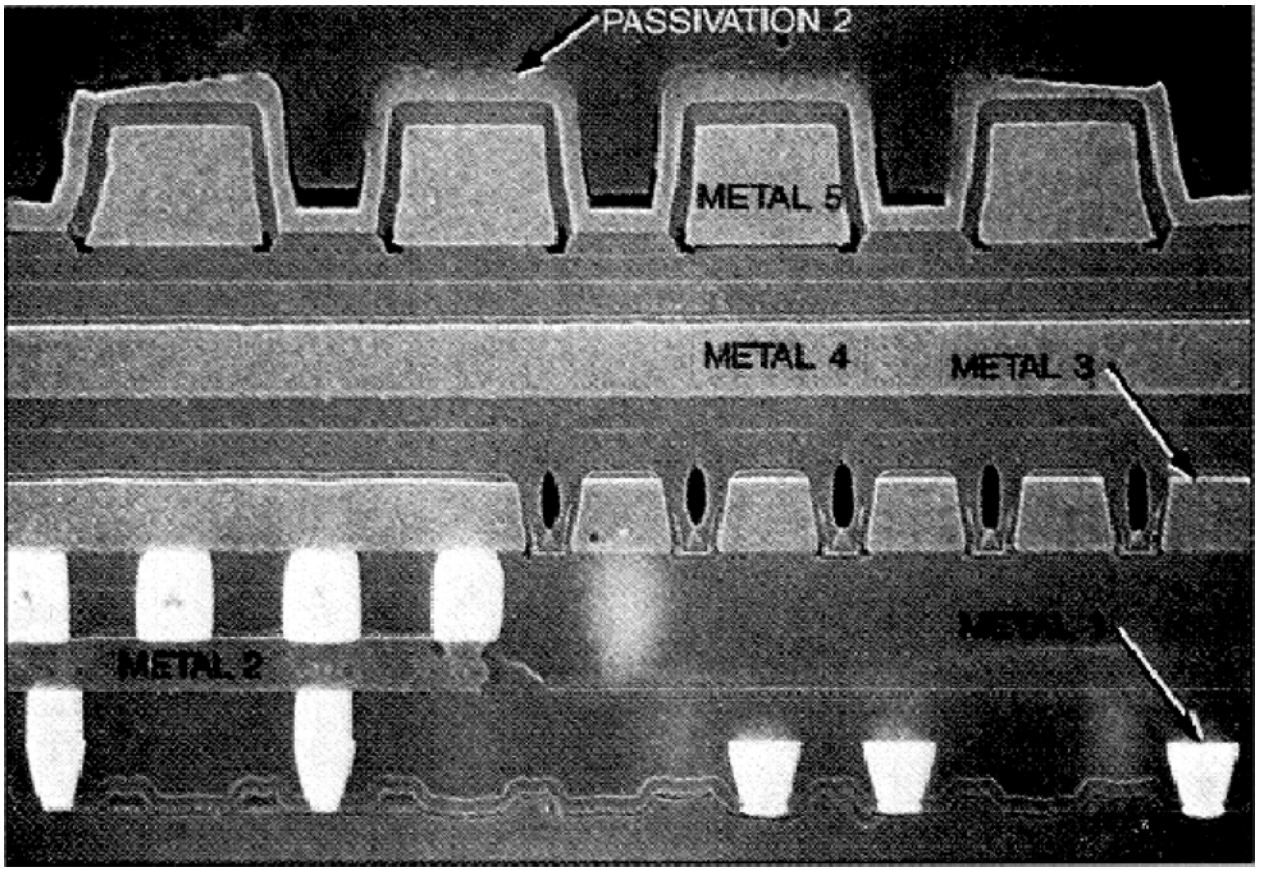
TI
0.09μ



(a) 90nmノード向けトランジスタ

Source: Nikkei Microdevices 9/02

Multi-Level Interconnect with CMP



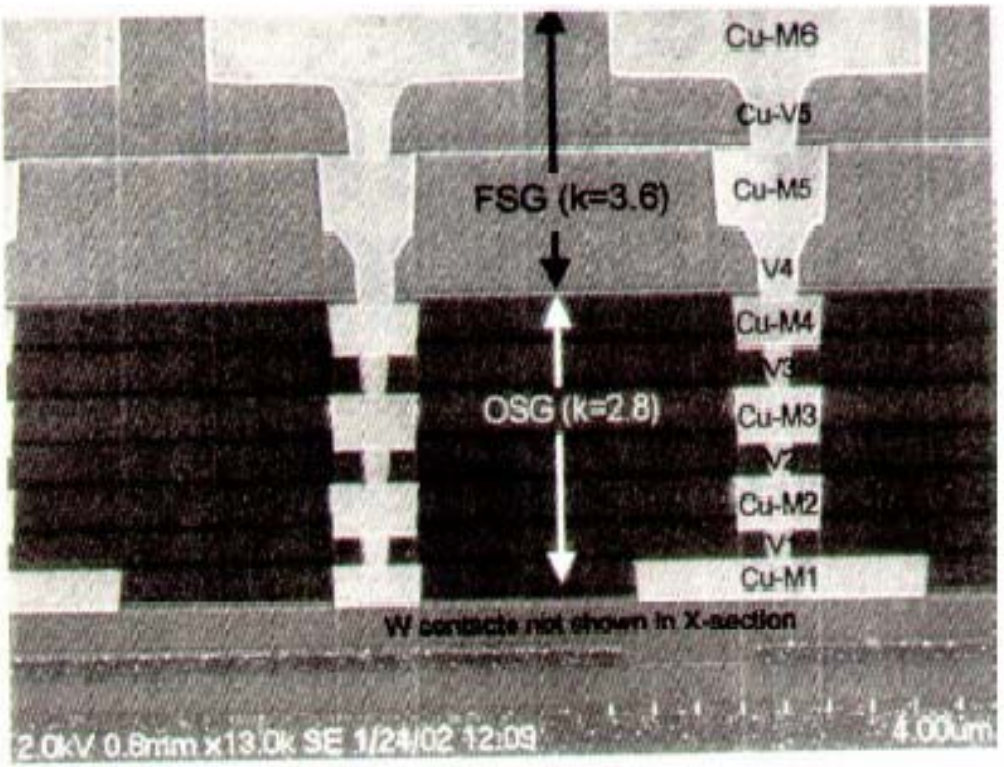
Multi-Level Metal Interconnect

TSMC
0.13μ
8 layers
Cu

Source:
Nikkei
Microdevices
11/00

Multi-Level Metal Interconnect

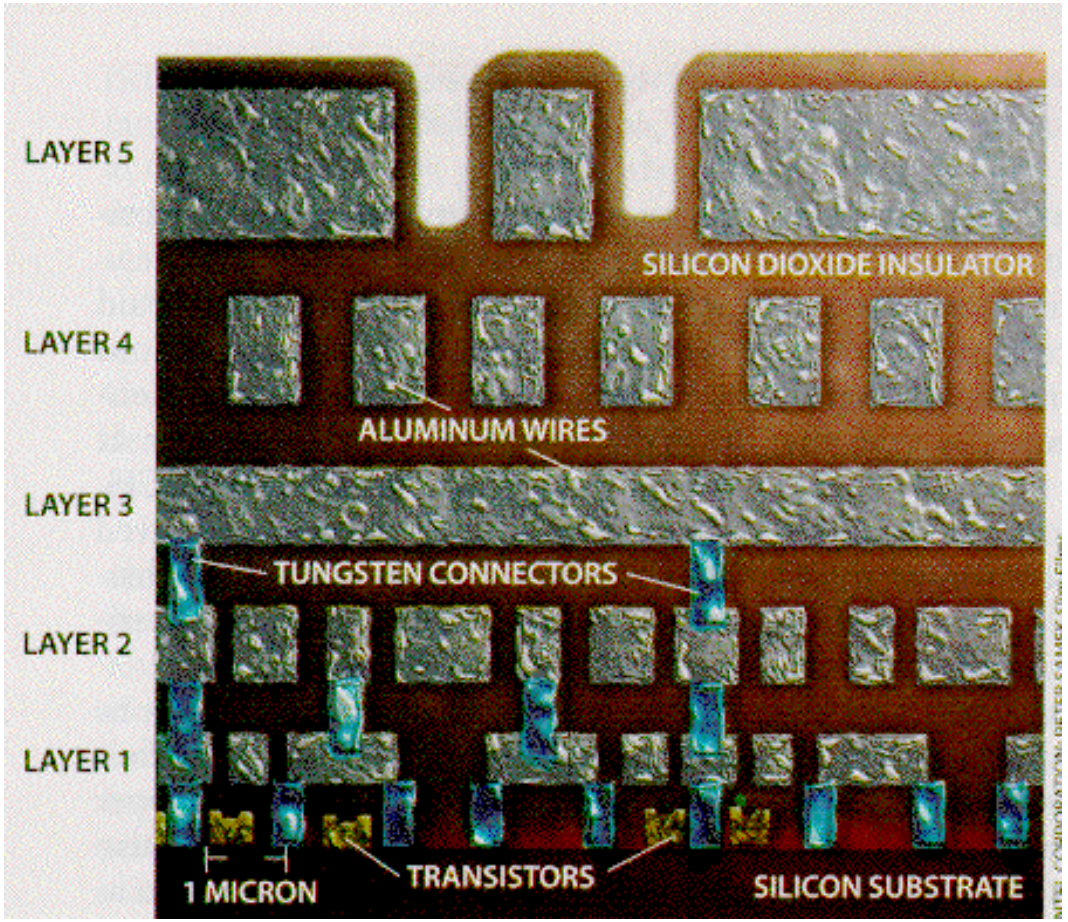
TI
0.09μ
6 layers
Cu



Source: Nikkei Microdevices 9/02

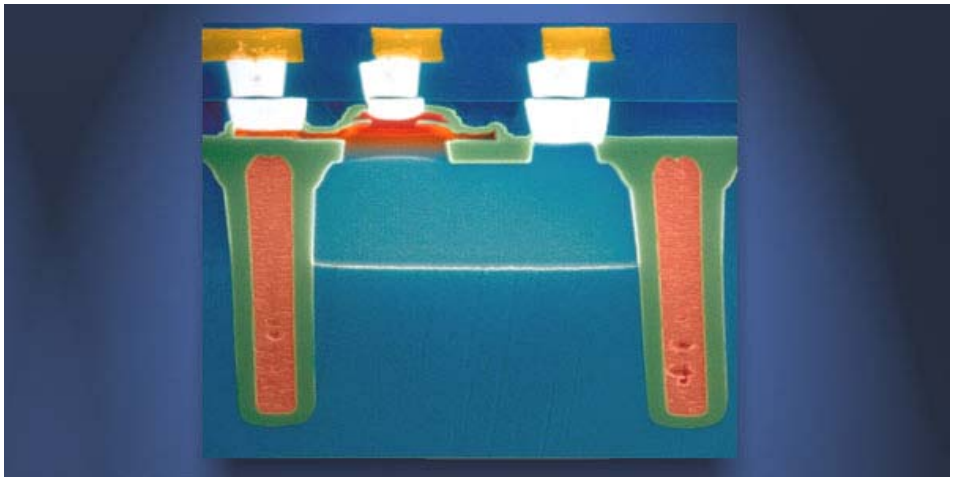
(b) 90nmノード向け多層配線

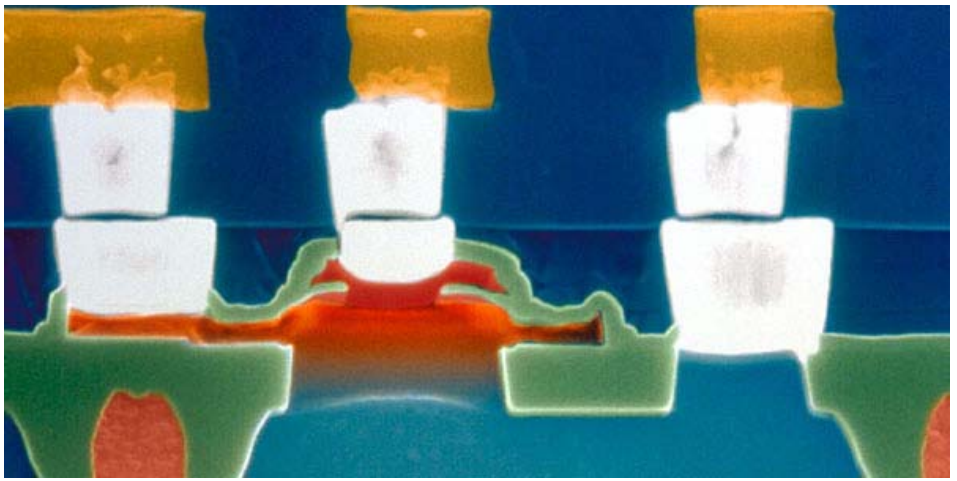
Multi-Level Metal Interconnect



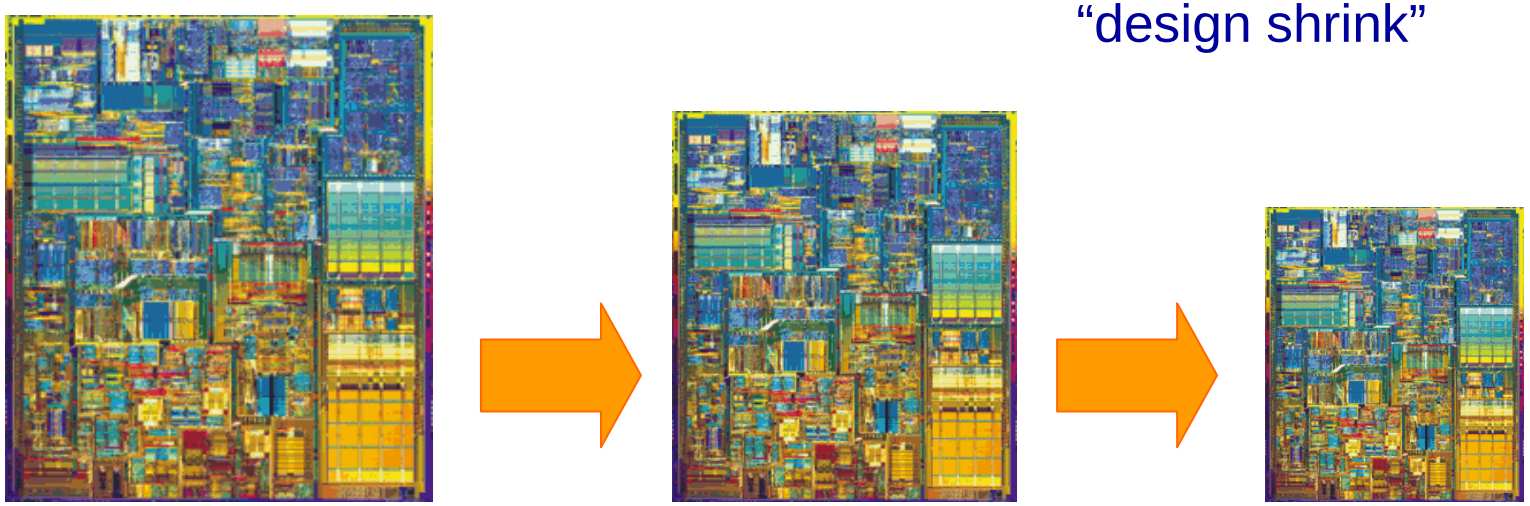
Silicon on Insulator (SOI)

The key innovation in SOI is to build the transistor structures on an **insulating** material rather than a common substrate as in CMOS. This reduces parasitic capacitances and eliminates substrate noise coupling.



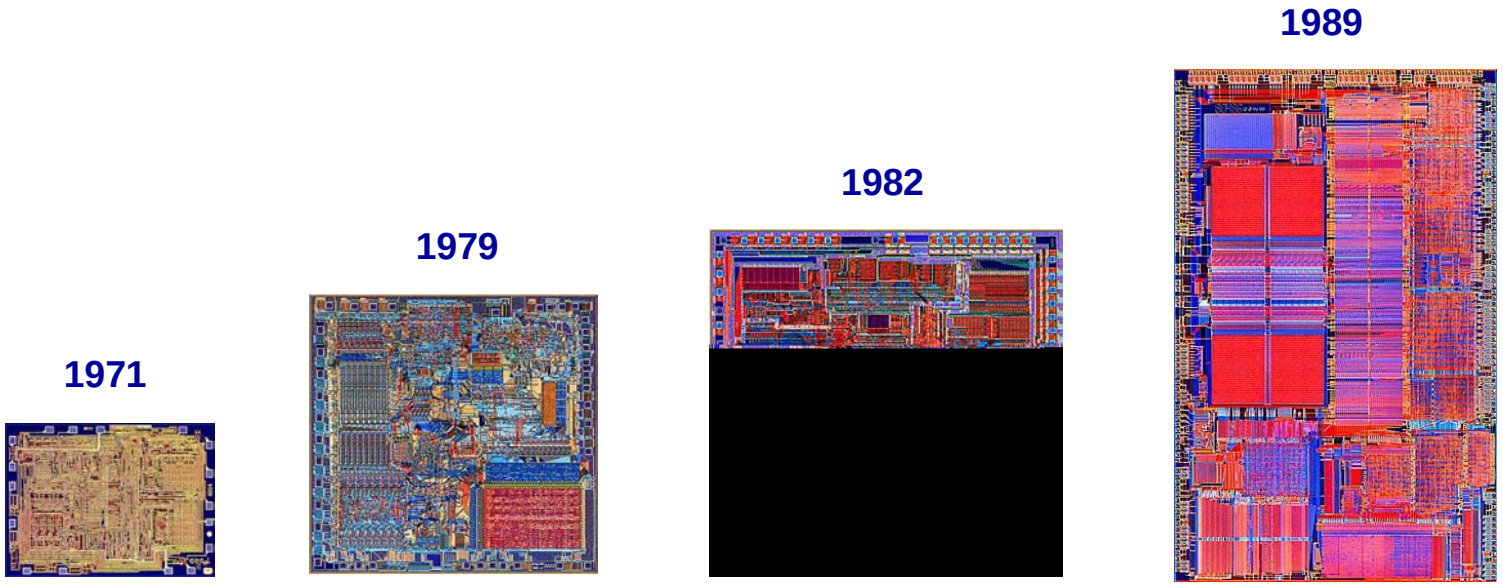


Lithography Resolution is Decreasing



With each new technology generation, we would be able to fit the same amount of functionality into a **smaller** silicon area (ideally).

Lithography Resolution is Decreasing



10 μm technology
12 sqmm

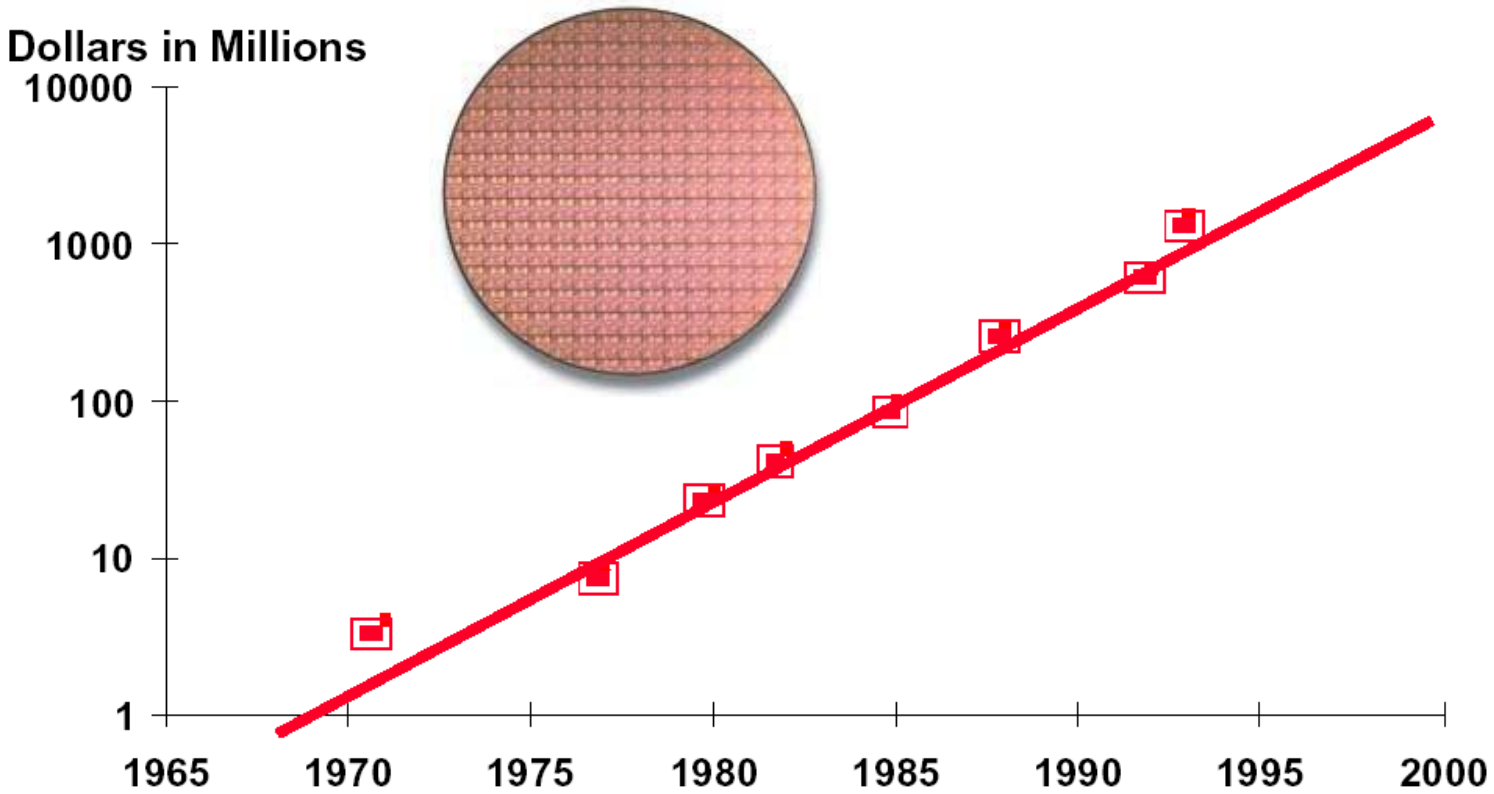
3 μm technology
33 sqmm

1.5 μm technology
50 sqmm

0.8 μm technology
81 sqmm

But at the same time, we try to put **more** functionality in each chip for each new technology generation, so that the average chip size actually **increases** over the years !

Final Remark: Fabrication Cost



Initial investment costs of a new fabrication facility