B. Tech.

THIRD SEMESTER EXAMINATION, 2010-11

Analog and Digital Electronics (EEC-309)

Time : 3 Hours Total Marks : 100

Note : Attempt **all** questions. All questions carry equal marks.

Q.1. Attempt any four parts of the following: **(5 × 4 = 20)**

(a) Explain the operation of a LED with the help of necessary diagrams. List the materials used for constructing LED. Give the advantages and disadvantages of LED.

Ans. Principle of LED Operation :

1. When the LED is forward biased, the electrons in the n-region will cross the junction as recombine with the holes in the p-type material.

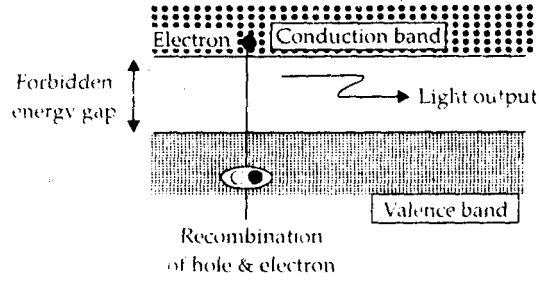


Fig. (a) : Principle of operation of LED

2. These free electrons reside in the conduction band and hence at a higher energy level than the holes in the valence band.
3. When the recombination takes place, these electrons return back to the valence band which is at a lower energy level than the conduction band.
4. While returning back, the recombning electrons give away the excess energy in the form of light. This is shown in Fig. (a). This process is called as **electroluminescence.** In this way an LED emits light. This is the principle of operation of LED.
5. The colours associated with different materials are as follows.

	Material-used	Colour of the emitted light
1.	Gallium Arsenide (Ga As)	Infrared (IR)
2.	Ga As P	Red or Yellow
3	Gallium phosphide (Ga P)	Red or Green

Advantages of LEDs :

1. LEDs are of small size and light weight. Therefore it is possible to pack a large number of LED, in a small space while manufacturing a display.
2. They are available in different spectral colours.
3. They have longer life as compared to the lamps.
4. The light emitted by a LED is proportional to the amount of current flowing through it. Hence we can control the current flowing through LEDs to vary their brightness as per the requirements of the application.
5. They are suitable at nigh operating speeds as they take less than 1 μs to turn on or off.
6. LEDs can be easily interfaced with the other electronic circuits.

Disadvantages of LEDs :

1. Output power is affected by changes in temperature.
2. Overcurrent can damage it easily.

3. They need larger power for their operation
4. Luminous efficiency of LEDs is low.

(b) Explain the forward and reverse characteristics of a Tunnel diode and explain the tunneling operation.

Ans. Tunnel Diode Characteristics :

1. The volatmpere characteristics of a tunnel diode is shown in Fig. and its symbols are shown in fig.

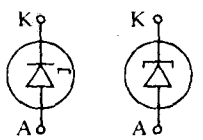


Fig. (a) : Circuit symbols of tunnel diode

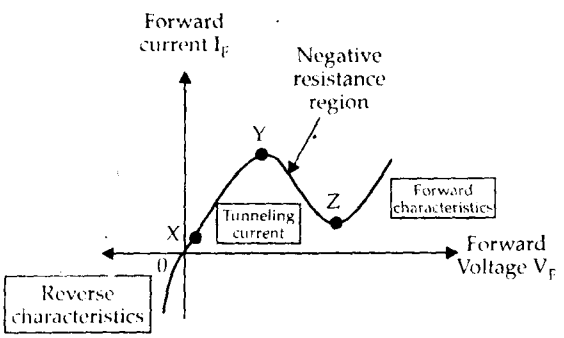


Fig. (b) : Volt-amperecharacteristics of a tunnel diode

Reverse Characteristics :

1. Due to heavy doping of p and n sides, the depletion region is extremely narrow when the tunnel diode is reverse biased.
2. Therefore the reverse blocking capacity of the junction is lost and reverse current will start flowing as soon as a very small reverse voltage is applied.
3. Thus the tunnel diode allows the conduction to take place for all reverse voltages. There is no breakdown effect as observed in the conventional rectifier diode.
4. Therefore we can not use the tunnel diode as a rectifier.

Forward Characteristics:

1. Forward characteristics can be diveded into three regions namely X to Y, Y to Z and Z onwards.
2. **Region X to Y :** In this region the forward voltage V_F is extremely small. But heavy conduction will take place in this region because electrons "tunnel" through the pn junction. The "tunnelling" takes place as a result of heavy doping.
3. **Region Y to Z :** In this region, at point Y the forward voltage begins to develop a barrier and the forward current starts decreasing inspite of continued increase in V_F. This region is called as the **negative resistance region.**
4. The diode resistance in the region Y to Z is mathematically expresses as

$$R_f = \frac{\Delta V_F}{\Delta I_F} \qquad ...(1)$$

ΔV_F is positive but ΔI_F is negative. Hence R_f is called as a negative resistance. The decrease in I_f with increase in V_F is opposite to the Ohm's law.

The negative resistance characteristics is utilized in the applications of tunnel diode such as oscillator and microwave amplifier.

5. **Region Z onwards :** At point Z, the current starts increasing with increase in voltage. So this is a positive resistance region and the tunnel diode acts as the conventional diode.

Construction of Tunnel Diode :

1. The material used for the construction of a tunnel diode is Germanium of Gallium Arsenide.
2. Fig. (c) shows the basic construction of a tunnel diode.

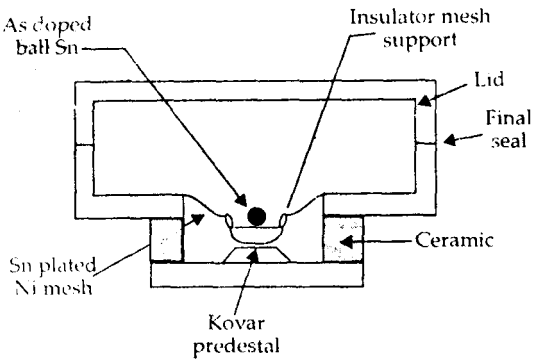
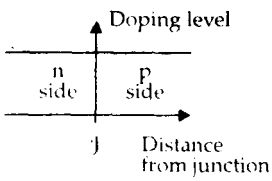


Fig.(c) : Construction of a tunnel diode

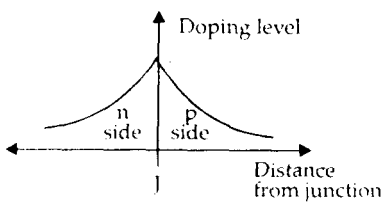
(c) Explain the characteristics of a varactor diode and mention how it can be used in a resonant circuit. Also list some of the applications of the varactor diode.

Ans. Varactor Characteristics :

1. The varactor diodes are used in many applications in place of the mechanically tuned capacitors.
2. In addition to this, a capacitance ratio C_R also is mentioned. It is nothing but the range of C_T corresponding to a reverse voltage range.
3. For example a varactor diode MV209 has $C_T = 29$ pF at -3 V and a capacitance ratio of 5 : 1 over the range to -3 V or -25 V.



(a) Doping profile of an abrupt junction



(b) Doping profile of a hyper abrupt junction

Fig.

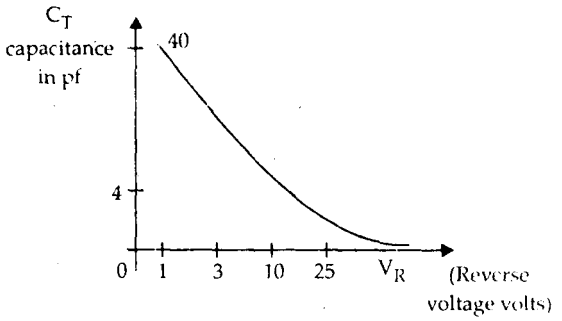


Fig. (c) : Varactor characteristics

4. The tuning range C_R of the varactor is actually dependent on the doping levels.
5. For an ordinary diode, the junction is abrupt type and the doping profile is uniform as shown in Fig (a). This diode gives a tuning range of 3 : 1 to 4 : 1.
6. The varactors have a large tuning range due to the **hyper abrupt** junction whose doping profile is as shown in fig. (b)
7. This shows that the doping levle increases as we approach the junction.
8. Heavy doping produces narrow depletion region and increases capictance.
9. The typical characteristics of a varactor is shown in fig. (c)

Application to a Varicap in Tuning a Resonant Circuit :

1. A varicap can be used to vary the resonant frequency of an LC oscillator circuit. For this, the varicap is connected across the LC resonant circuit as shown in fig. (d)
2. The resonant frequency of the tuned circuit without varactor diode is given by :

$$f_r = \frac{1}{2\pi\sqrt{LC}} \qquad ...(1)$$

3. When the varactor is connected in parallel with LC components as shown in fig. (d), the resonant frequency gets modified to

$$f_r = \frac{1}{2\pi\sqrt{L(C + C_T)}} \qquad ...(2)$$

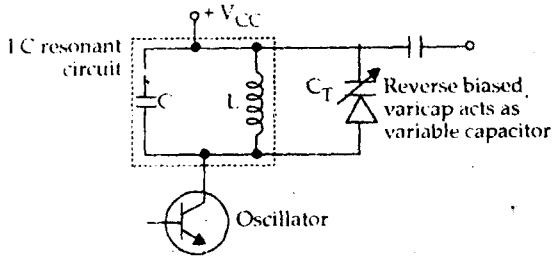


Fig. (d) : How to use the vactor diode in an LC circuit

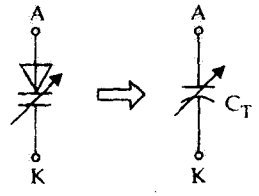


Fig. (e) : Simplified equivalent circuit of resonant the varactor diode

where C_T is the variable capacitance offered by the varactor diode.

4. With change in reverse voltage across the varactor C_T will change, this will change the resonant frequency. This is done in the FM modulator circuit.

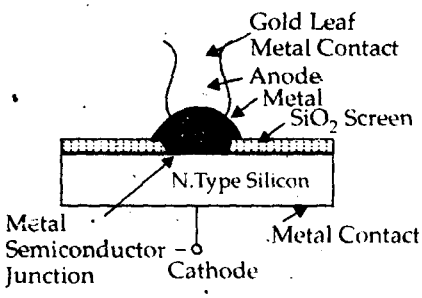
Other Applications of Varactor Diode :

1. FM modulator. 2. Automatic Frequency Control (AFC) in radio receiver

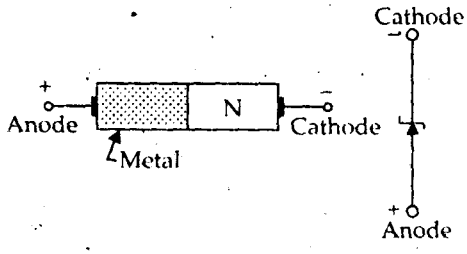
3. Automatic tuning circuits 4. in TV receivers 5. Automobile radios.

(d) Explain the construction, operation and I-V characteristics of a Schottky diode. Also give its equivalent circuit diagram and circuit symbol.

Ans. Schottkydiode : At lower frequencies, an ordinary diode can easily turn off when the bias changes from forward to reverse. But with the increase in frequency the diode reaches a point where it cannot turn off fast enough to prevent noticeable current during part of the reverse half cycle. The effect is called the charge storage. It



(a) Passivated Hot Carrier Diode



(b) Schematic Symbols of Schottky Diode

Fig.

restricts the useful frequency of ordinary rectifier diode. How does it happen, it is explained below :

When a diode is forward biased, some of the carriers in the depletion region have not yet recombined. If the diode is suddenly reverse-biased, the carriers can flow in the reverse for a while. The greater the lifetime, the longer these charges can contribute to reverse current.

The reverse recovery time is so short in small signal diodes that its effect cannot be noticed at frequencies below 10 MHz or so. It becomes very important well above 10 MHz.

The solution is a special-purpose device called a *Schottky diode*. Such a diode has no depletion layer eliminating the stored charges at the junction. Because of lack of charge storage the Schottky diode can switch off faster than an ordinary diode. In fact, a Schottky diode can easily rectify frequencies exceeding 300 MHz.

Its construction is very different from the normal P-N junction in that a metal semiconductor junction is developed, as illustrated is Fig. (a). On one side of the junction a

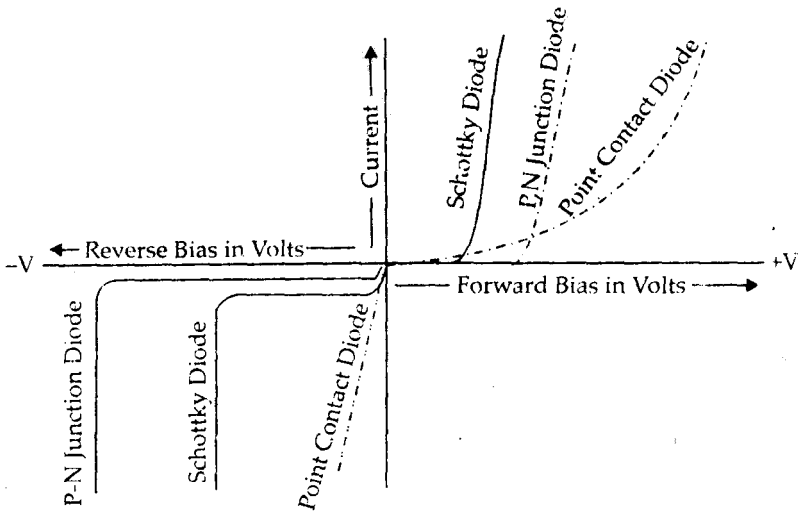


Fig. Comparison of V-I Characteristics of Schottky, Point Contact and P-N Junction diodes

metal (such as gold, silver, platinum, molybdenum, chrome or tungsten) is used and on the other side of the junction N-type doped silicon (but gallium is often used, especially at high frequencies) is used. Different construction techniques result in a differen. set of characteristics for the device, such as increased frequency range lower forward bias, and soon. In general, Schottky diode construction results in a more uniform junction region and increased ruggedness compared to a point-contact diode-its main rival.

(e) With the help of a neatly labeled circuit diagram explain the switching operation of a transistor. Also give the switching waveforms.

Ans. Transistor in cutoff region (Transistor as an open switch)

1. In the cutoff region both the junctions of a transistor are reverse biased and a very small reverse current flows through the transistor.

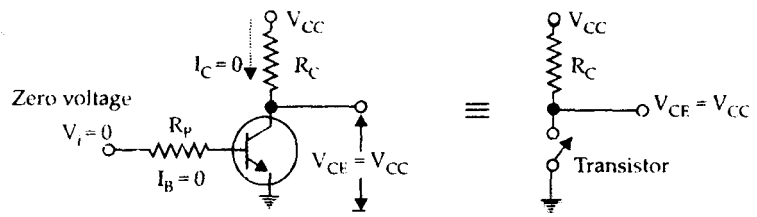


Fig.(a) : Transistor in cutoff is equivalent to an open switch

2. The voltage drop across the transistor (V_{CE}) is high. Thus in the cutoff region the transistor is equivalent to an open switch.
3. The input voltage is zero so $I_B = 0$ and $I_C = 0$
4. Applying KVL to the collector circuit of Fig (a) we get.

$$V_{CC} = I_C R_C + V_{CE}$$

But $I_C = 0$ $\quad \therefore \quad V_{CE} = V_{CC}$

5. The voltage across the transistor is $V_{CE} = V_{CC}$ *i.e.*, high and the current flowing through it $I_C = 0$. This shows that the resistance offered by the transistor is infinite and the transistor operates as an open switch.
6. Thus in the cut off region, the transistor acts as an open switch as shown in fig.(a)

Transistor in the saturation region (Transistor as closed switch) :

1. Fig. (b) shows the biasing of transistor in the saturation region. A high input voltage V_{in} is applied at the base.

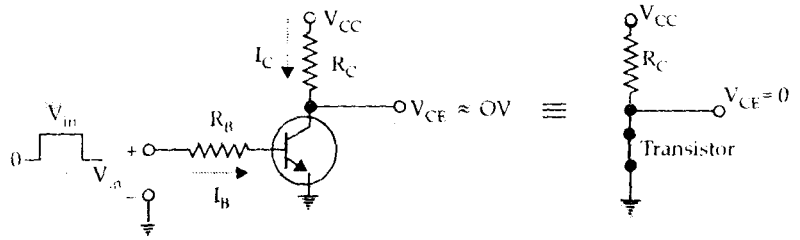


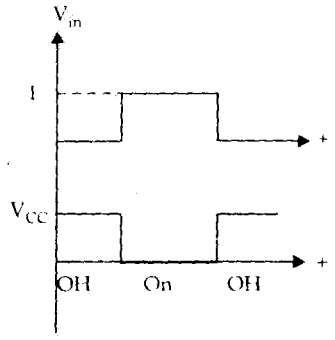
Fig.(b) : Transistor in saturation is equivalent to an close switch

2. The value of V_{in} and resistance R_B are adjusted such that a large I_B flows. This will saturate the transistor. The value of I_B should be such that the following condition should be satisfied.

$$I_B \geq \frac{I_{C\,(sat)}}{\beta}$$

3. In the saturation region but the junctions of a transistor are forward biased: The voltage drop across the transistor (V_{CB}) is very small of the order of 0.2V to 1V depending on the type of transistor and collector current is very large.
4. A low (almost 0) Voltage drop across 5 the transistor and a large current through it indicates that the transistor is equivalent to a closed switch.

Switching wave form :



(f) Define and explain the following terms in case of a photo detector:

(i) Responsivity, (ii) Quantum Efficiency, (iii) Directivity, (iv) Dark Current.

Ans. (i) Responsivity : It is defined as the ratio of the generated photocurrent (I_{ph}) and the incident optical power (ϕ)

$$R = \frac{I_{ph}}{\phi} \; (A/w)$$

$$\text{Max. responsibility } R_{max} = \frac{q}{Eg}$$

$$\left(I_{ph} = \frac{q\phi}{Eg} \right)$$

(ii) Quantum Efficiency : Some of the photogenerators carriers would recombine and thus, their number would be typically less than teh number of incident photons. This is quantum efficiency (η)

$$\eta = \frac{\text{no. of enerated EHP}_s / \text{sec}}{\text{no. of incident photon / sec}}$$

$$\eta = \frac{I_{ph} / q}{\phi / E_{ph}} = \frac{R\,hc}{q\lambda}$$

(iv) Dark Current : It is the current that flow through thephotodiode in the absence of any illumination and is due to the reverse saturation current of the diode as well as the current due to carriers.

Q.2. Attempt any two parts of the following: **(10 × 2 = 20)**

(a) Why π-parameters could not be used for high frequency analysis of the transistors? Give the hybrid-π equivalent circuit of a Bipolar Junction Transistor, explaining the significance of the terms appearing in the circuit. Define the following—f_α, f_β and f_γ and derive the relationship between f_α and f_β.

Ans. h-parameter is used for frequency in low frequency analysis capacitance did not show it's effect but high frequency analysis capacitance show it's effect.

Hybrid π model Transistors

1. The simplified extended hybrid π equivalent circuit is shown if Fig. (a)

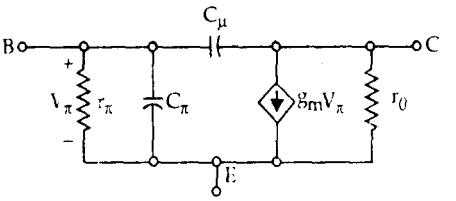


Fig. (a) : Simplified extended hybrid π equivalent circuit

2. Note that the resistance r_b, r_c, r_{ex} and r_μ alongwith the capacitance C_s have been neglected.
3. The small resistance r_b, r_c and r_{ex} have been replaced by short circuits whereas r_μ and C_s have been replaced by open circuit.
4. To obtain the short circuit gain, we use the approximate extended hybrid πeqivalent circuit with collector-emitter terminals short circuited as shown in Fig. (b)
5. The transistor is based to operate in the forward active region.
6. The small-signal current gain $A_I = I_c / I_b$

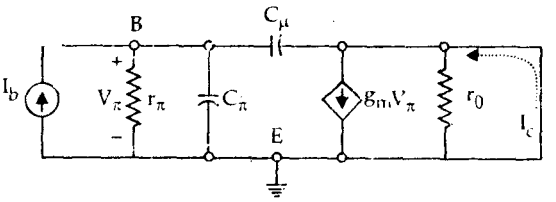


Fig. (b) : Simplified hybrid π equivalent circuit to determine the short circuit gain

Step 1 : Obtain the expression for I_b:

Refer fig. (c) and write KCL at node B

At node B we can write

$$I = I_1 + I_2 + I_3 = \frac{V_\pi}{r_\pi} + \frac{V_\pi}{X_C\pi} + \frac{V_\pi}{X_C\pi} = \frac{V_\pi}{r_\pi}$$

$$= \frac{V_\pi}{(1/\omega C_\pi)} + \frac{V_\pi}{(1/j\omega C_\mu)}$$

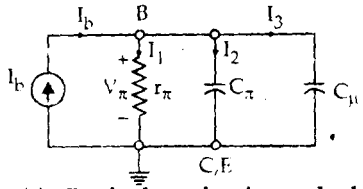


Fig. (c) : Equivalent circuit to calculate I_b

$$\therefore \quad I_b = V_\pi \left[\frac{1}{r_\pi} + j\omega (C_\pi + C_\mu) \right] \qquad ...(1)$$

Step 2 : Obtain the expression for I_c :

Now refer fig. (d) and apply KCL to the output node *i.e.* Node "C".

Applying KCL at node C we get,

$$I_3 + I_c = g_m V_\pi$$

$$\therefore \quad \frac{V_\pi}{X_C\mu} + I_c = g_m V_\pi$$

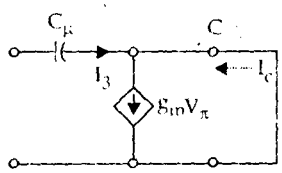


Fig. (d) : Equivalent circuit to calculate I_c

$$\therefore \quad \frac{V_\pi}{1/j\omega C_\mu} + I_c = g_m V_\pi$$

$$\therefore \quad j\omega C_\mu V_\pi + I_c = g_m V_\pi$$

$$\therefore \quad I_c = V_\pi (g_m - j\omega C_\mu) \qquad ...(2)$$

Step 3 : Obtain the expression for A_1 :

$$I_c = V_\pi (g_m - j\omega C_\mu)$$

$$\therefore \quad V_\pi = \frac{I_c}{(g_m - j\omega C_\mu)} \qquad ...(3)$$

Substituting the expression for V_π into the expression for I_b we get

$$I_b = \frac{I_c}{(g_m - j\omega C_\mu)} \left[\frac{1}{r_\pi} + j\omega (C_\pi + C_\mu) \right]$$

Therefore the small signal current gain is given by :

$$A_I = \frac{I_c}{I_b} = h_{fe} = \frac{g_m - j\omega C_\mu}{\left[\frac{1}{r_\pi} + j\omega (C_\pi + C_\mu) \right]} \qquad ...(4)$$

This is the exact expression for the small signal current gain But if we substitute $C_\mu = 0.2$ pF, $g_m = 50$ mA/V and $f = 100$ MHz, then $\omega C_\mu << g_m$. So the expression for A_I can be approximated as follows :

$$A_I \approx h_{fe} \approx \frac{g_m}{\frac{1}{r_\pi} + j\omega (C_\pi + C_\mu)}$$

$$= \frac{g_m r_\pi}{1 + j\omega r_\pi (C_\pi + C_\mu)} \qquad ...(5)$$

Equation for A_I tells us that the magnitude and phase of the current gain A_I are functions of frequency.

Fig. 1. (a) shows a Bode plot of the short circuit current gain magnitude whereas fig 1. (b) shows the phase of the current gain.

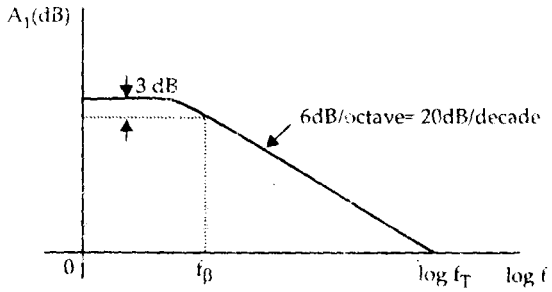


Fig. (a): Magnitude of short circuit current gain Vs frequency

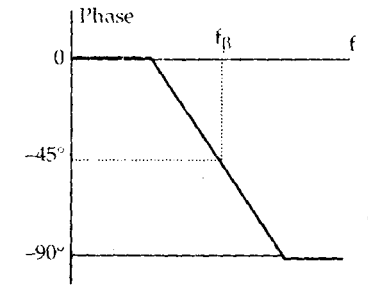


Fig. (b)Phase of S.C. current gain

1. Note that A_I (db) = 0 dB at frequency $f = f_T$ and for $f >> f_\beta$ the graph is a straight line havinga slope of 6 dB/octave or 20 dB/decade.
2. Let us now define various frequencies such as f_α, f_β and f_T.

Cut-off Frequency f_β :

1. This is the frequency at which the short circuit CE gain of the transistor drops by 3 dB from its value at low frequency as shown in Fig. The frequency range upto f_β is referred to as the bandwidth of the circuit. The expression for f_β is given by,

$$f_\beta = \frac{1}{2\pi r_\pi (C_\pi + C_\mu)} \quad ...(6)$$

2. Thus the current gain reduces to 0.707 or 7.7% of the low frequency current gain

$$f = f_\beta$$

Cut-off Frequency f_α :

We can define f_α on the similar lines as that of f_β. Therefore f_α is detined as the frequency at which the short circuit CB gain of the transistor drops by 3 dB from its value at low frequency.

The expression for f_α can be derived in a similar manner as f_β. The current gain of the CB configuration is given by,

$$A_I = \frac{-h_{fb}}{1 + j[f / f_\alpha]}$$

$$|A_I| = \frac{h_{fb}}{\sqrt{1 + [f / f_\alpha]^2}} \quad ...(7)$$

Hence at $f = f_\alpha$

$$|A_I| = \frac{h_{fb}}{\sqrt{2}} \quad ...(8)$$

Thus at $f = f_\alpha$ the common base short circuit current gain reduces to 0.707 of it current gain at low frequency *i.e.*, h_{fb}

The Cut off Frequency f_T :

1. It is the frequency at which the short circuit CE current gain attains unit magnitude (*i.e.*, $A_I = 1$)

   We know that,

$$A_I = \frac{\beta_0}{\sqrt{1 + [f / f_\beta]^2}}$$

   where β_0 = dc current gain
2. At $f = f_T$, $A_I = 1$

$$\therefore \quad 1 = \frac{\beta_0}{\sqrt{1 + [f_T / f_\beta]^2}}$$

   Assuming $\frac{f_T}{f_\beta} >> 1$ we get

$$1 = \frac{\beta_0}{[f_T / f_\beta]} = \frac{f_\beta \cdot \beta_0}{f_T} \quad ...(9)$$

$$\therefore \quad f_T = f_\beta \cdot \beta_0 \quad ...(10)$$

3. Substituting the value of f_β we get,

$$f_T = \frac{1}{2\pi r_\pi (C_\pi + C_\mu)} \times \beta_0$$

But $g_m r_\pi = \beta_0$

$$\therefore \quad f_T = \frac{g_m}{2\pi (C_\pi + C_\mu)} \quad ...(11)$$

Frequency f_β is also called as the bandwidth of transistor. Hence $f_T = \beta_0 f_\beta$ is called as the gain-bandwidth product of the transistor or unity gain bandwidth.

(b) Give the high frequency small-signal circuit of a MOSFET with load resistance showing the effect of Miller capacitance. Also drive an expression for the Miller capacitance and cut-off frequency (f_T).

Ans. Miller Effect and Miller Capacitance:

1. We have considered the Miller effect for transistors and we will do it for the FETs now
2. The simplified high frequency FET model is shown in fig. (a). This includes the load resistance R_L.
3. Let us now understand the Miller effect. In order to do so we have to obtain the current gain of the amplifier.
4. Now to obtain the expression for current apply KCL at the input node to write.

$$I_i = I_1 + I_2$$

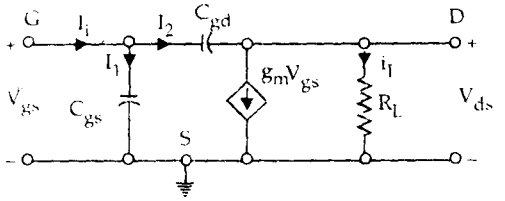


Fig. (a) : High frequency small signal circuit of a MOSFET with load resistance

$$\therefore \quad I_i = j\omega C_{gs} V_{gs} + j\omega C_{gd} (V_{gs} - V_{gd}) \quad ...(1)$$

5. Apply KCL at the output node to get.

$$I_2 = g_m V_{gs} + I_L$$

$$\therefore \quad j\omega C_{gd} (V_{gs} - V_{ds}) = g_m V_{gs} + \frac{V_{ds}}{R_L}$$

$$\therefore \quad g_m V_{gs} + \frac{V_{ds}}{R_L} + j\omega C_{gd} (V_{ds} - V_{gs}) = 0$$

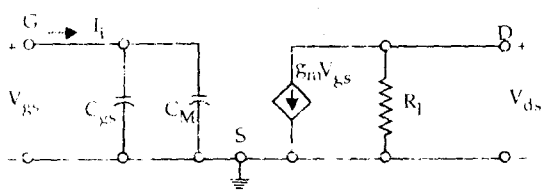


Fig. (b) : High frequency equivalent circuit including the Miller capacitance

...(2)

6. Combining Equations (1) and (2) we get,

$$I_i = j\omega \left\{ C_{gs} + C_{gd} \left[\frac{1 + g_m R_L}{1 + j\omega R_L C_{gd}} \right] \right\} V_{gs}$$

...(3)

7. But generally $(\omega R_L C_{gd}) << 1$. Hence we can neglect this term, to modify Equation (3) as follows

$$I_i = j\omega \left\{ [C_{gs} + C_{gd} (1 + g_m R_L)] \right\} V_{gs}$$

...(4)

8. So we can define the Miller capacitance C_M as,

$$C_M = C_{gd} (1 + g_m R_L) \quad ...(5)$$

9. The Miller capacitance is shown on the input side in the equivalent circuit of Fig. (b)

10. Thus the input current I_i can be expressed as

$$I_i = j\omega [C_{gs} + C_M] V_{gs} \quad ...(6)$$

11. The expression for C_M reveals the effect of the parasitic drain overlap capacitance (C_{gd}).

Cut off Frequency of MOSFET (f_T)

The cut off frequency of MOSFET *i.e.*, f_T is defined as the freqeuncy at which the current gain magnitude is 1 or when the input current I_i is equal to the ideal load current I_d.

But $I_i = j\omega (C_{gs} + C_M) V_{gs}$ ...(7)

and the ideal load current is given by,

$$I_d = g_m V_{gs} \quad ...(8)$$

Hence the magnitude of current gain is.

$$|A_i| = \left| \frac{I_d}{I_i} \right| = \frac{g_m V}{j\omega (C_{gs} + V_{gs})}$$

$$\therefore \quad |A_i| = \frac{g_m}{2\pi f (C_{gs} + C_M)}$$

At $f = f_T$ $|A_i| = 1$

$$\therefore \quad 1 = \frac{g_m}{2\pi f_T (C_{gs} + C_M)}$$

$$\therefore \quad f_T = \frac{g_m}{2\pi (C_{gs} + C_M)}$$

Letting $(C_{gs} + C_M) = C_G$ *i.e.*, the equivalent gate capacitance we get

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_M)} = \frac{g_m}{2\pi C_G}$$

(c) What are the general properties of Negative feedback? And explain how negative feedbacks can used for input restance, output resistance, and bandwidth stability.

Ans. General Properties of Negative feedback :

Sr. No.	Characteristics	Types of feedback			
		Series shunt	Series series	Shunt shunt	Shunt series
1.	Gain (A_f)	Reduces	Reduces	Reduces	Reduces
2.	Gain stability	Improved	Improved	Improved	Improved
3.	Input resistance	Increases	Increases	Decreases	Decreases
4.	Output resistance	Decreases	Increases	Decreases	Increases
5.	Nonlinear distortion	Decreases	Decreases	Decreases	Decreases
6.	Noise	Decreases	Decreases	Decreases	Decreases
7.	Frequency distortion	Decreases	Decreases	Decreases	Decreases
8.	Bandwidth	Increases	Increases	Increases	Increases

Effects of Negative Feedback on the Input Resistance :

To understand the effect of negative feedback on the input resistance, let us divide the four configurations into two groups :

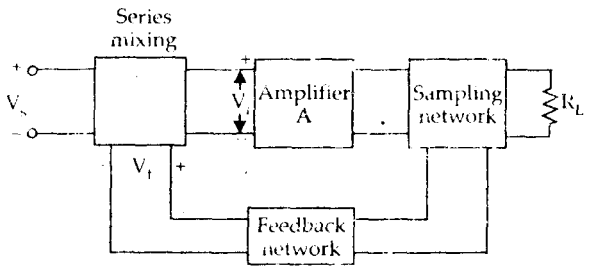


Fig. (a) : Feedback amplifier using series mixing (Series shunt and series series feedback)

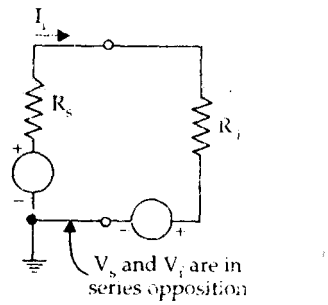


Fig. (b): Equivalent circuit

Effect of Series shunt and Series series feedback :

1. The block diagram of the "series type" feedback amplifier is an shown in Fig (a). This type of feedback amplifier uses "series mixing" on the input side, *i.e.*, signal voltage V_s and feedback voltage V_f are mixed in series. The equivalent circuit of series mixing type amplifiers is shown in Fig.
2. The feedback signal V_f is in series opposition with the signal voltage V_s as sown in Fig. (b). Therefore the current I_i will decrease with increase in negative feedback. The input resistance with feedback is given

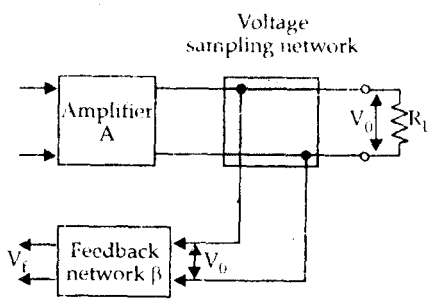


Fig. (a) Feedback amplifiers with voltage sampling (Series shunt and shunt shunt feedback)

Negative feedback $R_{if} = \frac{V_s}{I_i}$

Effect of the Output Resistance :

To understand the effect of negative feedback on the output resistance, let us divide the four feedback configuration into two groups based on the type of sampling :

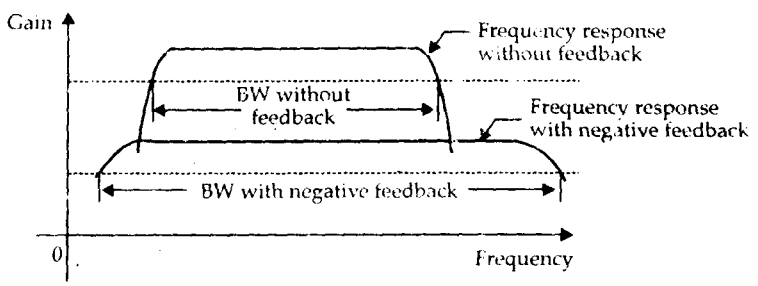


Fig. Effect of Negative feedback on Bandwidth

Effect on series shunt and shunt shunt feedback :

1. The first group uses voltage sampling while the second one uses the current sampling.
2. In the voltage sampling type amplifiers, the feedback network appears in parallel with R_l as shown in fig. (a)
3. The feedback network is a resistive network. Hence this parallel connection will decrease the output resistance when we connect two resistors R_1 and R_2 parallel to each other, their parallel combinations has a value less than R_1 as well as R_2.
4. **Thus output resistance decreases for series shunt and shunt shunt type feedback amplifiers.**

Effect on Bandwidth

1. One of the most important advantages of the negative feedback is that it increases the bandwidth of the amplifier.
2. For any amplifier, the product of voltage gain and bandwidth always remains constant.

   Gain × Bandwidth = Constant
3. With the negative feedback, gain reduces therefore to keep the value of the product constant, bandwidth of the amplifier increases proportionally.
4. It is possible to obtain the desired bandwidth by selecting a proper feedback factor β. The increase in bandwidth due to the negative feedback is shown in fig.
5. Also note the reduction in gain due to negative feedback.

Q.3. Attempt any two parts of the following: **(10 × 2 = 20)**

(a) Explain the Barkhausen criteria for oscillators. And also derive the necessary conditions required for oscillations. What are the factors on the basics of which oscillators are classified ?

Ans. Barkhausen Critiers :

1. The Barkhausen criteria should be satisfied by an amplifier with positive feedback to ensure the sustianed oscillations.
2. For an oscillator circuit, there is no input signal "V", hence the feedback signal V_f itself should be sufficient to maintain the oscillations.
3. Refer Fig. to understand the Barkhausen critiera

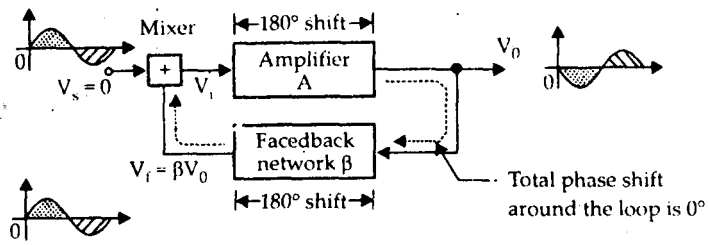


Fig. : Block diagram of an oscillator

(i) From Fig. the expression for output voltage V_0 is

$$V_0 = AV_i$$

(ii) But V_i is the sum of V_s and V_f

$$\therefore \quad V_i = V_s + V_f \qquad ...(1)$$

Note that we have added V_s and V_f because in positive feedback, V_s and V_f will be in phasewith each other and hence will get added

(iii) The expression for feedback voltage is,

$$V_f = \beta V_0 \qquad ...(2)$$

Substitute the value of V_0 frm Equation (1) into Equation (2) to get,

$$V_f = \beta\, AV_i \qquad ...(3)$$

(iv) Substitute this equation into Equation (2) to get

$$V_i = V_s + A\beta V_i$$

$$\therefore \quad (1 - A\beta)\, V_i = V_s \qquad ...(4)$$

(v) For an oscillator the input voltage V_s is absent *i.e.*, $V_s = 0$ and the feedback signal V_f is supposed to maintain the oscillations. Therefore substitute $V_s = 0$ into Equation (4) to get

$$V_i(1 - A\beta) = 0 \qquad \text{or} \qquad A\beta = 1 \qquad ...(5)$$

4. This condition must be satisfied in order to obtain sustained oscillations. Alongwith this condition, the condition for the positive feedback which states that the phase shift between V_s and V_f must be zero, should also be satisfied.
5. With an inverting amplifier introducing as 180° phase shift between V_i and V_0, the feedback network must introduce another 180° phase shift to ensure that V_i and V_f are in phase.
6. These two conditions which are required to be satisfied to operate the circuit as an oscillator are called as the "Barkhausen criterion" for sustained oscillations.

Statement of Barkhausen criterion :

The Barkhausen criterion states that :

1. An oscillator will operate at that frequency for which the total phase shift introduced as the signal proceeds from the input terminals, through the amplifier and feedback network and back again to the input is precisely 0° or 360° or integral multiple of 360°

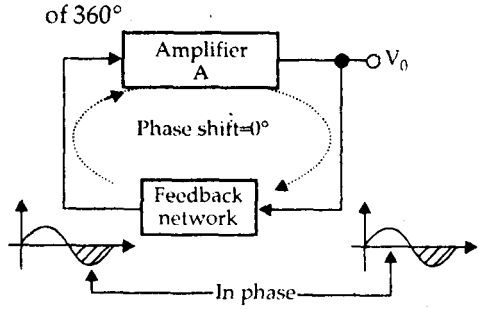


Fig. (a) The phase shift around the loop is 0°

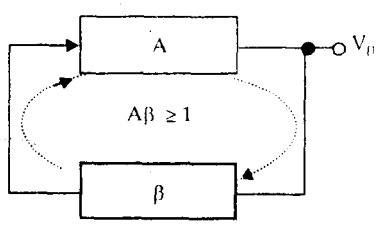


Fig. (b) Loop gain Aβ > 1

Fig. : Barkhausen criterion

2. At the oscillator frequency, the magnitude of the product of open loop gain of the amplifier A and the feedback factor β is equal to or greater than unity.

$$\therefore \quad |A\beta| \geq 1$$

The product $A\beta$ is called as the "loop gain"

These conditions are diagrammatical illustrated in Fig. (a) and (b)

Classification Based on the Nature of Output Waveform :

1. The oscillator output voltage can be either sinusoidal or nonsinusoidal.
2. So we can classify the oscillators as sinewave oscillators and nonsinusoidal oscillators.
3. The examples of sinusoidal oscillators are : RC-phase shift Wien bridge, Hartley, colpitt, Clapp oscillators
4. The nonsinusoidal oscillators can produce either square wave or triangular, ramp waves at their output. Multivibrators of all kinds are the square wave oscillators.

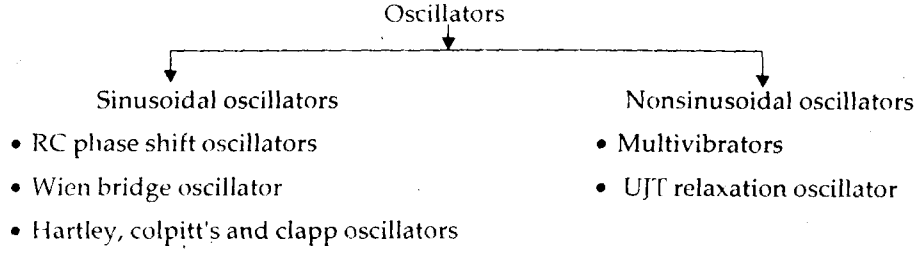


Fig. Classification based on nature of output waveform

Classification Based on the types of Components used :

1. Depending on the components used for the feedback network, the oscillators are classified as RC oscillators and LC oscillators.
2. The RC oscillators use only resistors (R) and capacitors (C) in their feedback network whereas the LC oscillators use inductors (L) and capacitors (C).
3. Examples of RC oscillators are RC-phase shift oscillator and Wien bridge oscillator whereas Hartley, Colpitt's and Clapp oscillators are the well known examples of LC oscillators.

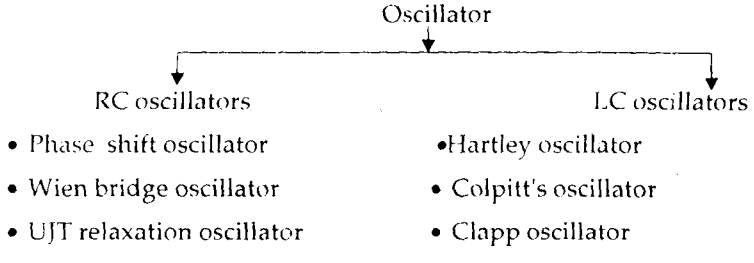


Fig. Classification based on the components used

Classification Based on the Range of Operating Frequency :

1. Based on the range of operating frequency the oscillators can be divided into two categories namely low frequency (LF) oscillators and high frequency (HF) or radio frequency (RF) oscillators.

2. The frequency range of LF oscillators is approximately from 20 Hz to 100 KHz and they are generally RC oscillators. The operating frequency for the HF oscillators is in the range of 100 kHz to a few GHz. These are LC oscillators.

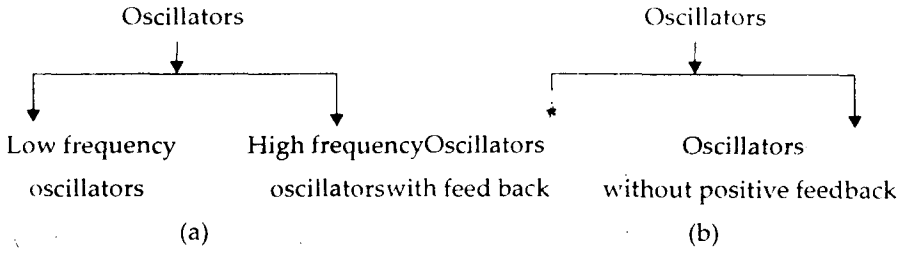


Fig.

(b) Design an RC phase shift osillators using BJT for a frequency of 1KHZ. The stability factor S ≤ 8. Given that V_{cc} = 10 V. The transistor has h-parameters as follows—h_{ie} = 1kΩ, h_{fe} = 50, h_{re} = h_{oe} = 0.

Ans. Step 1 : Draw the circuit :

The RC oscillator to be designed is as shown in Fig.

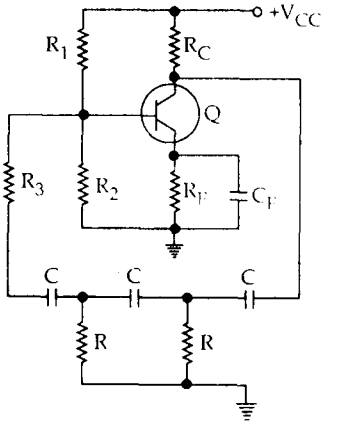


Fig. : RC oscillator to be designed

Step 2 : Design of RC network :

$$f = \frac{1}{2\pi RC} \cdot \frac{1}{\sqrt{6 + (4k)}}$$

where $k = R_f / R$

The minimum value of $k = 2.7$

$$\therefore \quad 1 \times 10^3 = \frac{1}{2\pi RC} \cdot \frac{1}{\sqrt{6 + (4 \times 2.7)}}$$

$$\therefore \quad RC = 3.8829 \times 10^{-5}$$

Let $C = 0.1\,\mu F$

$$\therefore \quad R = \frac{3.8829 \times 10^{-5}}{0.1 \times 10^{-6}}$$

$$\therefore \quad R = 388.3\Omega$$

Select R = 390 Ω as the standard value

Step 3 : DC circuit design :

$$R_C = k \times R = 2.7 \times 390 = 1053\,\Omega$$

Select R_C = 1kΩ as the standard value.

V_E should be atleast equal to 3V for good stability.

$\therefore$ Let $V_E = 3V$

Also V_{CEQ} should be atleast equal to 3V to ensure that the BJT is in the active region

$$\therefore \quad V_{CEQ} = 3V$$

$$\therefore \quad I_{CQ} = \frac{V_{CC} - (V_{CEQ} + V_E)}{R_C}$$

$$= \frac{10 - (3 + 3)}{1\,k\Omega} = 3\,mA$$

Let $I_E \approx I_{CQ} = 4\,mA$

$$\therefore \quad R_E = \frac{V_E}{I_E} = \frac{3V}{4mA} = 750\,\Omega$$

The stability factor

$$S = (1 + \beta)\frac{1 + (R_B / R_E)}{1 + \beta + (R_B / R_E)}$$

Let $\beta = h_{fe} = 50$, $s = 8$

$$\therefore \quad 8 = (1 + 50)\frac{1 + (R_B/750)}{1 + 50 + (R_B/750)}$$

$$\therefore \quad 408 + \frac{8R_B}{750} = 51 + \frac{51}{750}R_B$$

$$\therefore \quad R_B = 6085.23\,\Omega$$

But $R_B = R_1 \| R_2$ Let $R_2 = 10\,k\Omega$

$$\therefore \quad 6.085 = \frac{10R_1}{10 + R_1}$$

$$\therefore \quad 60.85 + 6.085R_1 = 10R_1$$

$$\therefore \quad R_1 = 15.54\,k\Omega$$

The bypass capacitor C_E can be calculated as follows:

$$X_{CE} \le 0.1R_E$$

$$\therefore \quad \frac{1}{2\pi f C_E} \le 0.1 \times 750$$

$$\therefore \quad \frac{1}{2\pi f \times 75} \le C_E$$

$$\therefore \quad C_E \le \frac{1}{2\pi \times 1 \times 10^3 \times 75}$$

$$\therefore \quad C_E \ge 2.12\,\mu F$$

Select $C_E = 4.7\,\mu F$ ...standard value

Step 4 : Check the value of $A\beta$

$$\text{Gain } A = -h_{fe}\frac{R_C}{h_{ie}} = -50 \times \frac{1}{1} = -50$$

The gain is greater than 29. So the $AB \ge 1$ and there will be sustained oscillations.

Component Values

$R_1 = 15.54\,k\Omega$, $R_C = 1\,k\Omega$, $R_L = 750\,k\Omega$

$C = 0.1\,\mu F$ $R_2 = 10\,k\Omega$ $R = 390\,\Omega$,

$C_E = 4.7\mu F$

(c) Explain the operation of a Wien-Bridge oscillator and derive the necessary condition for oscillation. Give the equivalent circuit of a crystal and give the advantages of a crystal osillator.

Ans. Wien Bridge oscillator

1. The feedback network used for this type of oscillator is called as "Wien bridge". Therefore the name wien bridge oscillator.
2. Before we start analyzing various circuits for the Wien bridge oscillator, let us analyze the Wien bridge circuit.

The Wien Bridge Circuit :

1. The "Wien bridge" which is used as the feedback network in Wien bridge oscillator is shown in Fig. (a) and Fig (b) shows the basic Wien Bridge oscillator.
2. The amplifier in Fig (b) can use a transistor or FET or an OP-AMP as amplifying device.
3. The Wien bridge of Fig (a) has four arms. The arms AD which consists of the series combination of R_1 and C_1 and the arm CD which consists of the parallel combination of R_2 and C_2 are called as the frequency sensitive arms. This is became the components connected in these arms decide the oscillator frequency.
4. The resistors R_3 and R_4 are used to generate a reference voltage which remains constant independent of frequency.
5. The ac input voltage is applied between points "A" and "C" of the bridge. When the Wien bridge is used in the oscillator

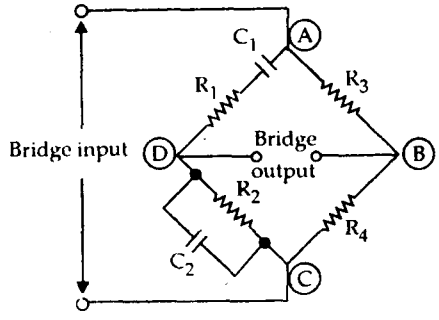


Fig. (a) : Basic Wien bridge circuit

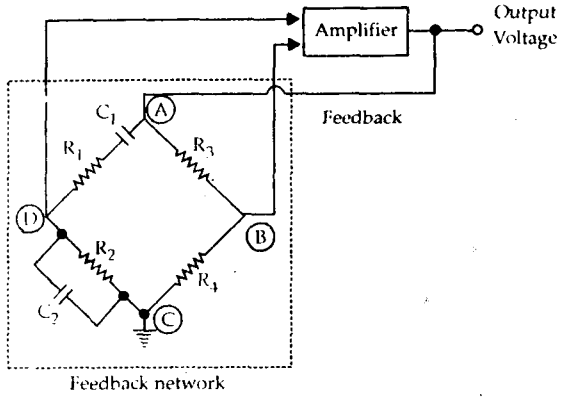


Fig. (b) : Basic Wien bridge oscillator

circuit, the feedback voltage is applied between these points as shown in Fig. (b)

6. The ac output of the bridge is obtained between points "B" and "D" of the bridge. When used in the oscillator circuit these points are connected to the input of the amplifier as shown in Fig. (b)
7. Wien bridge of Fig. (a) is used a feedback network in the Wien bridge oscillator circuit as shown in Fig. (b) It is also called as the "Lead-Lag Network". At low frequencies it acts like a lead network whereas at high frequencies it acts like a lag network. But the phase shift introduced at the output frequency is 0°.

Necessary condition for oscillators :

1. The positive sign of β in equation shows that phase shift introduced of frequency f is zero, to satisfiy the other condition

$|AB| \geq 1, \quad \beta = 1/3$ than $A \geq 3$

The amplifier gain should be at least equal to 3 to ensure substained oscillation.

Equivalent Circuit of a Crystal oscillator

1. The ac equivalent circuit of a crystal is as shown in Fig. (b) It shows that the crystal is equivalent to a resonant circuit.
2. In the ac equivalent circuit of a vibrating crystal, the internal frictional losses are represented by a resistance R.

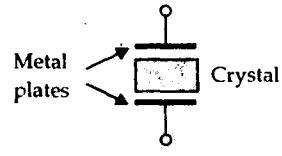


Fig. (a): Crystal

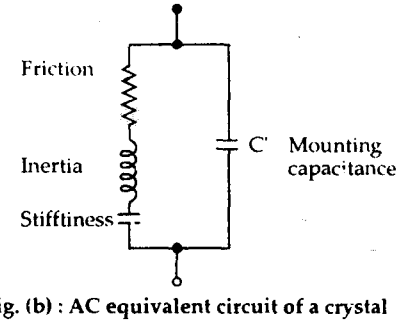


Fig. (b) : AC equivalent circuit of a crystal

3. Mass of the crystal and hence its inertia is represented by L and stiffness under the vibrating condition is represented by capacitor C.
4. Due to the mounting arrangement shown in Fig. (a) the crystal is equivalent to a capacitance denoted by C' in the equivalent circuit C' is called as the mounting capacitance.

Resonant frequencies :

1. There are two resonant circuits existing in the ac equivalent circuit of the crystal RLC form a series resonant circuit and RLC in parallel with C' will form a parallel resonant circuit. The resonant fre-

quency of the series R-L-C series circuit is given by :

$$f_s = \frac{1}{2\pi\sqrt{LC}}$$

2. This is with an assumption that quality factor Q is very large. The resonant frequency of the parallel resonant frequency formed by R-L-C and C′ is given by :

$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

Where, $C_{eq} = \frac{CC'}{(C + C')}$

Advantage of Crystal Oscillators

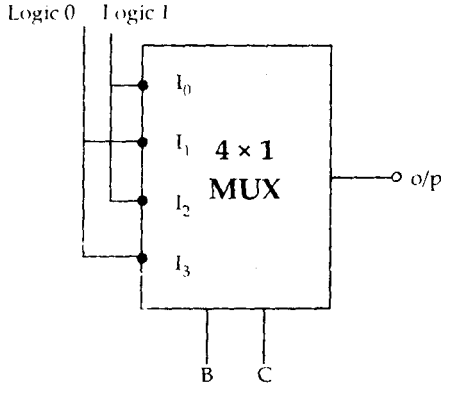
1. Very high frequency stability.
2. Very low frequency drift due to change in temperature and other paremeter.
3. It is possible to obtain very high pricise and stable frequency of oscillation
4. The Q is very high.

Q.4. Attempt any four parts of the following: (5 × 4 = 20)

(a) Define combinational circuit. Realize the following expression f (A,B, C)=Σm (0, 2, 6) using a 4:1 multiplexer.

Ans. $f(A, B, C) = \sum n(0, 2, 4, 6)$

	I_0	I_1	I_2	I_3
$\overline{A}$	(0)	1	(2)	3
A	(4)	5	(6)	7
	1	0	1	0



(b) Explain the difference between Latch and Flip-Flop. Explain how a D flip-flop is obtained from a JK flip-flop.

Ans. Difference between Latch and Flip-Flop.

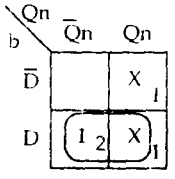
1. Latch are unlock Flip-Flop or we can say Latch have no clock element. But Flip-Flop have clock.

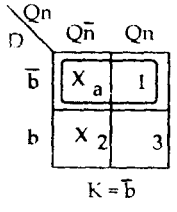
Conversion of Flip-Flop J-K to D

Truth table for J-K to D conversion

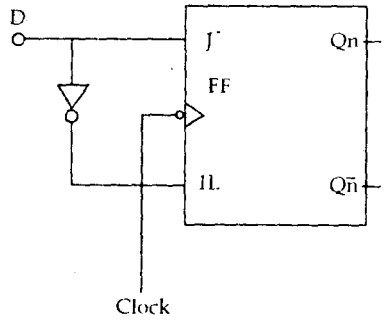
D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
1	0	1	1	X
0	1	0	X	1
1	1	1	X	0

k-map simplification





Logic Diagram 1



(c) Design a 3-bit Bi-Directional Shift resistor using JK Flip-Flop.

Ans. A 3-bit Bidirectional shift register using JK flip flops is shown in Fig.

1. This circuit is same 4-bit bi-directional shift Register discussed
2. The only modification is the inclusion of an inverter between the J and K inputs of each Flip-Flops.
3. With M = 1, the shift Right operation will take place and for M = 0 shift left operation will take place.

(d) What is a universal shift register? Explain its operation with the help of a logic diagram showing all the necessary signals.

Ans. Universal Shift Register :

1. A shift register which can shift the data in only one direction is called as unidirectional shift register.
2. A shift register which can shift the data in both the directions is called as a bi-directional shift register.
3. Applying the same logic, a shift register which can shift the data in both the directions (shift right or left) as well as load it parallely, then it is called as **a universal shift register.**
4. Fig shows the logic diagram of a universal shift register.

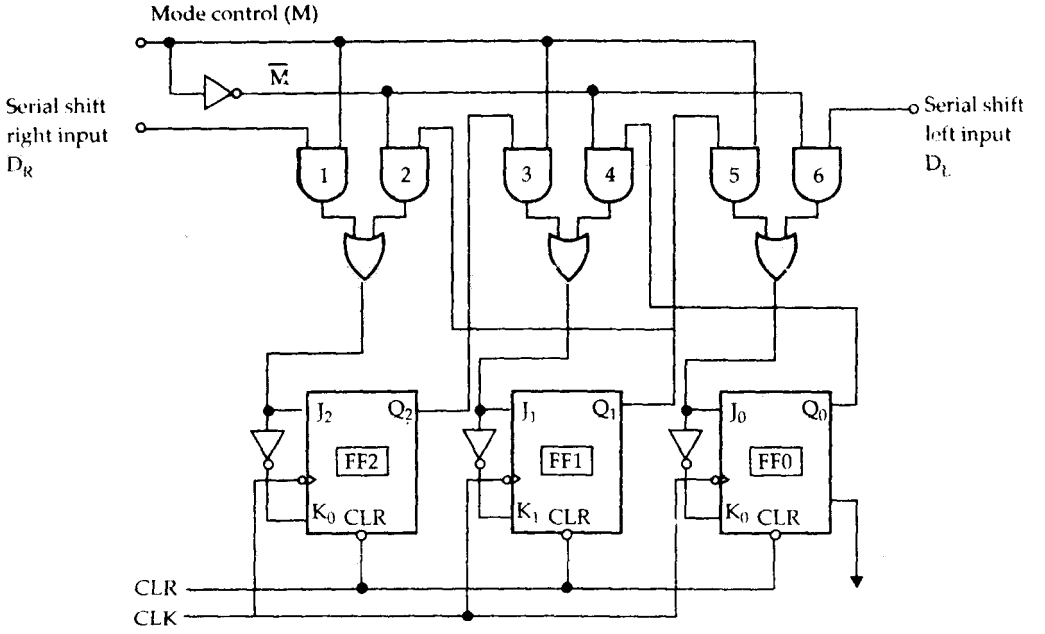


Fig.A 3 bit bi-directional shift register using JK flip flops

5. This shift register is capable of performing the following operations :
   (i) Parallel loading (prallel input parallel output)
   (ii) Left shifting
   (iii) Right shifting

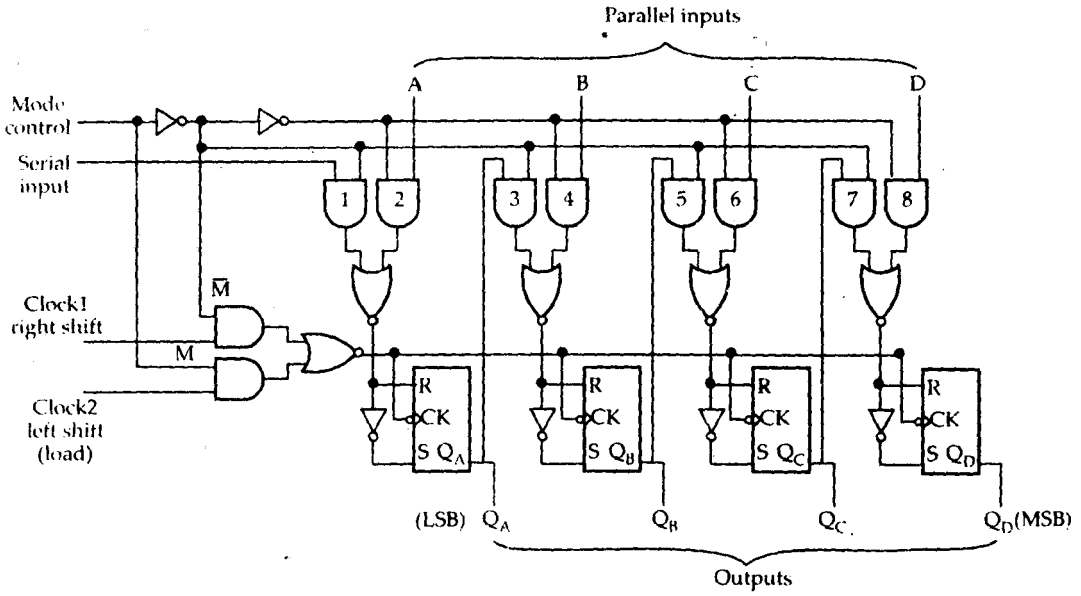
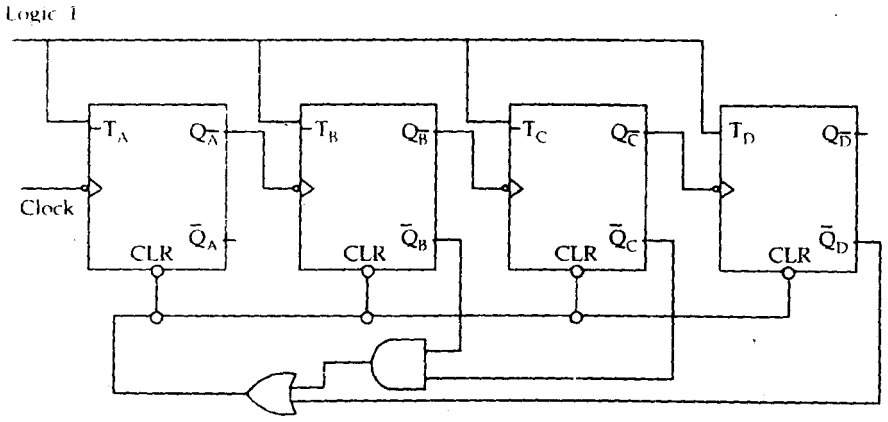


Fig. Logic diagram of a universal shift register

6. The Mode control input is connected to Logic 1 for parallel loading operation whereas it is connected to 0 for serial shifting.
7. With mode control pin connected to ground, the universal shift register acts as a bi-directional register.
8. For serial left operation, the inputs is applied to the serial input which goes to AND gate-1 in Fig.
9. Whereas for the right operations input is applied to D-input.

(e) Differentiate between synchronous and asynchronous counter. Give the logic diagram of a BCD counter.

Ans. A synchronous Counter: For these counter external clock signal is applied to on Flip-Flop and then output of preceding Flip-flop is connected to the clock of Next flip-Flop

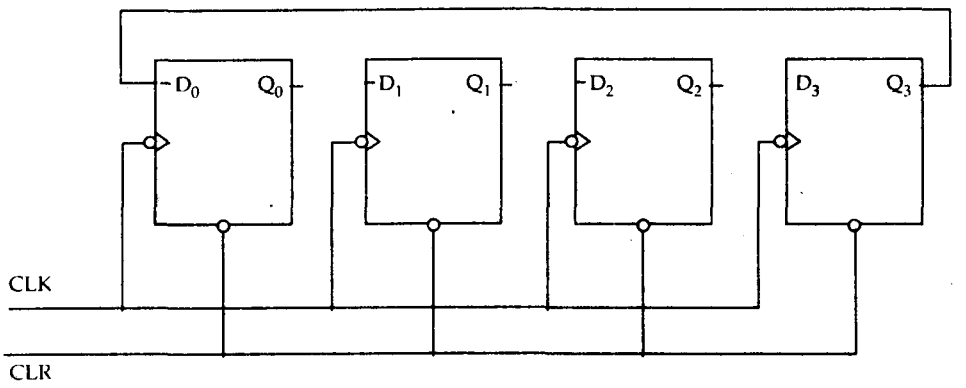


Synchronous Counter : In synchronous counter all the Flip-Flop receive the external clock pulse simultaneously.

Logic diagram of BCD counters :

(f) Explain the operation of a johnson counter using D flip-flop.

Ans. Johnson's counter using D Flip-Flop :



The operations is given below :

CLR	CLK	Q_0	Q_1	Q_2	Q_3
1	↓	1	1	0	0
1	↓	1	1	1	0
1	↓	1	1	1	1
1	↓	0	1	1	1
1	↓	0	0	1	1
1	↓	0	0	0	1
1	↓	0	0	0	0

Q.5.. Attempt any four parts of the following: **(5 × 4 = 20)**

(a) Give the circuit diagram of a Non-inverting Schmitt trigger and derive the expression for *Hystersis voltage.*

Ans. Non-Inverting Schmitt Trigger :

1. The circuit diagram of Non-inverting Schmitt trigger is given
2. The external input signal is being applied to the non-inverting Terminal of the op-amp and the two resistor R_1 and R_2 are connected to provide a positive feedback.

The operation of non-inverting schmitt trigger is summarised as follows :

1. Initially the OPAMP output is asumed to be equal to $- V_{sat}$

↓

2. Output will switch to $+ V_{sat}$ when $V_{in} = V_{ul} = \frac{R_1}{R_2} V_{(sat)}$

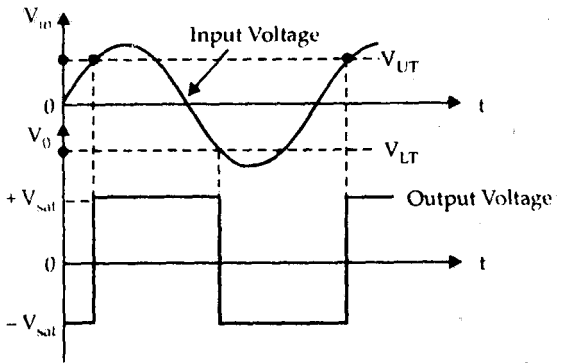


Fig. (a) : Input and output voltage waveforms of an on-inverting schmitt trigger

↓

3. Now the feedback voltage is positive hence to change the state of output, a sufficient negative voltage should be applied.

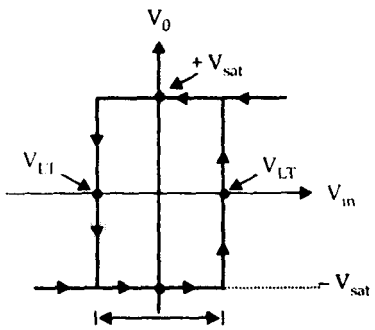


Fig. (b) : Transfer characteristic of a non-inverting schmitt trigger

↓

4. Output will switch to $-V_{sat}$ when $V_{in} = V_{LT} = \frac{-R_1}{R_2} V_{(sat)}$

This operation will repeat

The output voltage waveform is very similar to that for an inverting schmitt trigger, except for 180° phase reversal.

(b) Explain the operation of a Astable Multivibrator circuit using an Op-Amp. Also derive the expression for cut off frequency.

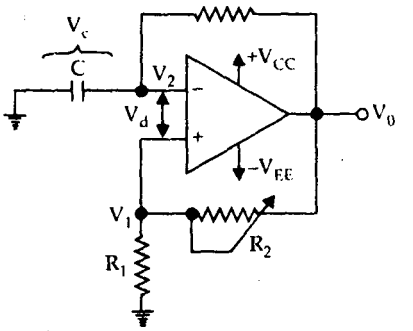


Fig. (a) : Square wavegenerator

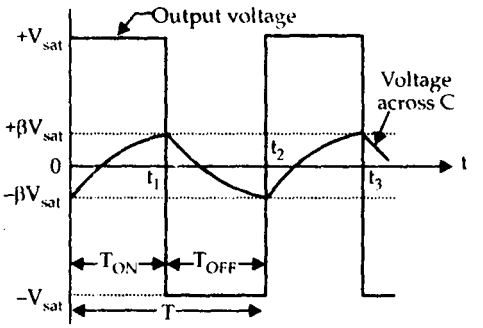


Fig. (b) : Waveforms for a square wave generator

Ans. Astable Multivibrator :

1. The OP-AMP can be used to generate waveforms such as square wave, triangular wave or sawtooth wave etc.
2. The square wave generator is also known as the free running or stable multivibrator. The schematic diagram of the square wave generator is as shown in Fig. (a) and the relevant waveforms are as shown in fig. (b)

Operation of the circuit :

1. Let the voltage on the capacitor C is zero when power is applied to the circuit. Therefore initially voltage at the inverting (–) terminal is zero ($V_2 = 0$)
2. Due to some output offset voltage persent at the output of the OP-AMP, the voltage V_1 at the non-inverting (+) terminal is

nonzero and will have a value that depends on the output offset voltage and the values of resistance R_1 and R_2.

3. Hence the differential input voltage "V_d" is equal to the voltage V_1.

Time period and frequency of the output waveform :

1. The time period of the output waveform is given by,

$$T = 2RC \log_e \left[\frac{2R_1 + R_2}{R_2}\right] \quad ...(1)$$

2. We can substitute $\left[\frac{2R_1 + R_2}{R_2}\right] = \left[\frac{1+\beta}{1-\beta}\right]$ to get,

$$\boldsymbol{R = 2RC \log_e \left[\frac{1+\beta}{1-\beta}\right]} \quad ...(2)$$

3. This shows that the time period of the output waveform can be changed by changing either the values of R and C components or by varying the value of β. Hence a variable resistance R_2 in the circuit diagram for the astable multivibrator will actually change T and hence the output frequency f_0.

4. The expression for output frequency is given by,

$$f_0 = \frac{1}{T} = \frac{1}{2\ RC \log_e [(2R_1 + R_2)/R_2]} \quad ...(3)$$

5. If we substitute $R_2 = 1.16\ R_1$ then the above equation becomes,

$$f_0 = \frac{1}{2\ RC} \quad ...(4)$$

(c) Give the functional block diagram of timer IC 555 and explain how it can be used to obtain a Monostable Multivibrator.

Ans.

1. Before we learn how to use the timer IC 555, we must know its functional block diagram which is being shown in fig.
2. The timmer IC consists of two comparators a resistive voltage divider which generates the required, reference voltages for the two comparators the SR flip-flop, an output buffer and a discharge transistor T_1 as shown in Fig.
3. The pin connection diagram of the IC is as shown in Fig. (a) which shows the 8 pin dial in line package (D.P.) for the timmer IC 555.
4. Monostable multivibrator using 555 timers
5. The monostable multivibrator has only one pernmanetly stable state and one quasi-stable state.'
6. For a monostable circuit we require an external triggening signal to induce a transition of its output from the stable state to the quasi stable state.

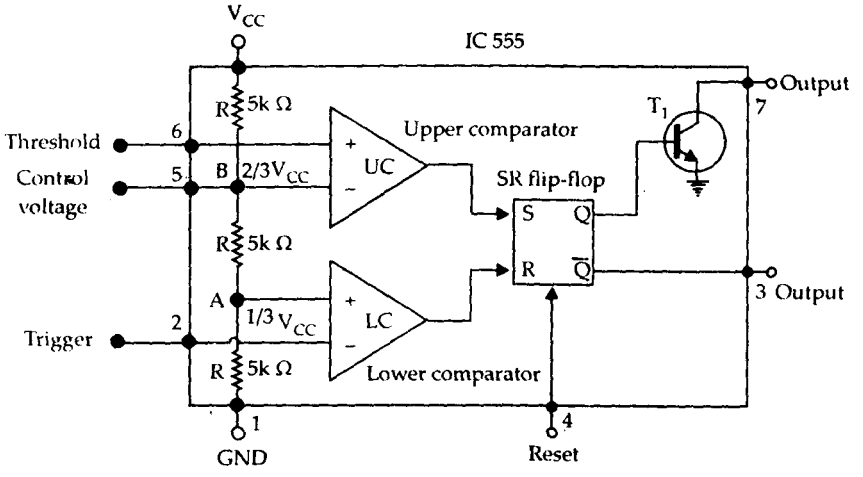


Fig. (a) : Functional block diagram of IC 555

7. The circuit remains in the quasi stable state for some time and eventually returns to its stable state on its own.
8. The circuit configuration for a monostable multivibrator using IC 555 is as shown in Fig. (b)
9. This is called as monostable multivibrator because the output has only one stable state. R_A and C are the externally connected components.

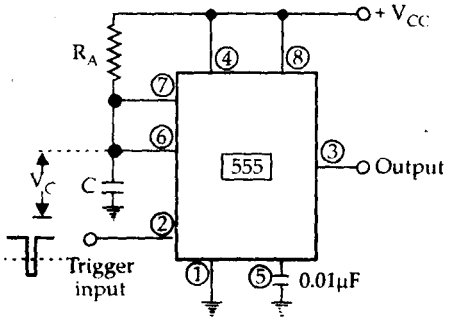


Fig.(b) : Monostable multivibrator using timer IC 555

10. The threshold (6) and discharge (7) pins are connected to each other.
11. The trigger pulse is applied to the trigger input (2) pin of the timer IC. Whenever voltage at pin (2) goes below 1/3 V_{CC}, the output goes high.
12. This circuit does not show the internal diagram of IC 555, but it shows only the external components to be connected.
13. Pin no. 4 is the "Reset" pin and it is made inactive by connecting it to V_{CC}.

14. A capacitor of 0.01 μF is connected from pin no. 5 (control voltage) to ground in order to filter out any noise coupled there.

(d) Distinguish between A/D and D/A converters. Explain the operation of any one of them.

Ans. Binary Ladders (R-2R Ladder Network) :

1. **This is the second type of resistive network used for the D to A conversion.**
2. Fig shows the basic R-2R ladder network. It consists of resistors of only tow values. R and 2R.
3. This will simplify the network and also the selection of network components.

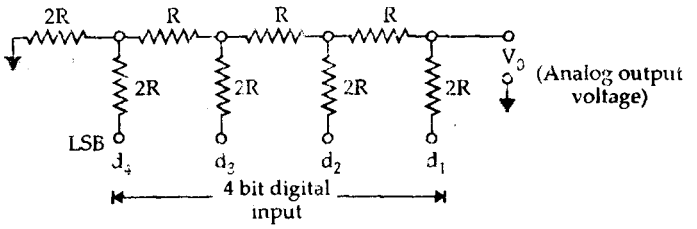


Fig. (a) : 4 bit R-2R ladder network

4. The R-2R network is the heart of R-2R ladder type DAC and the one shown in fig.(a) is a 4 bit R-2R network.
5. It is possible to have a 2 bit, 3 bit, 5 bit or n bit R-2R ladder.
6. d_1, d_2 d_3 d_4 is a 4 bit digital input word with d_1 as the most significant bit (MSB) and d_4 as the least significant bit (LSB)
7. V_0 is the analog output voltage which is proportional to the digital input.

(e) Give the circuit diagram of a sample and hold circuit and explain its operation.

Ans. For accurate analog to digital conversion, the analog input voltage must be kept constant during the convrsions process (cycle). If the analog input voltage changes by more than ± 1/2 LSB, an error can occur in the digital output code. The effect of a changing analog input voltage on the conversion process, let us consider a situation of a successive approximation ADC with an analog input voltage

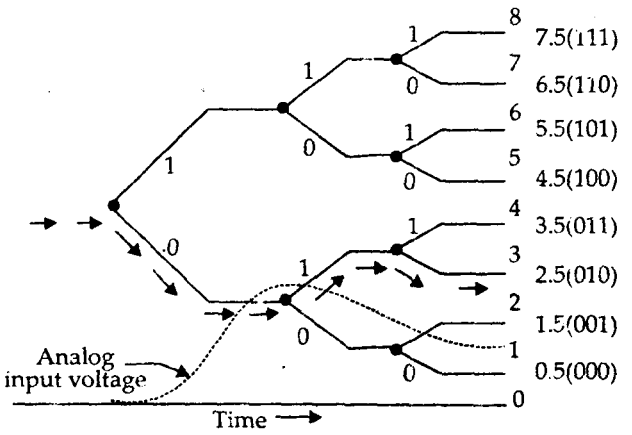


Fig. : Effect of changing input voltage

which is initially set at zero. There happens to be a large change in voltage amplitude that occur during the conversion process. Fig. shows the changing input voltage and its effect on the successive approximation conversion process.

As shown in figure, analog input voltage at start of conversion process is zero volts and at the end of

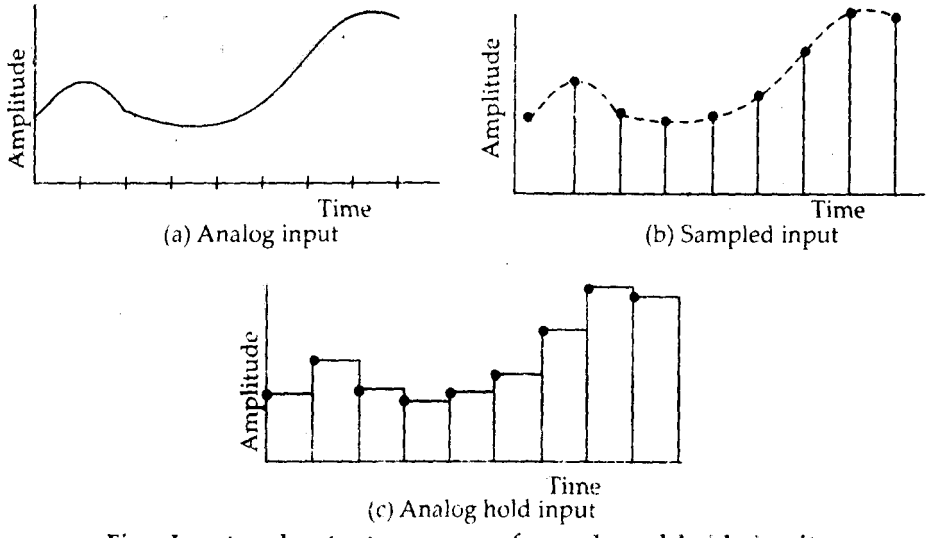


Fig : Input and output response of sample and hold circuit.

conversion process, it is close to 1.5 volts, and the conversion process result is 010_2, *i.e.*, 2.5 V. This result does not corresponds to the analog voltage at the start of conversion or at the end of conversion. To minimise the occurence of these errors, it is necessary to hold the value of the analog input voltage constant during the conversion process. The sample and hold circuit does this task.

As its name implies, the sample and hold (S/H) circuit sample the value of the input signal in response to a sampling command and hold it at the output until arrival of the next command. It samples an analog input voltage in a very short period, generally in the range of 1 to 10 μs and holds the sampled voltage level for an extended period.

Which can range from a few milisecond to several seconds. Fig. shows input and output response of the sample and hold circuit. The sample and hold circuit uses two basic components analog switch and capacitor. Figure shows the basic sample and hold circuit.

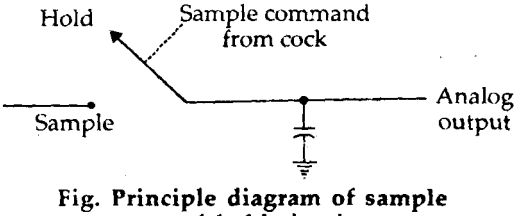


Fig. Principle diagram of sample and hold circuit

The circuit tracks the analog signal until the sample commond causes the digital switch to isolate the capacitor from the signal, and the capacitor holds this analog voltage during AD conversion.

(f) Explain the procedure for obtaining a 32×4 memory using 16×4 memory chips. Also show the necessary circuit diagram.

Ans. Step 1 : Number of memory chips :

- To obtain a memory of capacity in words using memory chips with M words each, the number of chips required is given by

  $X \geq m/M$

  Where X is an integer

- In the example, m = 32 and M = 16

  $\therefore X = 2$ *i.e.* 2 chips of capacity 16 × 4 are required.

Step 2 : Connection :

The two 16 × 4 chips are connected in the following manner :

1. The address lines are connected to the address lines of two chips individually. That means out of the 5 address lines (we need 5 address lines) the 4 LSB lines A_3 A_2 A_1 A_0 will be same for each chip and the MSB line A_4 should be used to select chip-1 or chip-2

   with A_4 = 0 chip-1 should be selected

   with A_4 = 1 chip-2 should be selected

2. As the word size is same (4 bit), the data input/output lines of both the chips should be connected to each other.

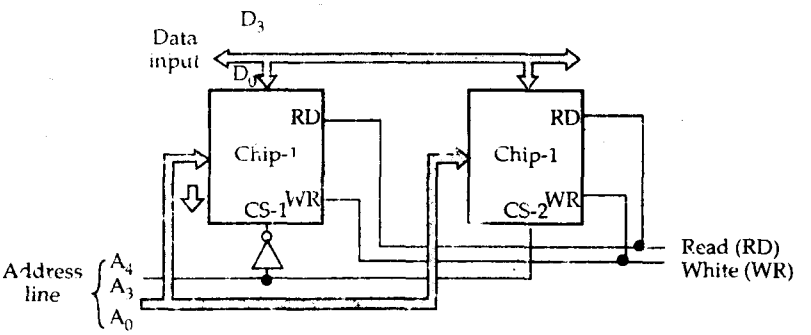


Fig. A 32 × 4 size memory obtained using two 16 × 4 memory chips

That means D_0 of chip-1 is connected to D_0 of chip-2 and the common D_0 line now acts as the D_0 line of the overall memory. Similarly the connections are made for D_1, D_2 and D_3 lines.

3. Connect the read input of each chip together and write inputs also together.
4. The connection diagram is shown in Fig.

- When $A_4 = 0$, the first chip is selected.So the first 16 locations can be accessed for $A_3 A_2 A_1 A_0 = 0000$ to 111.
- With $A_4 = 1$, first chip is disabled and second chip is selected For $A_3 A_2 A_1 A_0 = 0000$ to 1111 now the RD or WR operation can be performed on the 16 locations of chip-2