# UNIT 4
# Analog and Digital Electronics

## Sequential Circuit

## Asynchronous Counter

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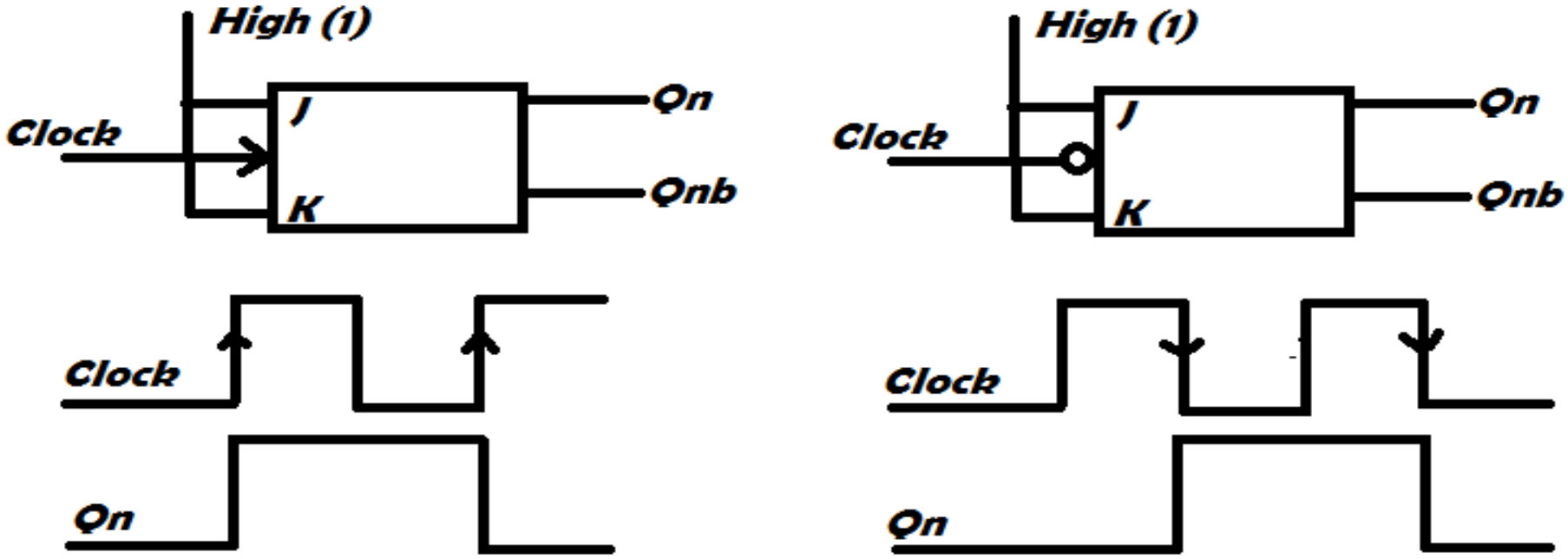
# Asynchronous counter

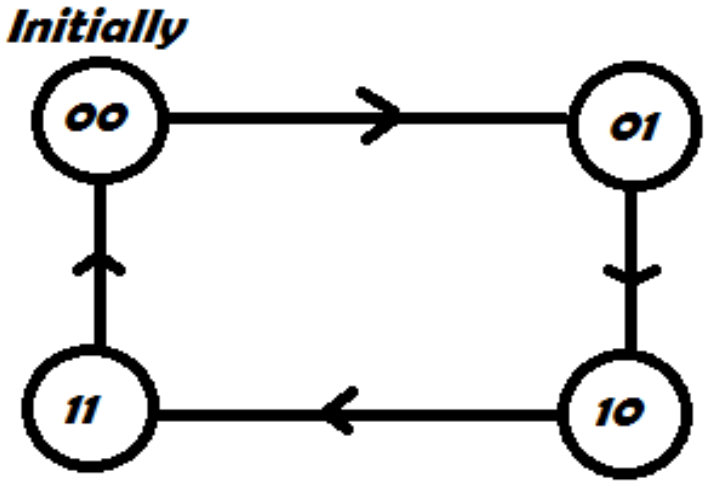
- Output of the first clock act as the clock for the next one.
- T flip-flop or the toggling behaviour of JK Flip is used. At J=K=1
- Counter can be Positive edge trigger or negative edge Trigger means it can change its state only at the edge of the clock.

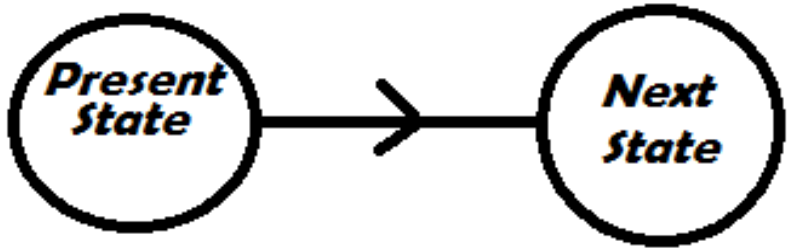


# Contd.

- An *n*-bit counter
- – has *n* Flip-Flops
- – can cycle through at most 2n
- Suppose a counter counts

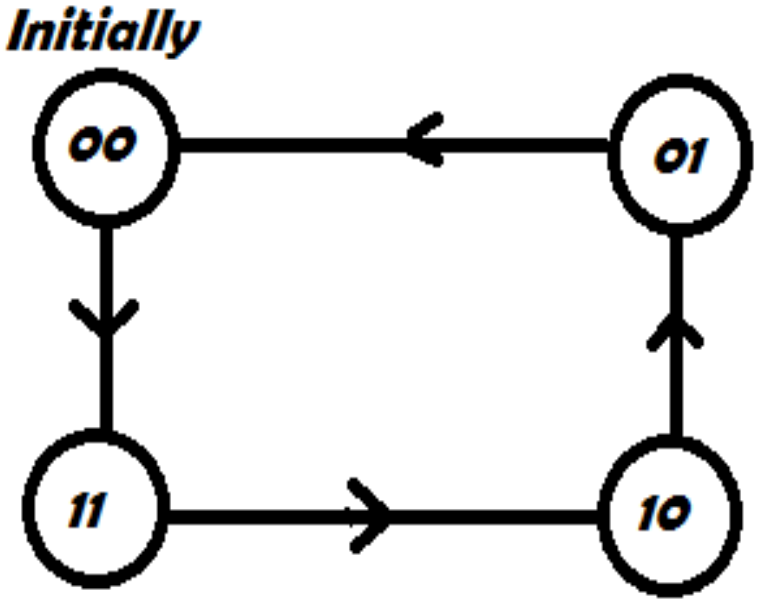
  0→1→2→3→0 (00→01→10→11→00) (Two bit & MOD 4 Counter and UP counter )



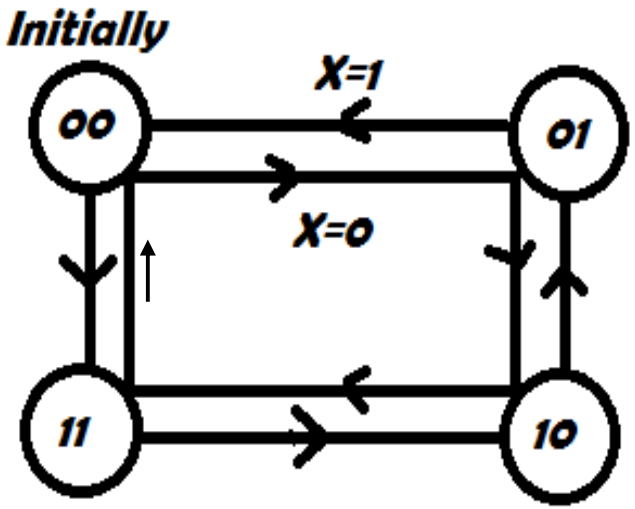



# Contd.

**Down Counter**



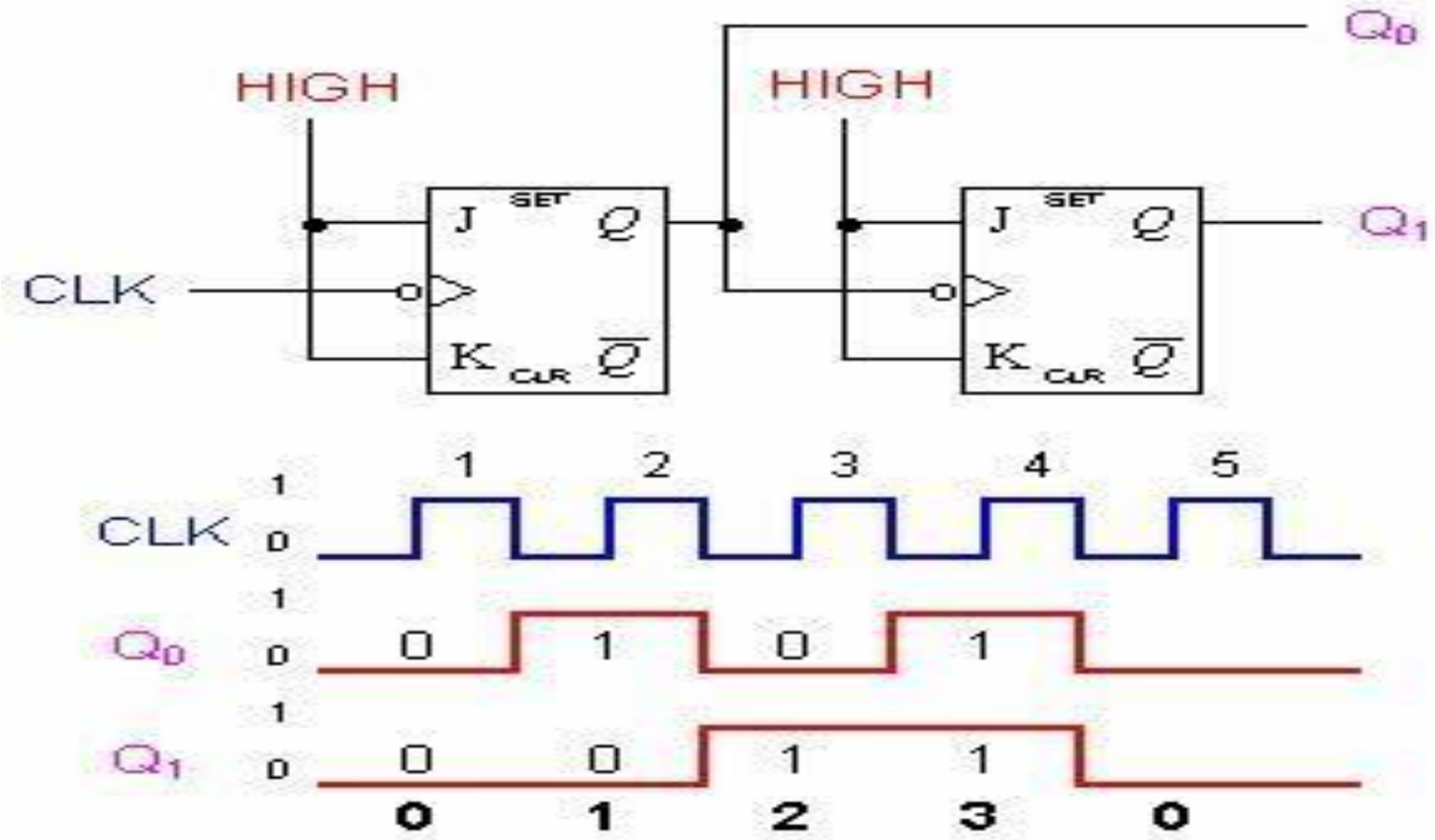

**UP and Down Counter**



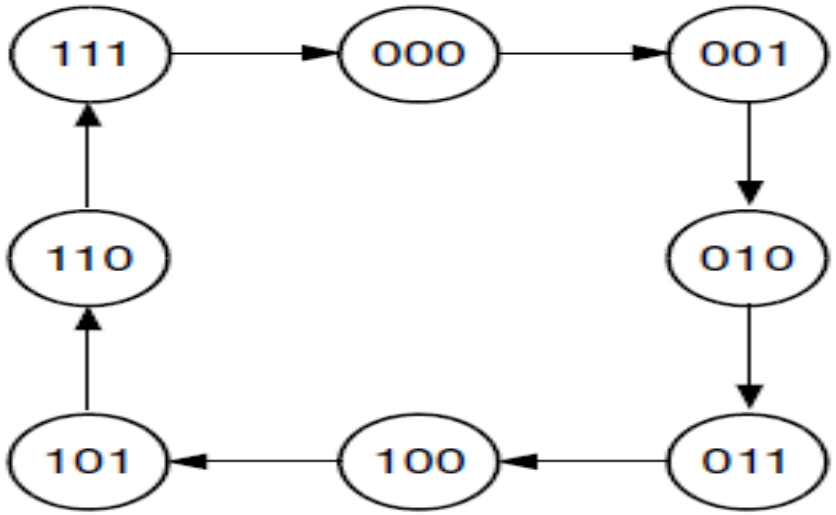

*If control input X=0 counter act as UP Counter*

*If the control input X=1 counter act as Down counter*

# Two bit Asynchronous Counter

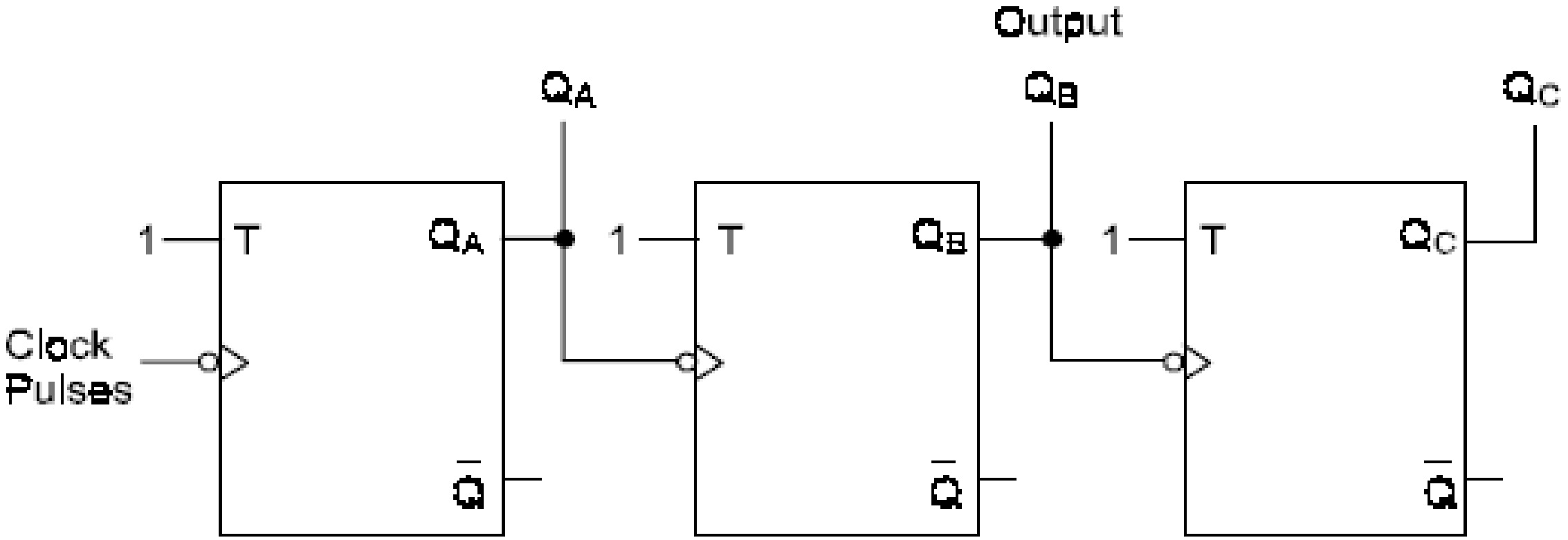


# Contd. 3 bit counter mod 8 counter Number of Flip flop require ??



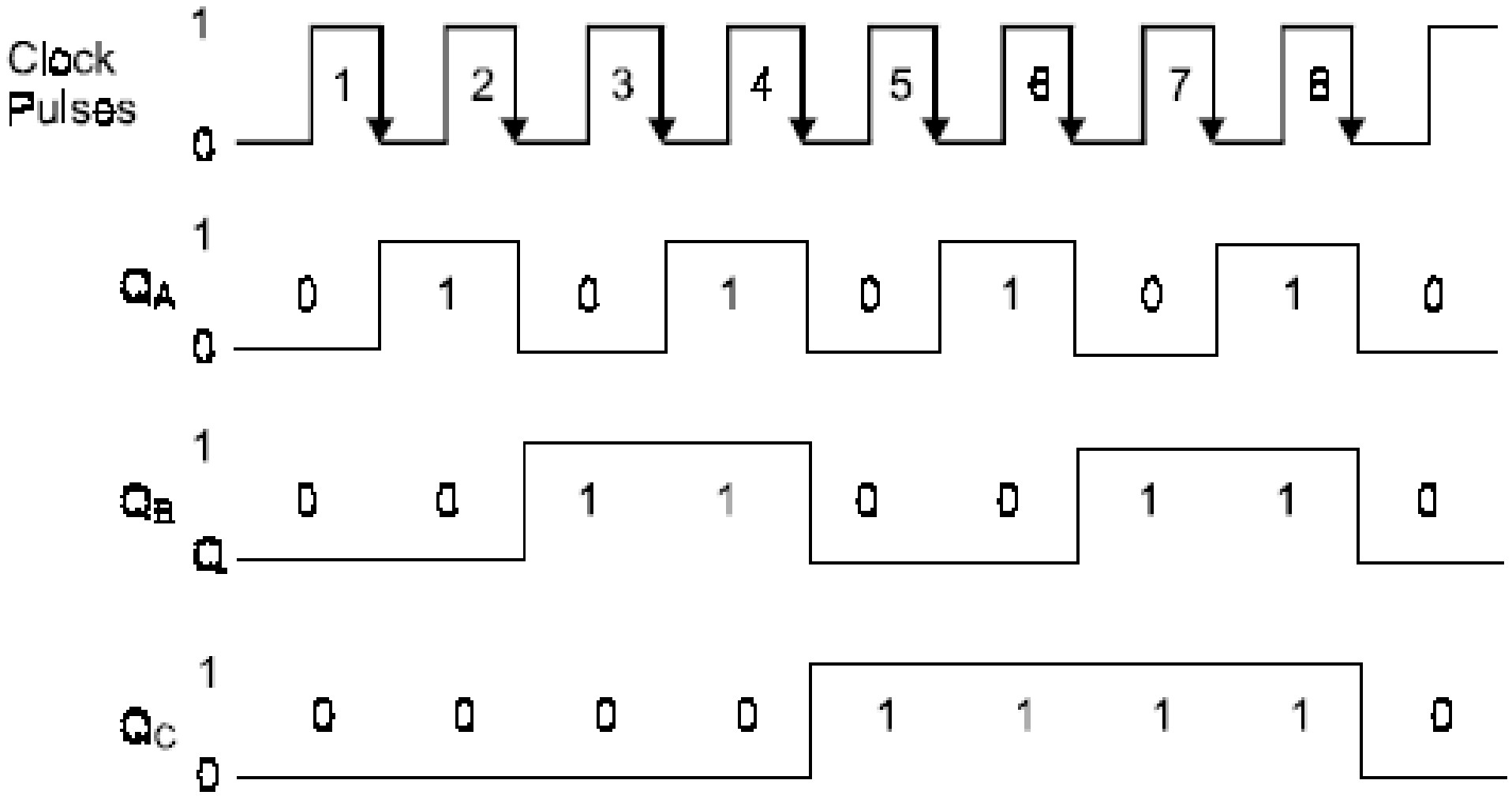

3-bit Counter

# *Three-bit asynchronous counter*

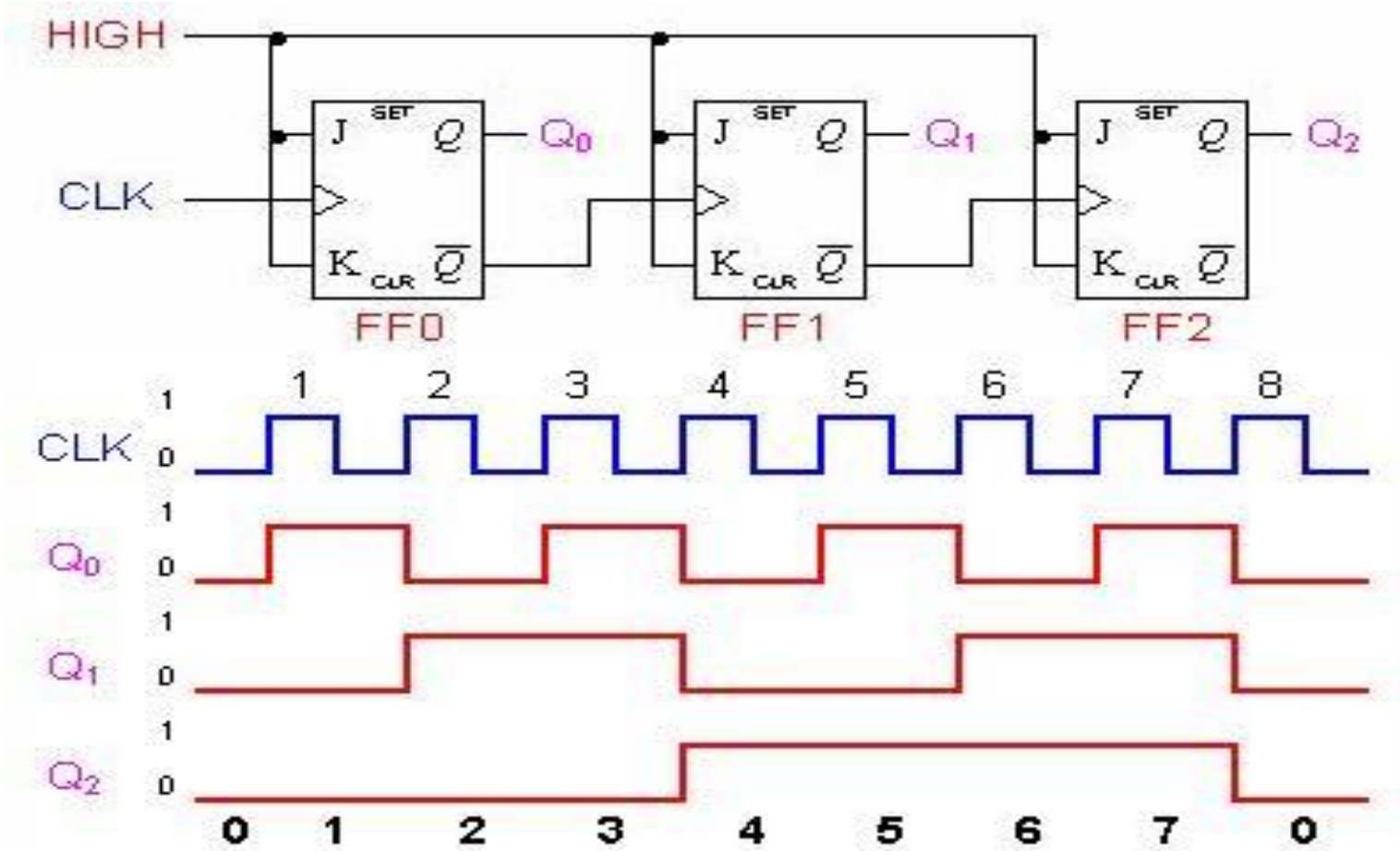



**UP counter**

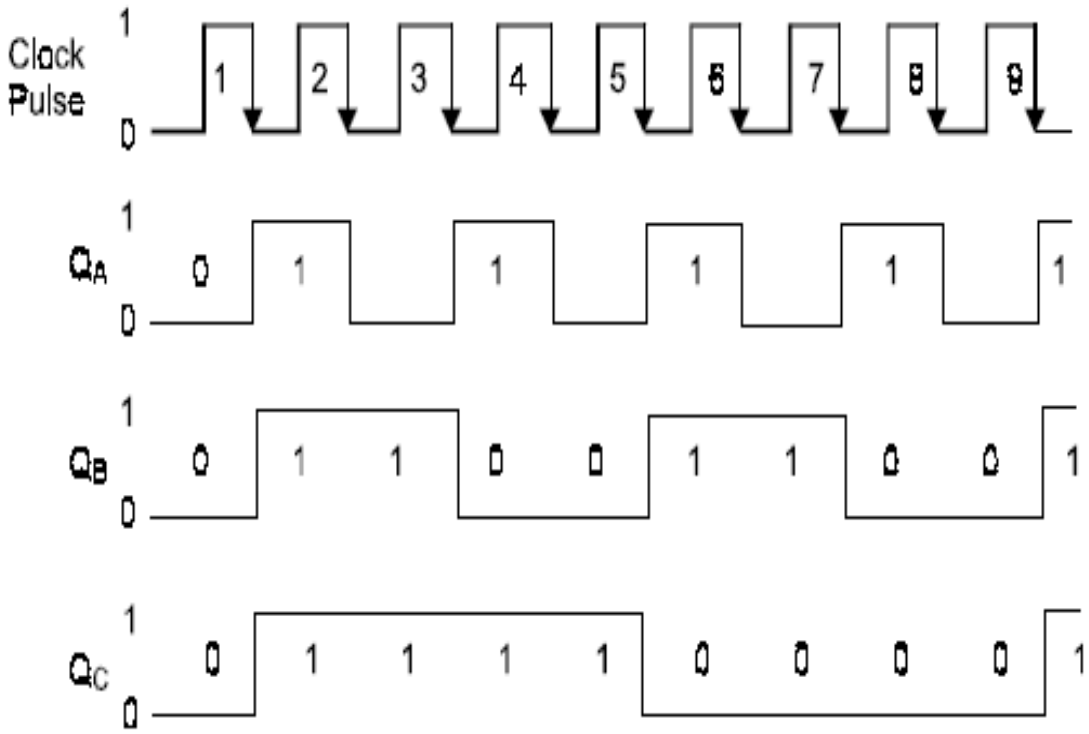
# UP Counter Output Wave Form

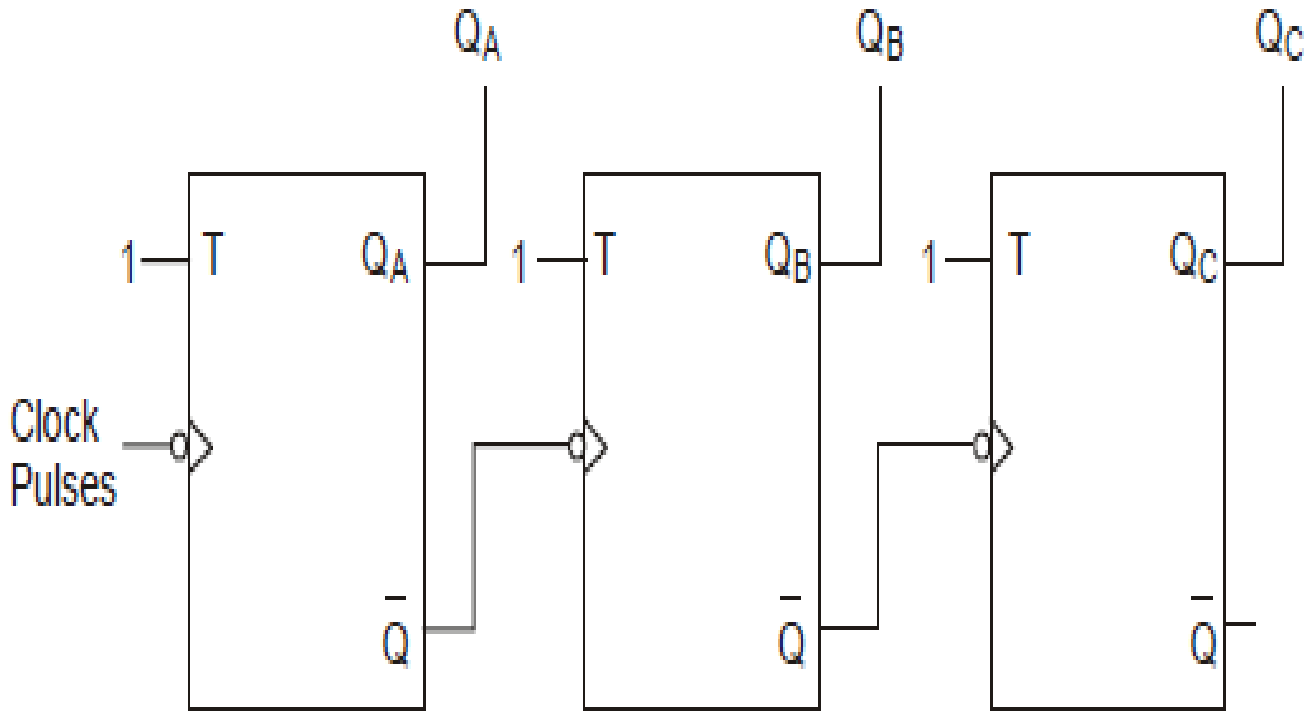


# *Three-bit asynchronous UP counter*

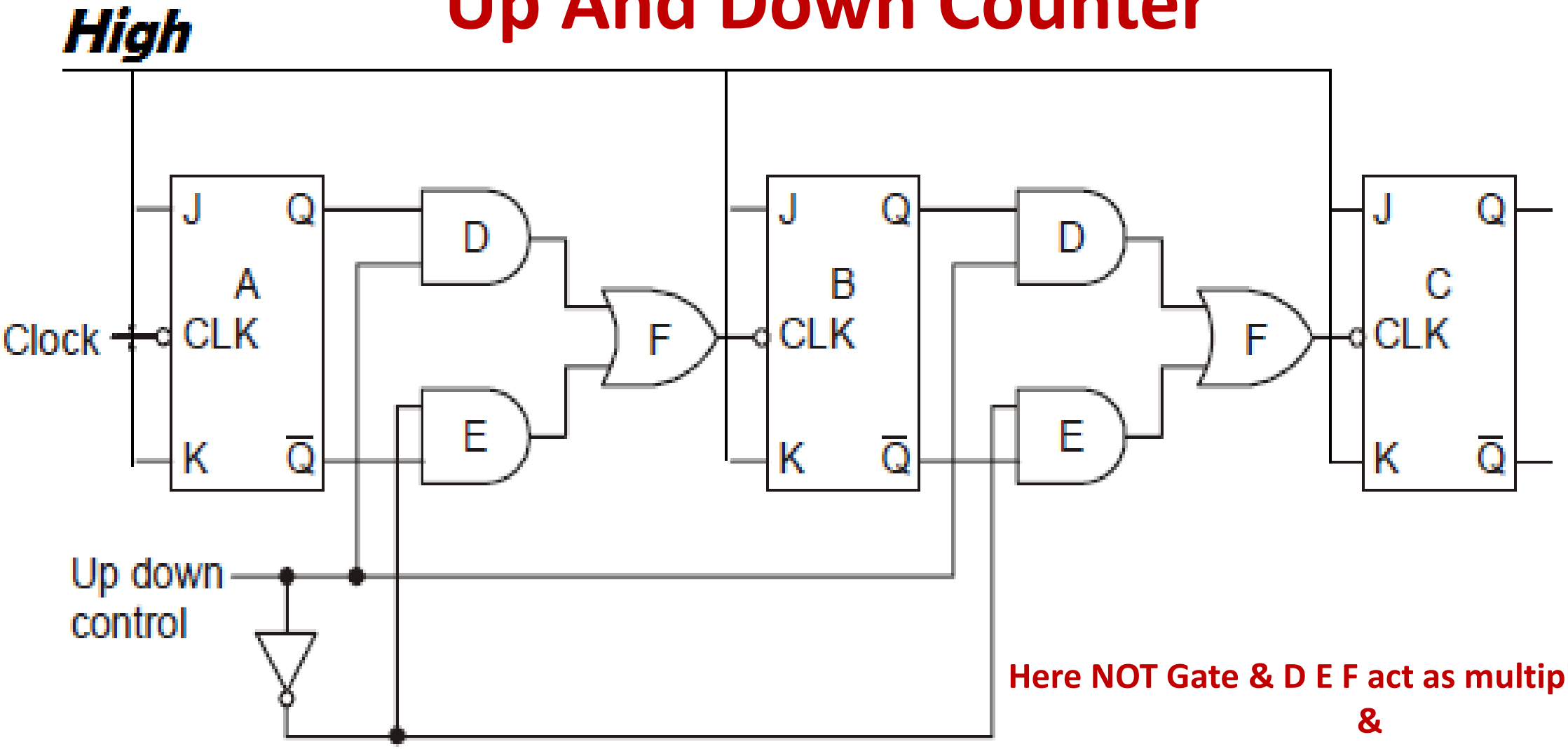


# THREE BIT Asynchronous Down COUNTER



# Up And Down Counter




**Here NOT Gate & D E F act as multiplexer (2:1).**

**&**

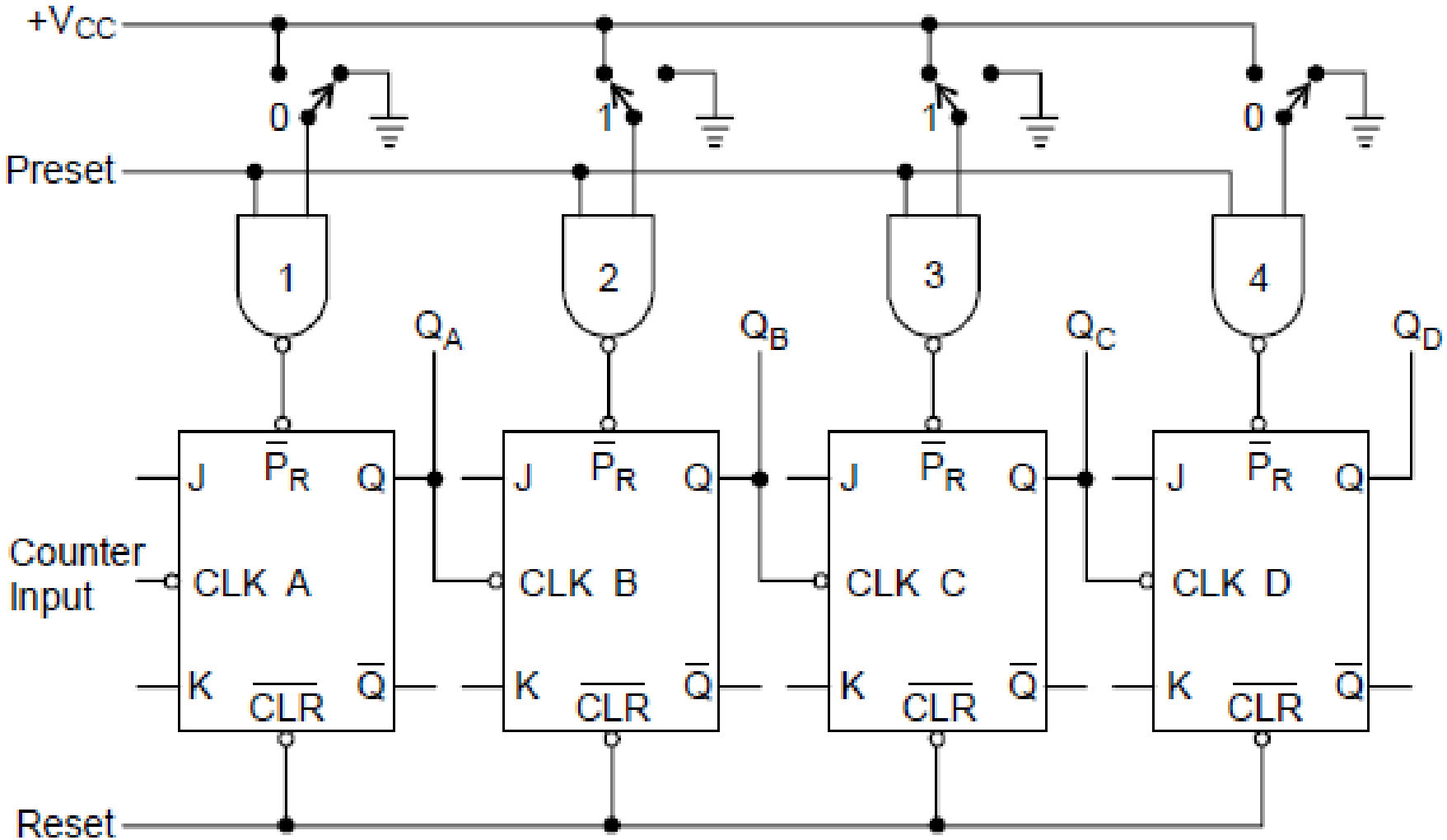
**Up down control act as selection line**

# Flip-Flop Pins

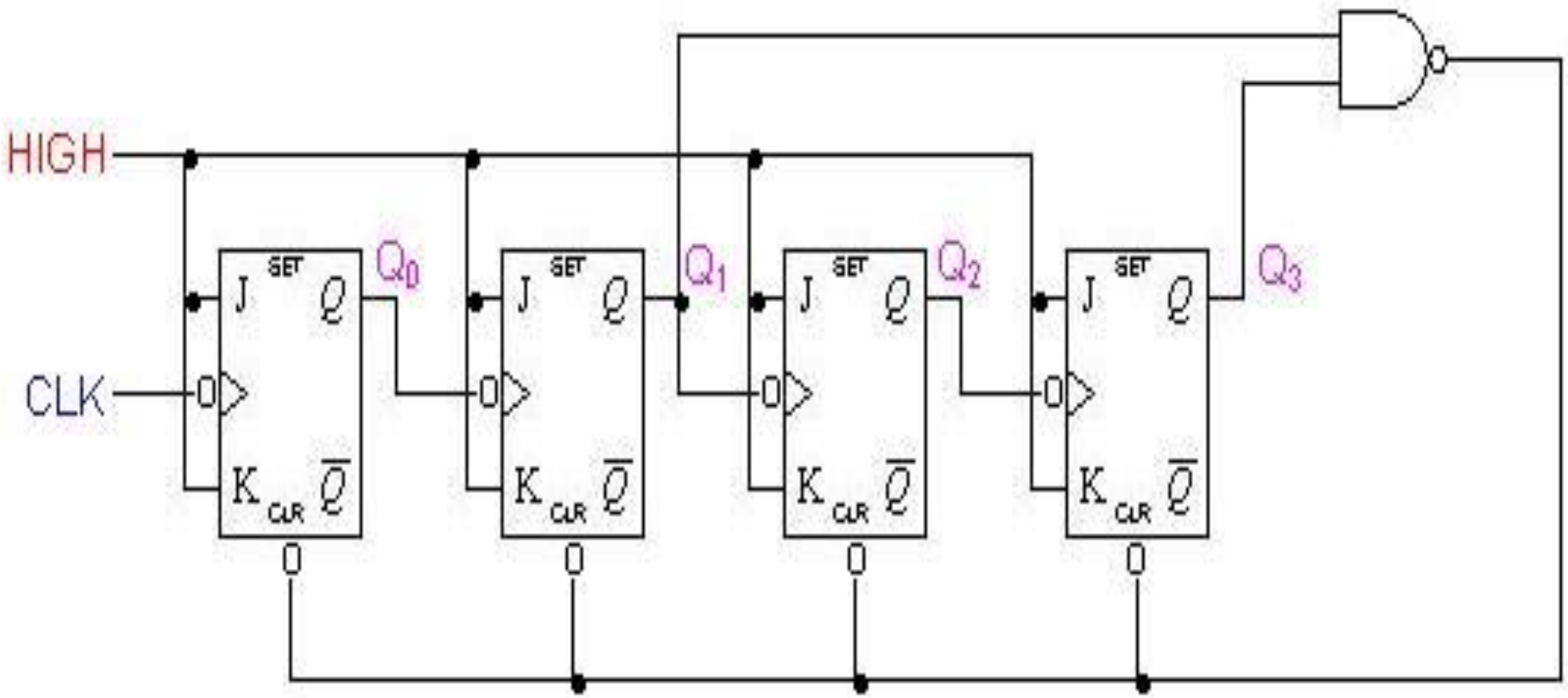
- Input Pin (like JK or T or D or SR)
- Clock Pin (+ve or -ve edge trigger )
- Reset pin /Clear Pin (Can Reset Low or High)
- Pre-set Pin

**With the help of Pre-set Pin we can force FF to set 1**
**With the help of Reset function to clear FF to 0**

# Pre-set and Reset Function



# *A Decade Counter (asynchronous counter)*



Design a 4 bit Up Down & Up/Down counter

# END

# NEXT Synchronous Counter