UNIT 4
Analog and Digital Electronics

Sequential Circuit

Latches and Flip-Flops

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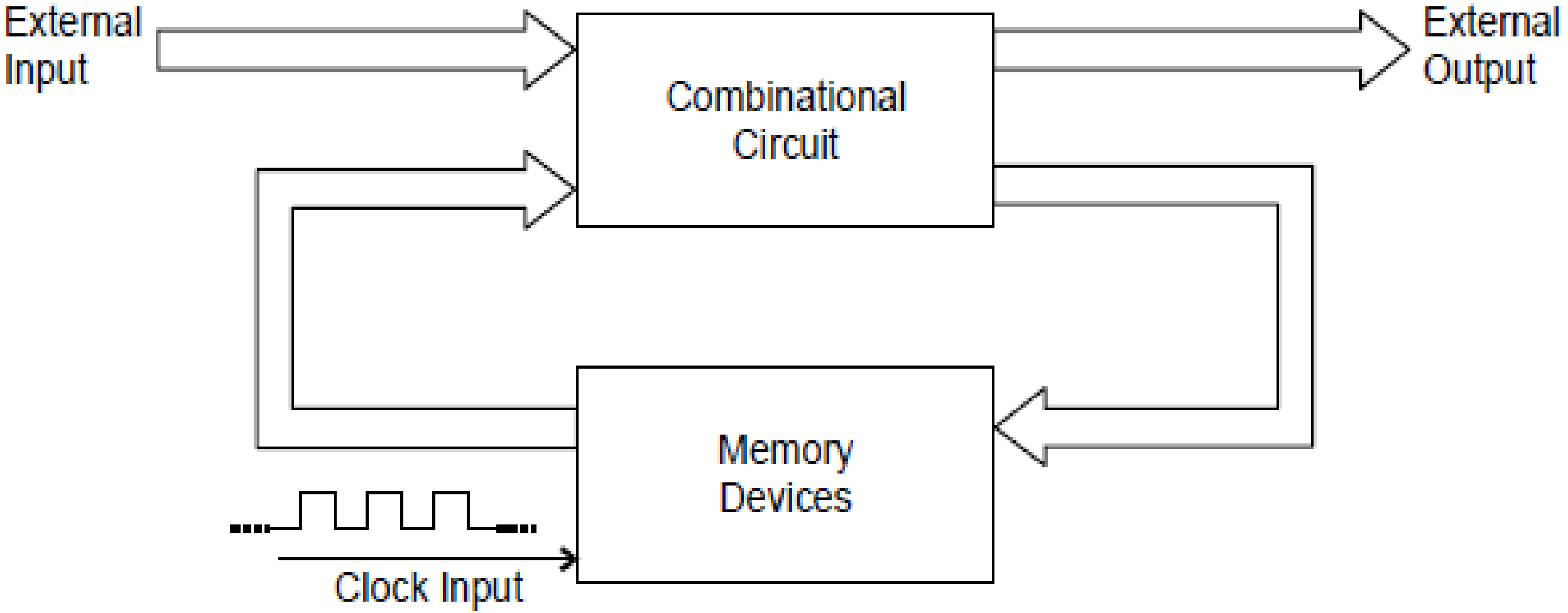
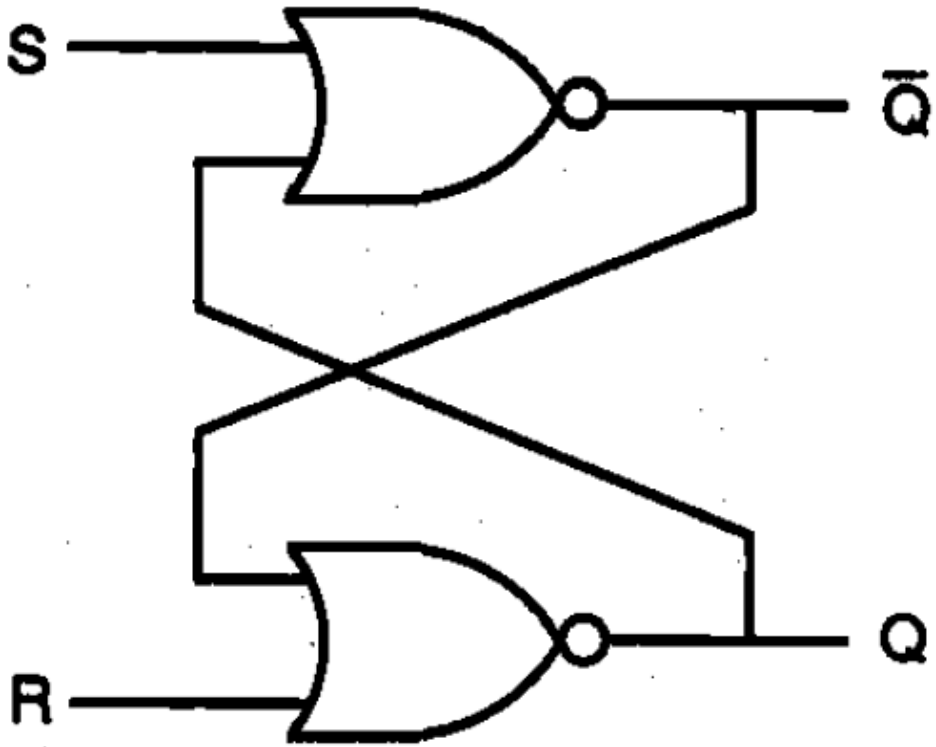
Sequential Circuit

Sequential circuit are those in which output at any given time not only dependent on the input, present at that time but also on previous output.

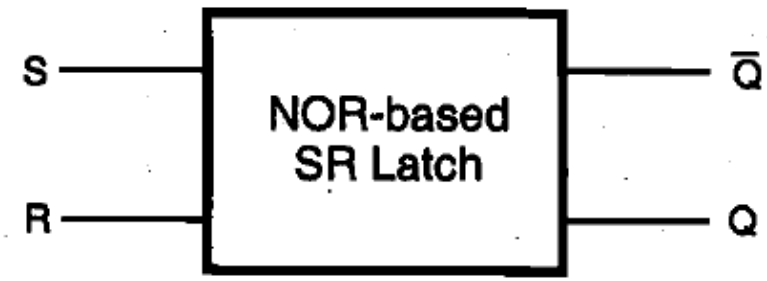


NOR Latch (Bistable state)

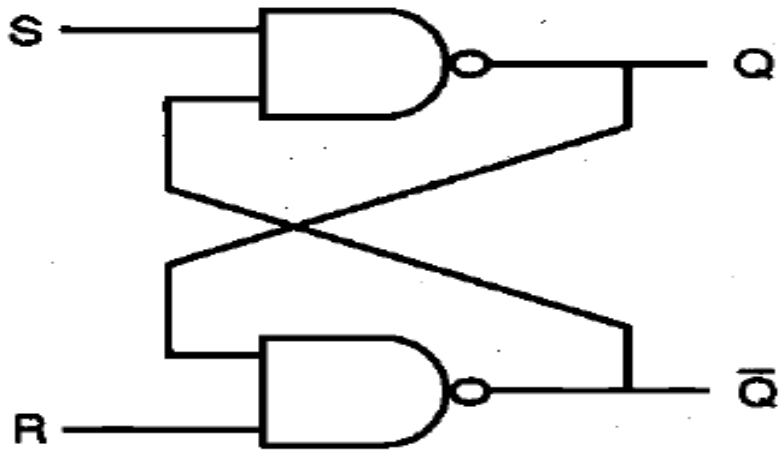
Nor gate if any one input is ‘1’ output will be ‘0’.



S	R	Q_{n+1}	$\overline{Q}_{n+1}$	Operation
0	0	Q_n	$\overline{Q}_n$	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

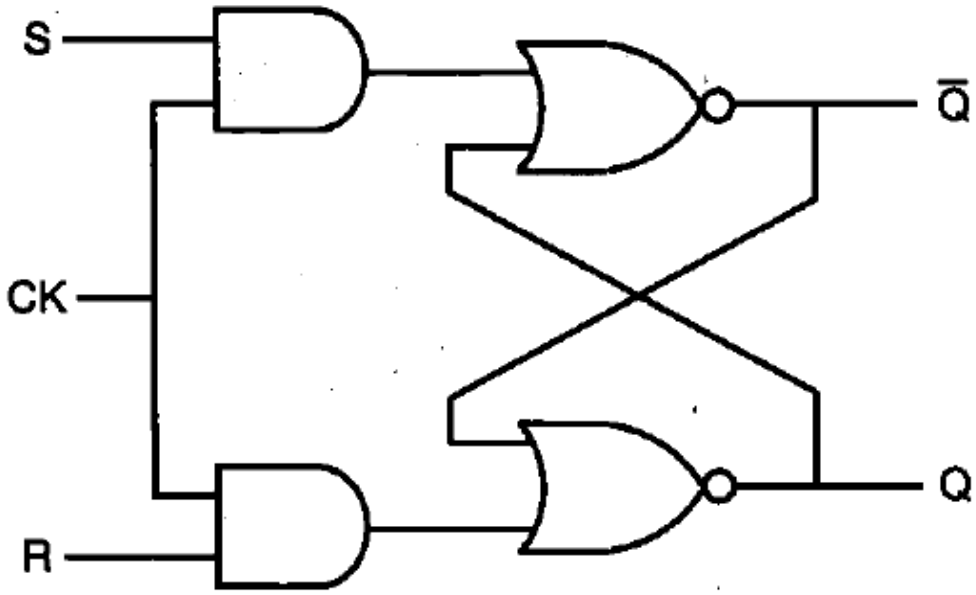


NAND Based SR latch
(In NAND gate if one input is ‘0’ output will be ‘1’.



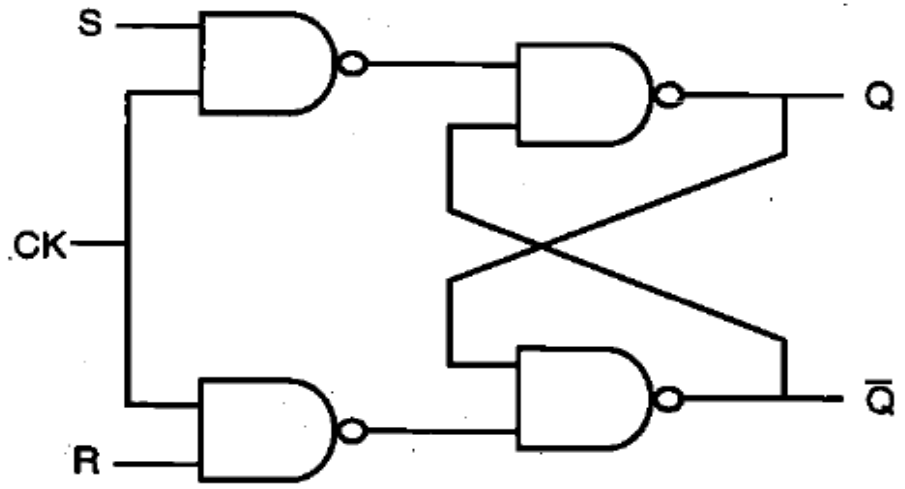
S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	1	1	not allowed
0	1	1	0	set
1	0	0	1	reset
1	1	Q_n	$\overline{Q_n}$	hold

Clocked SR Latch(Level Triggered) with active High



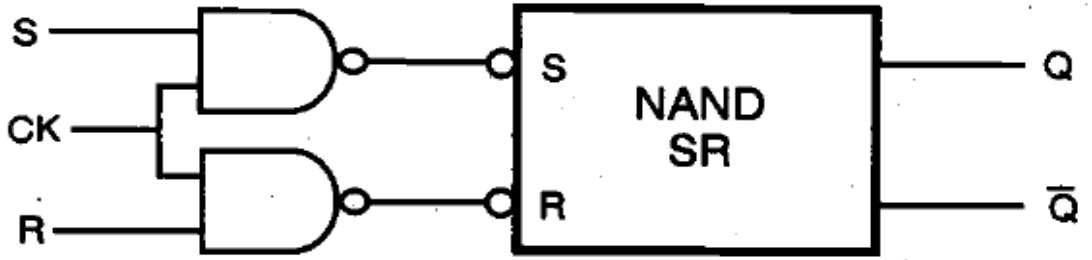
S	R	Qn	Qnb	Qn+1	Qn+1b	Comment
0	0	0	1	0	1	Qn (No change)
		1	0	1	0	
0	1	0	1	0	1	Reset
		1	0	0	1	
1	0	0	1	1	0	Set
		1	0	1	0	
1	1	0	1	0	0	indeterminate
		1	0	0	0	

Clocked NAND SR LATCH Active High

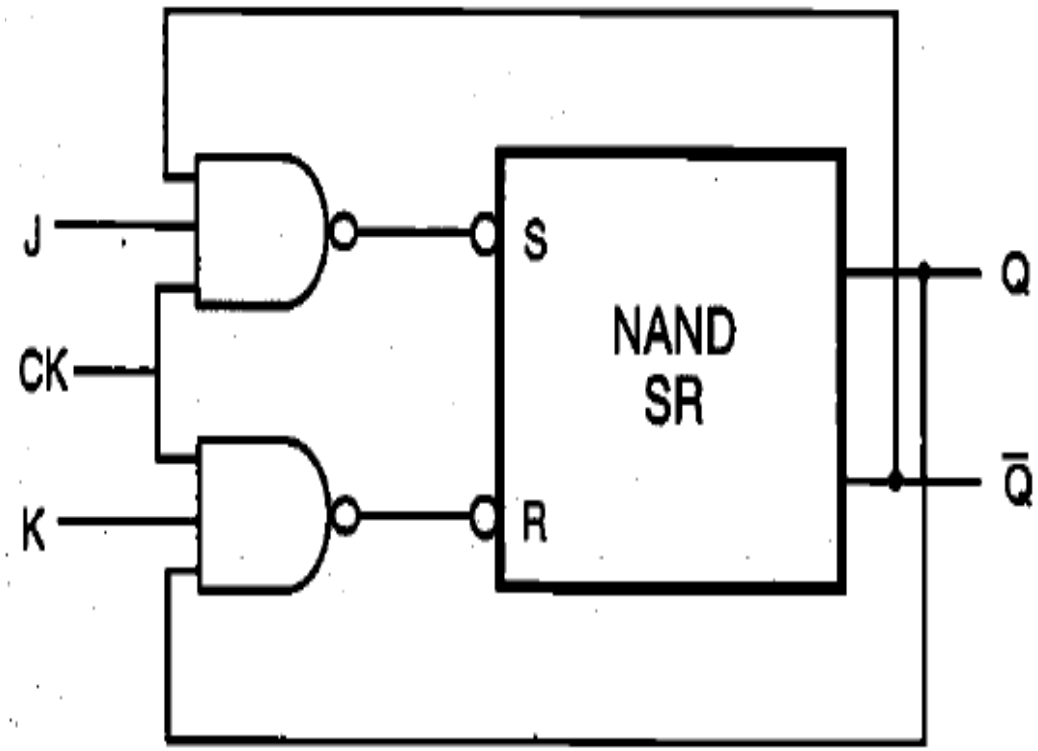


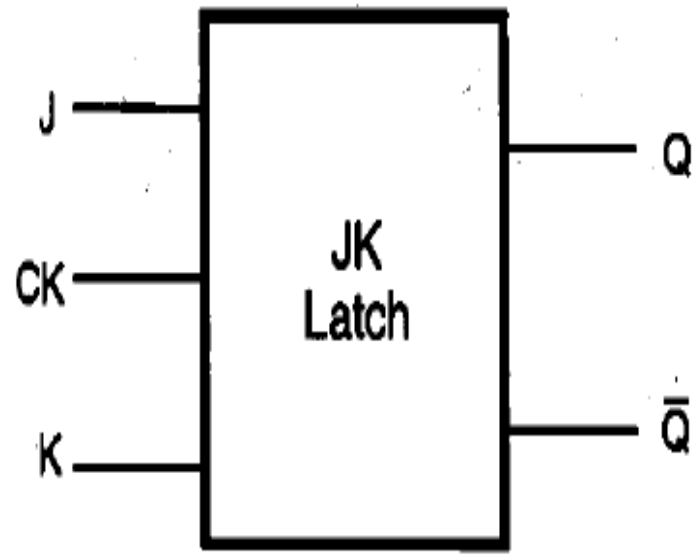
(a)

S	R	S'	R'	Qn	Qnb	Qn+1	Qn+1b	Comment
0	0	1	1	0	1	1	1	indeterminate
				1	0	1	1	
0	1	1	0	0	1	0	1	Reset
				1	0	0	1	
1	0	0	1	0	1	1	0	Set
				1	0	1	0	
1	1	0	0	0	1	0	1	Qn (No change)
				1	0	1	0	

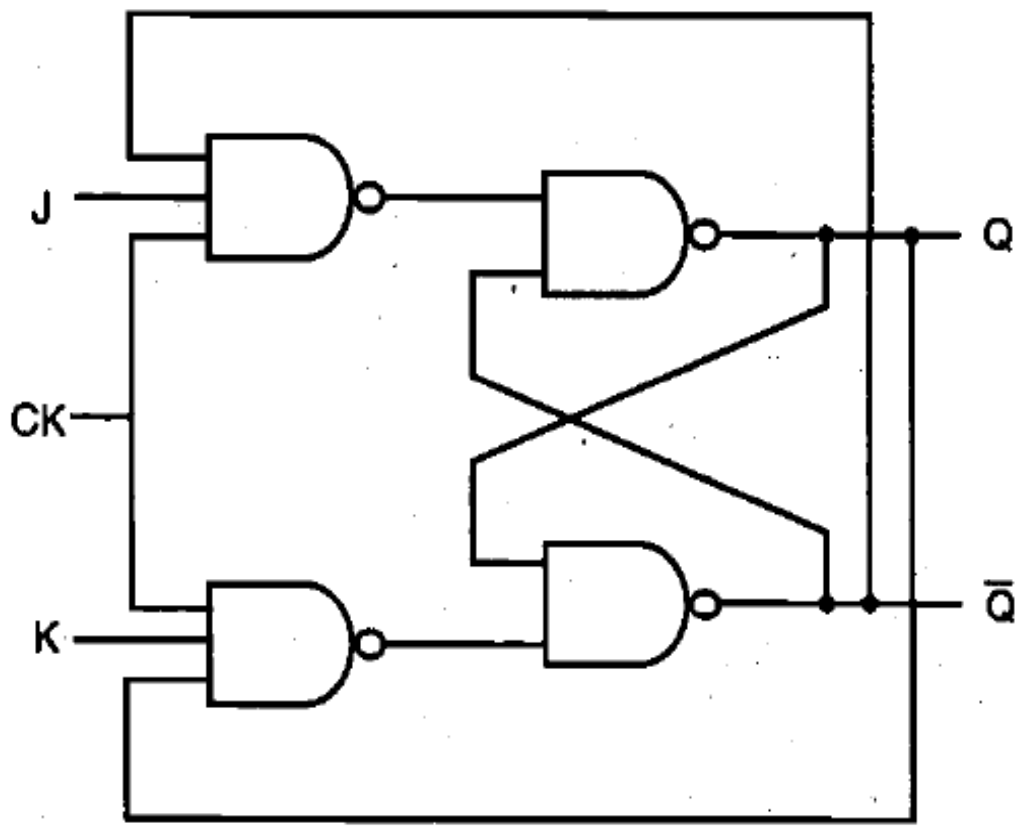


CLOCKED JK Latch NAND Based



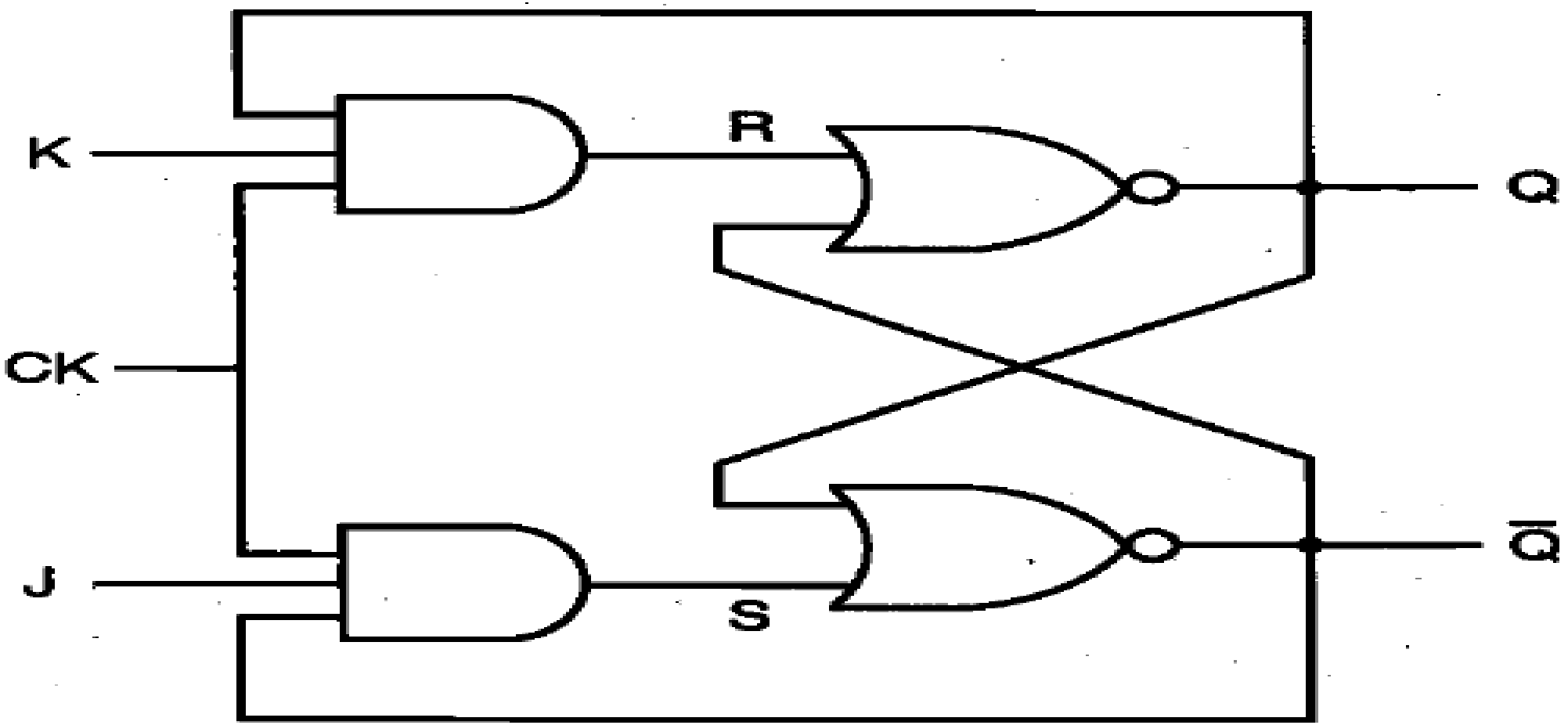


Truth Table

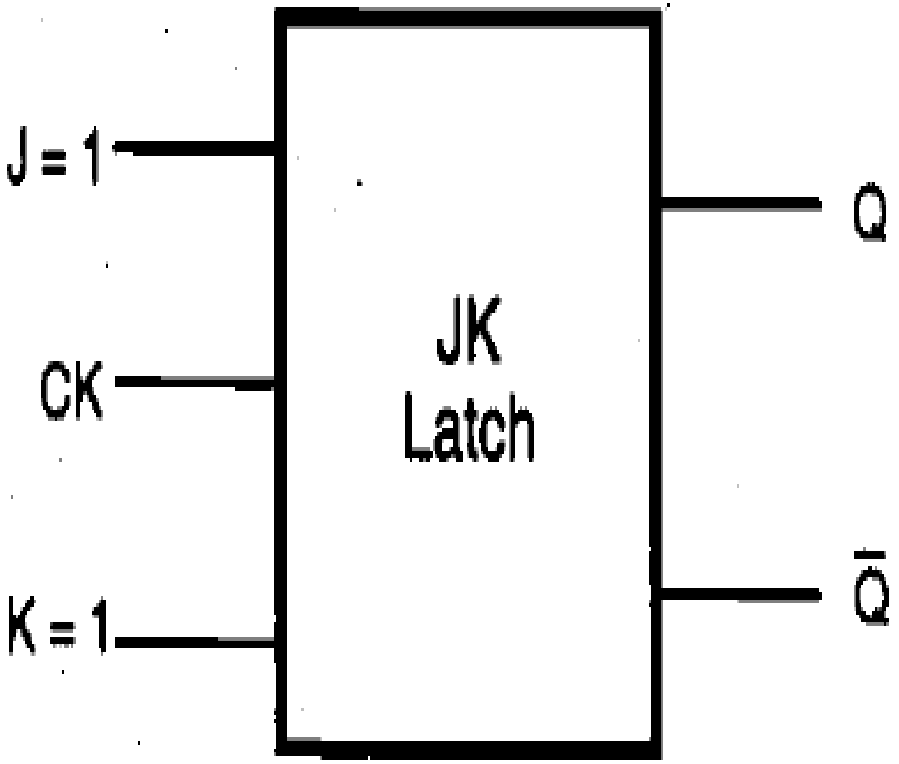


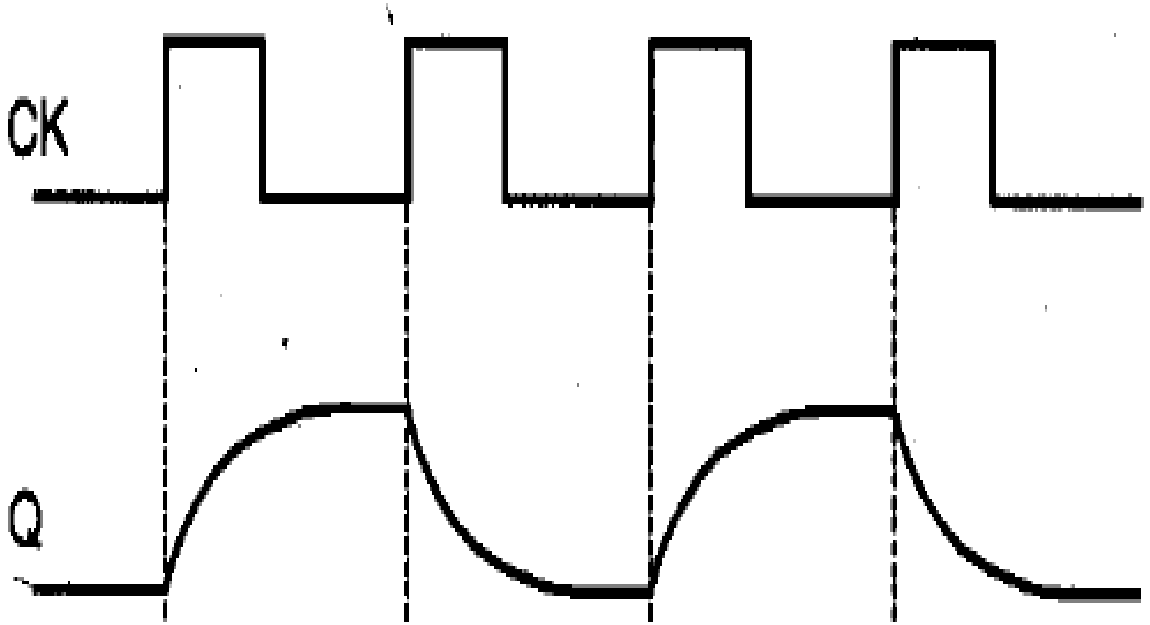
J	K	Q_n	$\overline{Q_n}$	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	*Operation*
0	0	0	1	1	1	0	1	*hold*
		1	0	1	1	1	0	
0	1	0	1	1	1	0	1	*reset*
		1	0	1	0	0	1	
1	0	0	1	0	1	1	0	*set*
		1	0	1	1	1	0	
1	1	0	1	0	1	1	0	*toggle*
		1	0	1	0	0	1	

JK LATCH NOR BASED



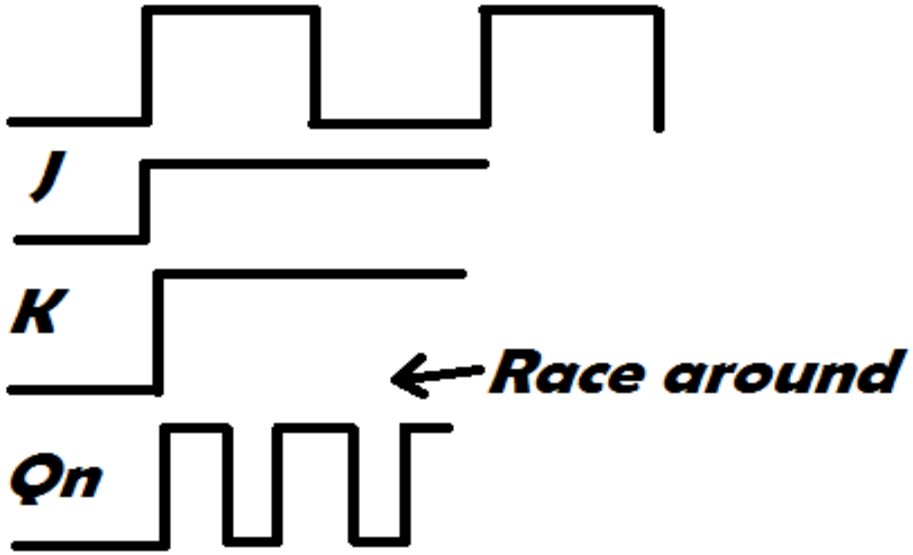
JK as a toggle Switch



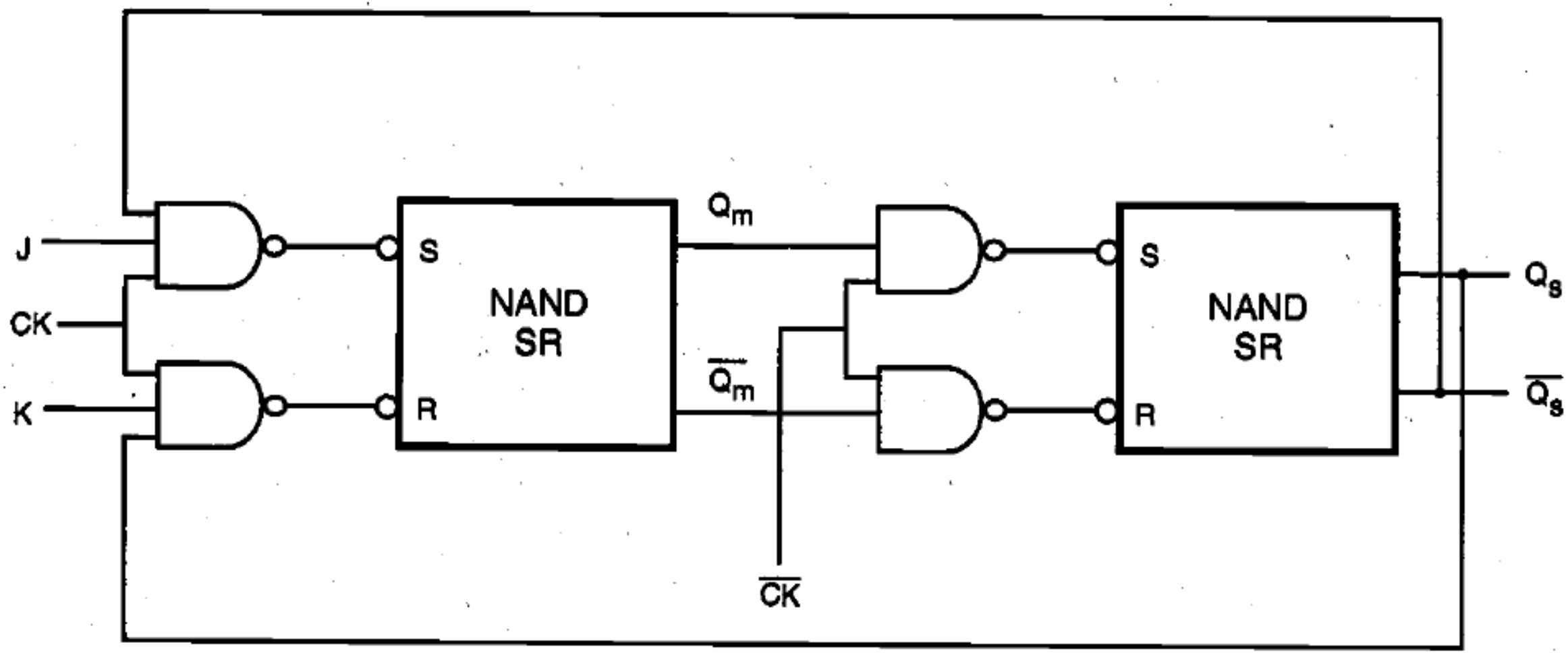


Master Slave JK FF

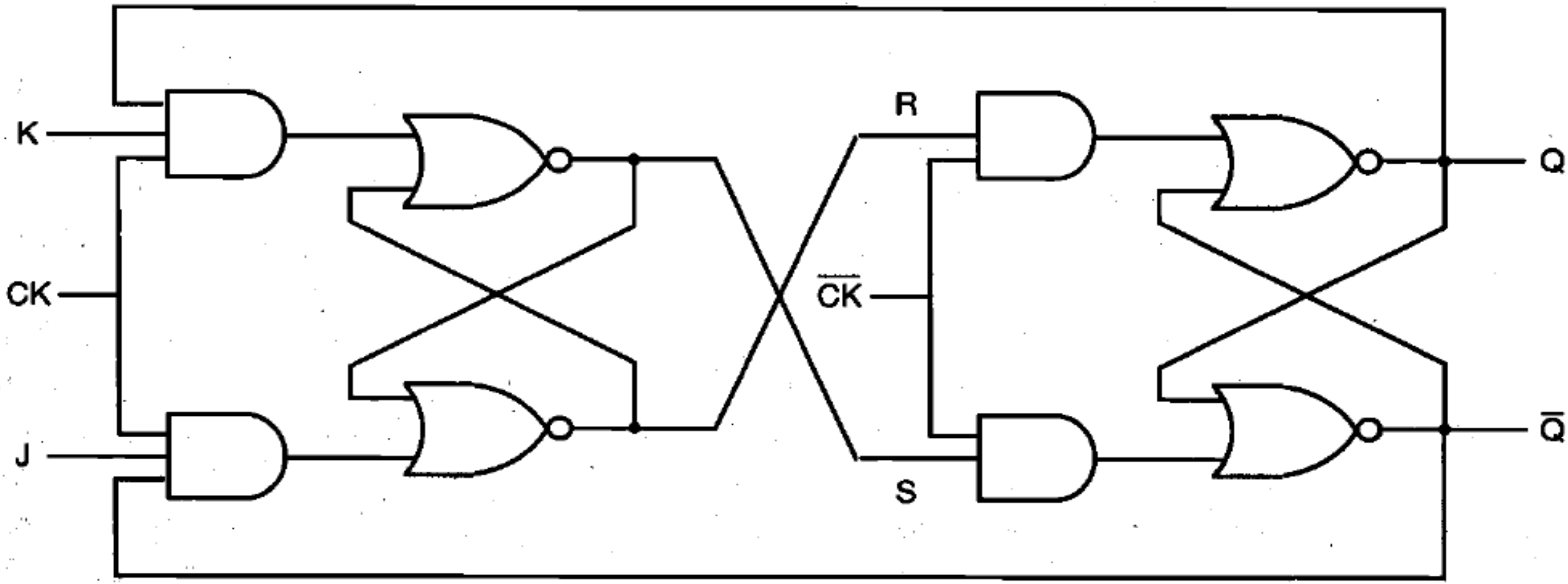
- When J=K=1 Toggle
- When the Clock pulse width is high, the output changes or toggle one or more in the same input J=K=1 the same clock period.
- This Problem is known as Race Around Condition.



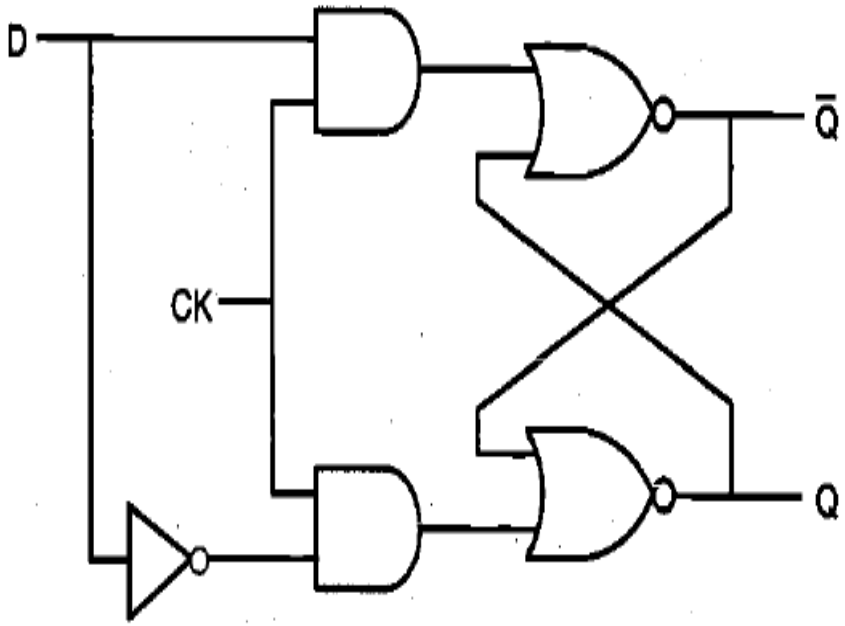
Master Slave JK FF NAND Based

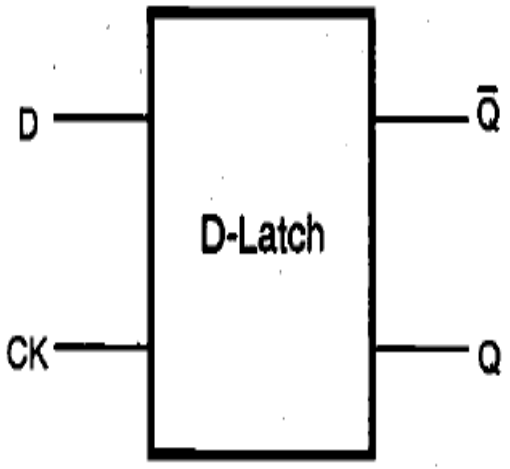


Master Slave JK FF NOR Based



D Latch

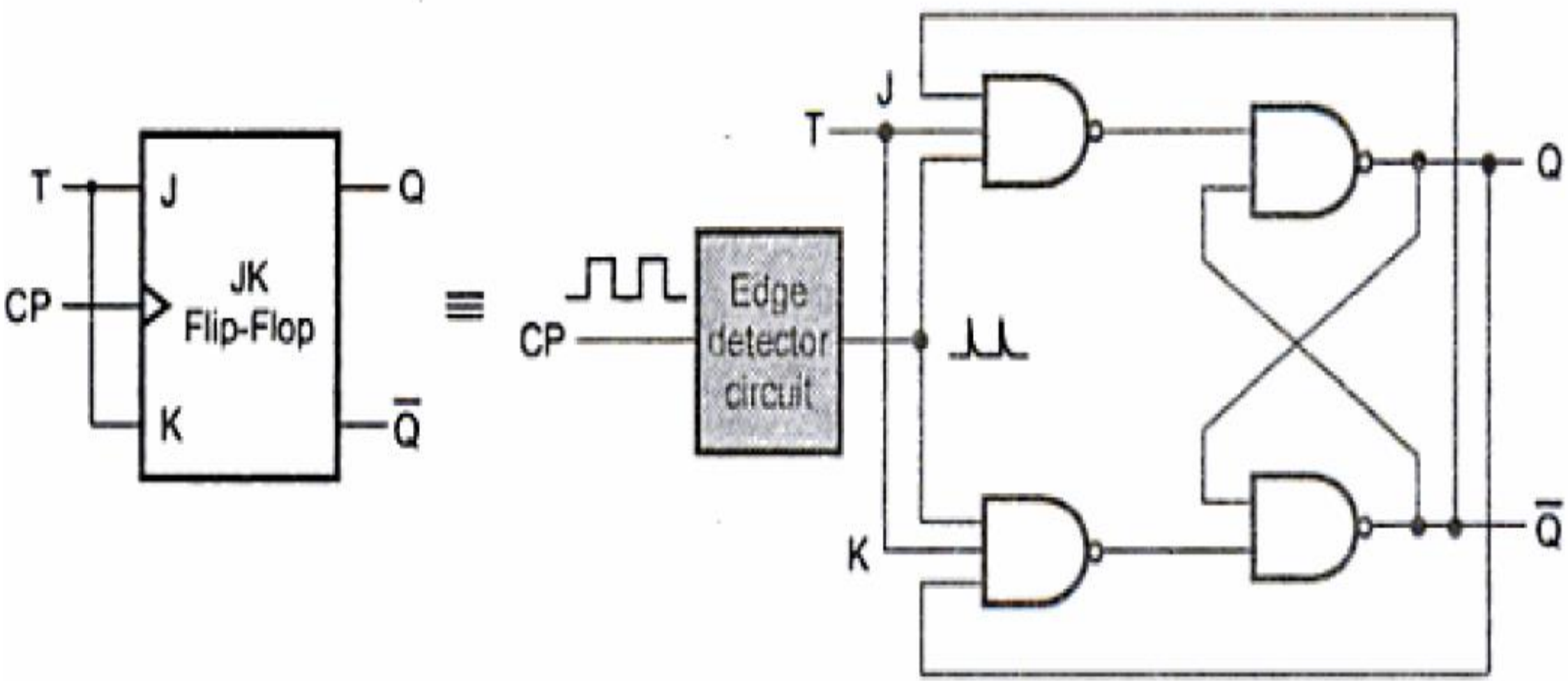




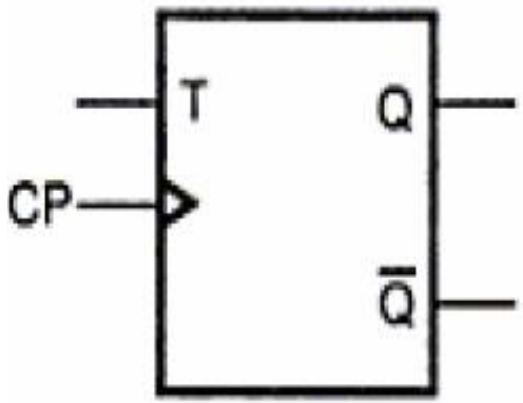
D	Qn+1
0	0
1	1

Qn+1=D

T FF T→ Toggle FF



T Flip-flop



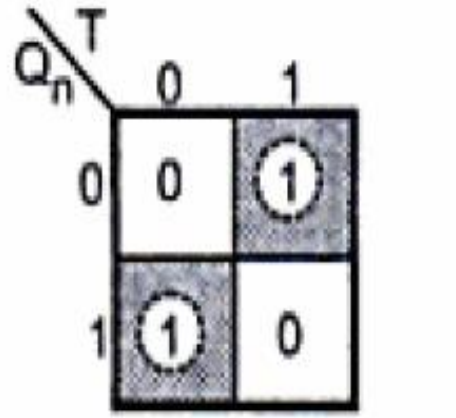
(a) Logic symbol

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

b) Truth table

≡

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$



$\therefore Q_{n+1} = T\overline{Q}_n + \overline{T}Q_n$

(c) Characteristic equation

RS FF Truth Table & Excitation Table

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	*

Table 6.5 (a) RS Truth table

Q_n	Q_{n+1}	R	S
0	0	X	0
0	1	0	1
1	0	1	0
1	1	0	X

Table 6.5 (b) RS Excitation table

Find Q_{n+1} Expression

JK FF Truth & Excitation Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Table 6.6 (a) JK truth table

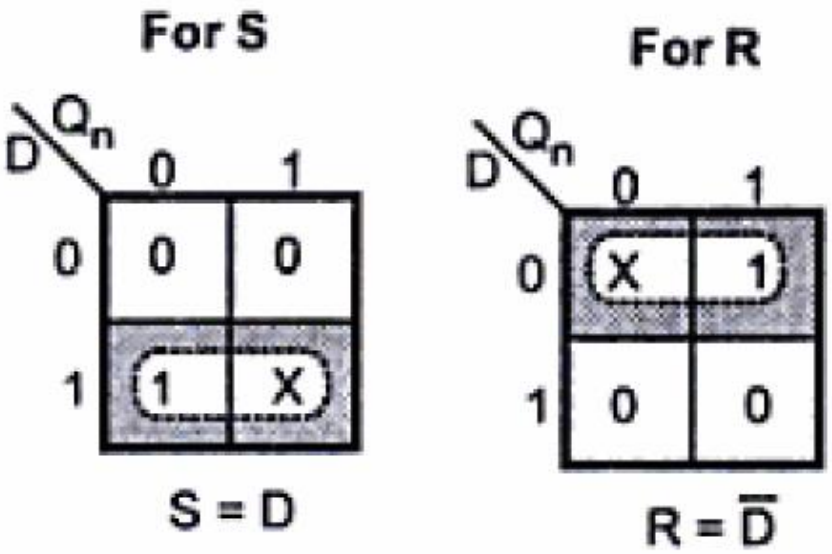
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

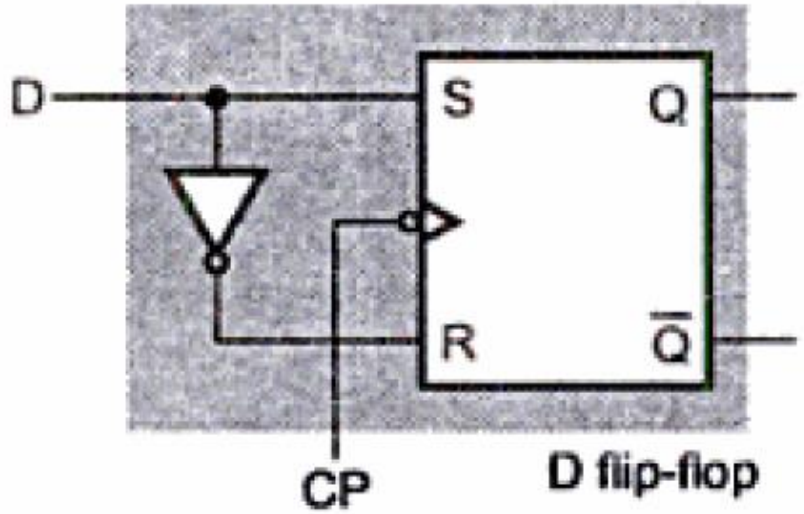
Table 6.6 (b) JK excitation table

$$Q_{n+1} = J\,Qb + Kb\,Q$$

Flip-Flop Conversion
SR FF To D FF

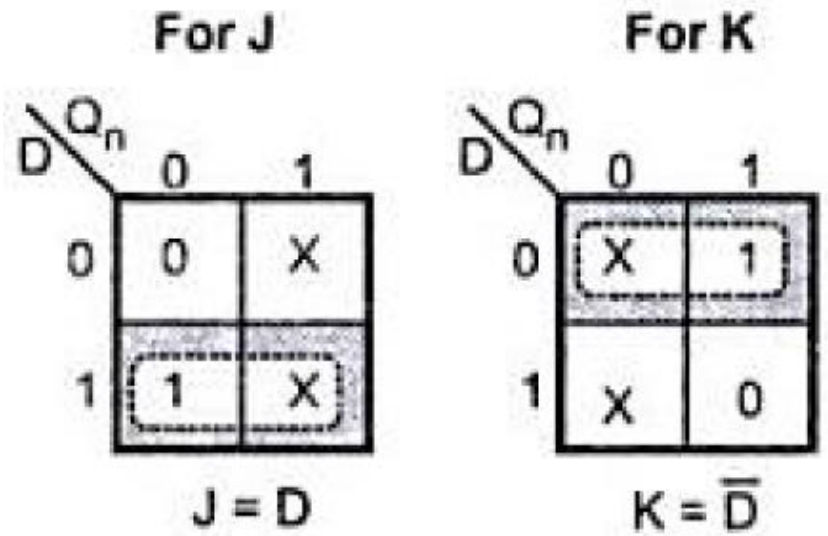
Input	Present state	Next state	Flip-flop inputs	
D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

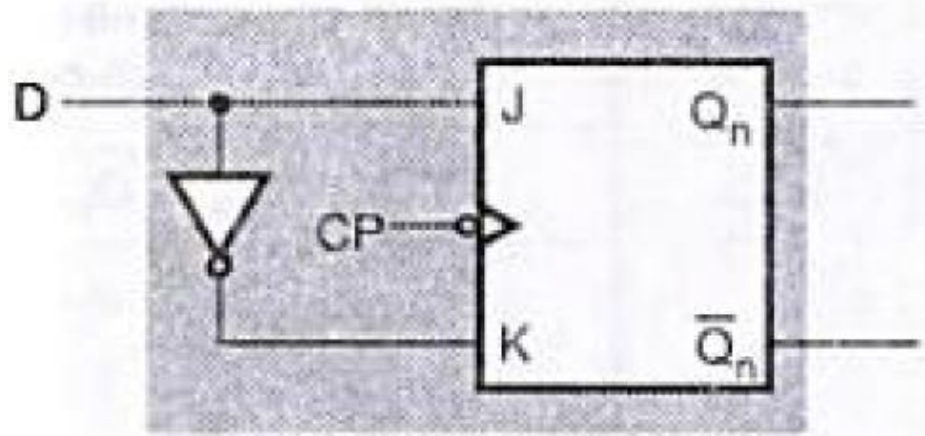




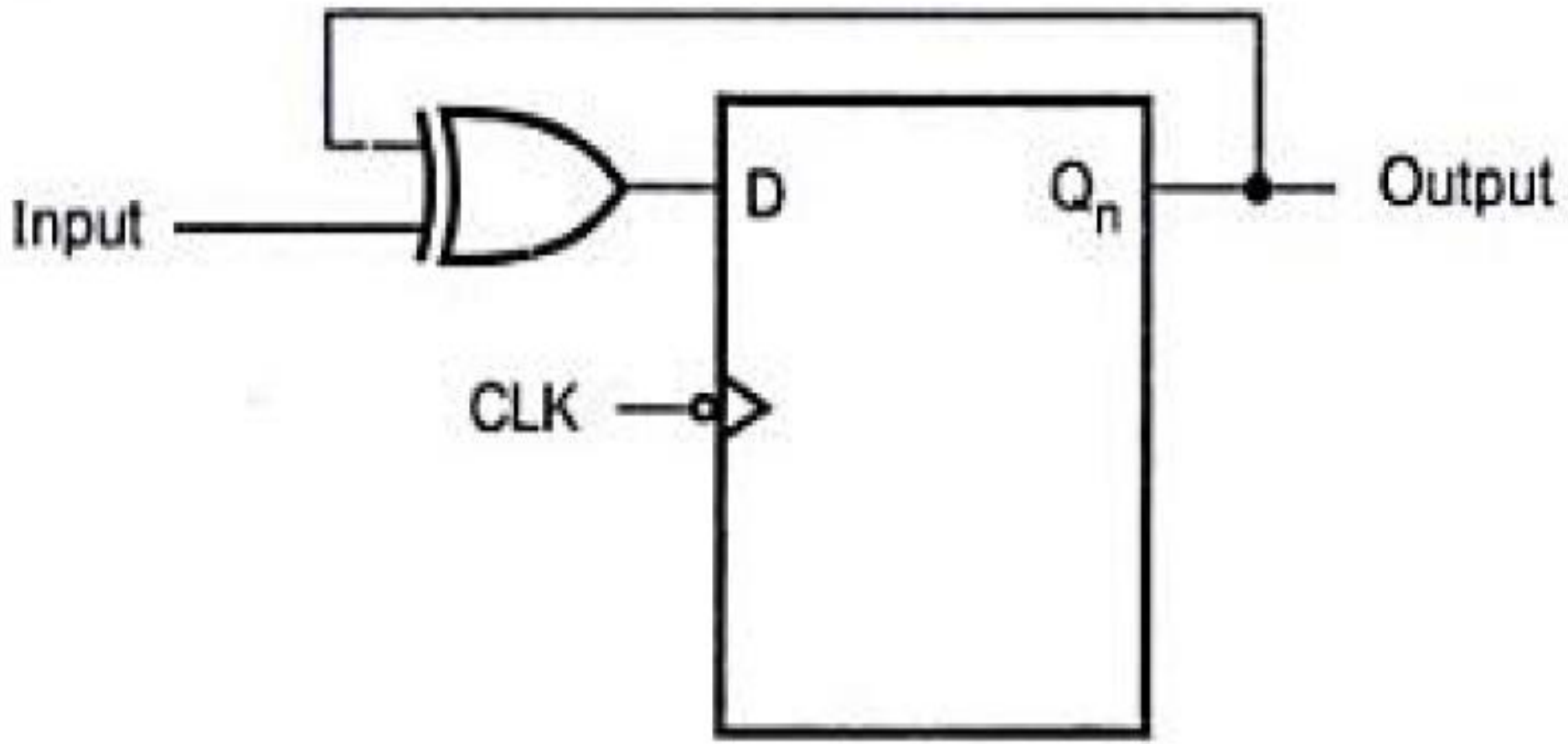
JK To D FF

Input	Present state	Next state	Flip-flop inputs	
D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0





Analysis
Prove that the given circuit is equivalent To T FF



END

NEXT is Shift Registers And Counters