B.Tech.

THIRD SEMESTER EXAMINATION, 2007-08

PULSE & DIGITAL ELECTRONICS

Time : 3 Hours] *[Total Marks : 100*

Note : *(1) Attempt all questions.*

(2) All questions carry equal marks.

(3) Be precise in your answer.

(4) No second answer book will be provided.

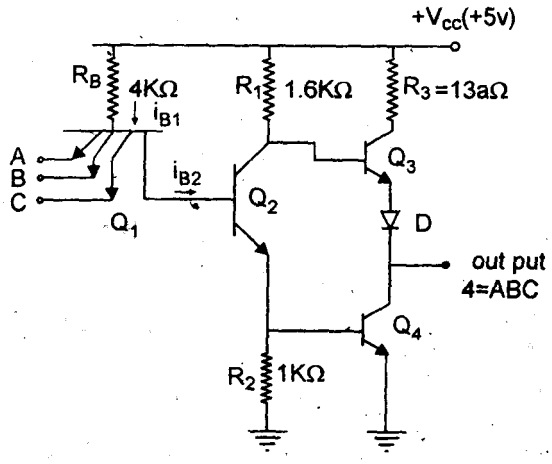
Q. 1. Attempt and four parts of the following : **5 × 4 = 20**

(a) What are the different types of output configuration for TTL gates ? Explain any one type in detail AND and NAND.

Ans. There are two output configuration for TTL logic family.

1- AND 2. NAND

Operation of TTL NAND Gate : TTL circuit uses a special single multi-emitter transistor that is fabricated with several emitters at its input. The number of emitters used depends on the desired fan-in of the circuit. Since a multi emitter transistor is smaller in area than the diode it replaces. They yield from the water is increased.



Circuit operation. : Each emitter of Q_1, acts like a diode. Therefore, transistor Q_1 and the 4 kΩ resistor act like a 3-input AND gate and rest of the circuit invert the signal. Hence the overall circuit act like a 3-input NAND gate.

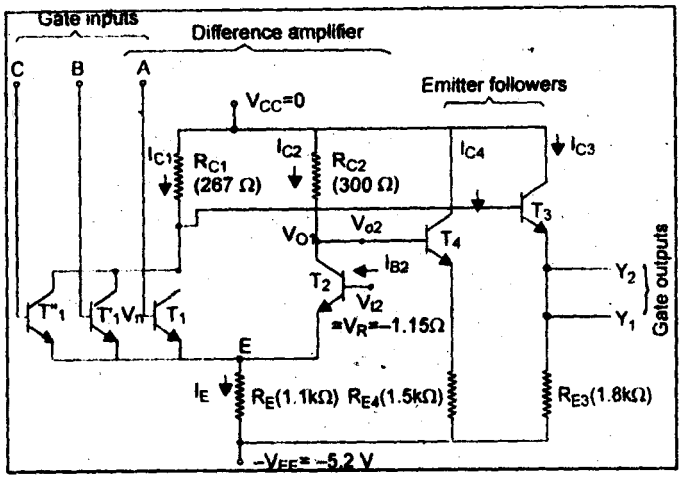
When any one or all input (A, B, C) are at ov (logic O), the corresponding emitter-base junction of Q_1 become forward biased. The value of R_B is selected so as to ensure that Q_1 is turned ON. However the value of current i_{B_2} flowing through the base of Q_2 reduces the potential at the base of Q_2, and hence transistor Q_2 and Q_4 are cut off so that he output voltage is at V_{CC} (logic 1).

If all the input is high (logic 1), emitter base junction of Q_1 is reverse biased so that it has no base current. Hence Q_1 is OFF. However its collector-base junction is forward biased supplying base current i_{B_2} to Q_2 and Q_2 get saturated.

As a result, transistor Q_2 is turned ON and drop across R_2 is sufficient to forward biased the base-emitter junction of Q_4, there by turning Q_4 ON. Hence the output at its collector is low (logic 0).

Note : The function of diode D is to prevent both Q_3 and Q_4 from being ON simultaneously.

Q. 1. (b) Describe the operation of basic circuit of the ECL gate.



Ans. Emitter-Coupled Logic (ECL) : Basically, ECL is realized using difference amplifier in which the emitters of the two transistors are connected and hence it is referred to as emitter-coupled logic. A 3-input ECL gate is shown in Fig., which has three parts : The middle part is the difference amplifier which performs the logic operation.

Emitter followers are used for d.c. level shifting of the outputs, so that $V(0)$ and $V(1)$ are same for the inputs and the outputs. Note that two output Y_1 and Y_2 are available in the circuit which are complementary. Y_1corresponds to OR logic and Y_2 to NOR logic and hence it is named as an OR/NOR gate.

Additional transistors are used in parallel to T_1 get the required fan-in. There is a fundamental difference between all other logic families (including MOS logic) and ECL as far as the supply voltage is concerned. In ECL, the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimize the effect of noise induced in the power supply (Prob.), and protection of the gate from an accidental short circuit developing between the output of a gate and ground (Prob.). The voltage corresponding to $V(0)$ and $V(1)$ are both negative due to positive end of the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig.

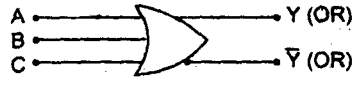
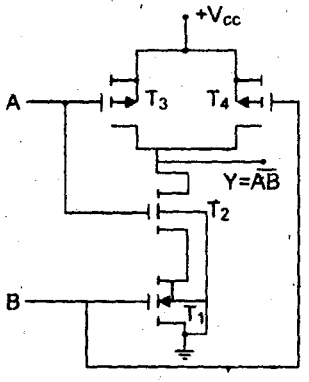


Fig. The Symbol for a 3-input OR/NOR gate.

Q. 1. (c) Explain the operation of a 2-input CMOS NAND gate.

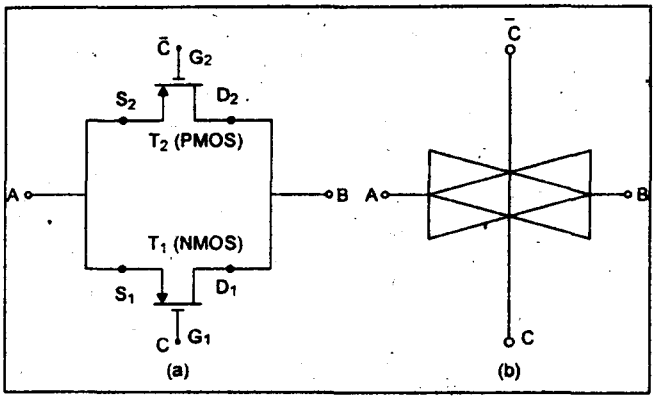
Ans. CMOS NAND and NOR Gates : A 2-input CMOS NAND gate is shown in Fig. and NOR gate in Fig. In the NAND gate, the NMOS drivers are connected in series, where as the PMOS loads are connected in parallel. On the other hand, the CMOS NOR gate is obtained by connecting the NMOS drivers in parallel and PMOS loads in series. The



operation of NAND gate can be understood from Table. The operation of the NOR gate can be verified in the similar manner (Prob.).

Table Operation of CMOS NAND gate

Inputs		*State of MOS devices*				Out put
A	*B*	T_1	T_2	T_3	T_4	*Y*
0	0	OFF	OFF	ON	ON	V_{CC}
0	V_{CC}	ON	OFF	ON	OFF	V_{CC}
V_{CC}	0	OFF	ON	OFF	ON	V_{CC}
V_{CC}	V_{CC}	ON	ON	OFF	OFF	0



Q. 1. (d) Explain merits and demerits of different logic families.

Ans. According to characteristic Merit and demerit of different logic families given by :

(i) RTL :

noise margin is 0 to 0.3 V for logic 0

propagation delay is 25 ns.

Power dissipation is 12 mW

(ii) Direct coupled transistor logic (DCTL) :

(a) DCTL is simpler than RTL.

(b) It has current hogging problem.

(c) In DCTL. Saturation voltage of load transistor may be different.

(iii) DTL Basic gates :

(a) More complex than RTL but has greater fan out.

(b) It has greater fan out than RTL.

(c) Has improved noise margin.

(d) It has more propagation delay of 30 ns.

(e) Power dissipation of a DTL gate is about 12 mW.

(iv) TTL Basic gates :

(a) Fan out : 10 - 40

(b) Power dissipation 1- 22 mW

(c) Propagation delay 1.5 to 33 ns

(v) ECL Basic gates :

(a) Propagation delay of 2 ns (lowest delay)

(b) noise immunity is worst. (noise-margin 0.3 V)

(c) Power dissipation 25 mW.

(d) High fan out.

(vi) Metal oxide Semiconductor (MOS) :

(a) MOS can be used as transistor as well as resistor also.

(b) Due to high input impedance fan out is large.

(c) Due to increase in capacitance at output of driving gate speed is reduces.

(d) propation delay time is caparable to TTL logic.

(e) Power dissipation is small.

(vii) CMOS logic gates :

(a) Power dissipation is 1 mW.

(b) CMOS fabrication process is simpler than TTL.

(c) Noise margins is 0.45 V_{CC}.

Q. 1. (e) Simplify the following Boolean function using tabulation method :

$$f(w, x, y, z) =$$

$$\Sigma m\,(1, 5, 6, 12, 13, 14) + \Sigma\, d(2, 4, 7, 9)$$

Ans. simplify this expression using K-map and implement the result with universal gates only.

$$F(w, x, y, z) =$$

$$\Sigma m\,(1, 5, 6, 12, 13, 14) + \Sigma d\,(2, 4, 7, 9)$$

To find the *PJ*

no. of 1 is	main term	Binary Eq.	1st reduction	II-Reduction	III Red.
1	1	0001	(1, 5) 0-01	(1, 5, 9, 13) - - 01	P_1
			(1, 9) -001	(4, 5, 6, 7) 01 - -	P_2
	2	0010	(2, 6) 0-10	(4, 5, 12, 13) -10 -	P_3
			(4, 5) 010 -	(4, 6, 12, 14)-1- 0	P_4
	4	0100	(4, 6) 01-0		
			(4, 12)-100		
2	5	0101	(5, 7) 01-1	P_5	
	-		(5, 13) -101	P_6	
	6	0110	(6, 7) 011-	P_7	
			(6, 14)-110	P_8	
	9	1001	(9, 13) 1-01-	P_9	
			(12, 13) 110-	P_{10}	
	12	1100	(12, 19) 11-0	P_{11}	
	7	0111	- -		
3	13	1101	P_{12}		
	14	1110	P_{13}		

Table fo find essention *PI*

Marks	1	5	6	12	13	14
PI						
P_1	×	×			×	
P_2		×	×			
P_3		×		×	×	
P_4			×	×		×
P_5		×			×	
P_6		×				
P_7			×			
P_8			×			×
P_9					×	
P_{10}				×	×	

P_{11}		×	×
P_{12}		×	
P_{13}			×

$$f(x, y, z) = P_1 + P_2 + P_3 + P_4$$

$$f(w, x, y, z) = \bar{y}\, z + \bar{w}\, x + x\, \bar{y} + x\, \bar{z}$$

Q. 1. (f) Simplify the following expression using K-map and implement the result with universal gates only. $F(A, B, C, D) = \bar{A}\,\bar{B}\,\bar{C} + A\,\bar{B} + AB\,C\,\bar{D} + \bar{A}\,\bar{B}\,C$

Ans. $F(A, C, B, D) = \bar{A}\,\bar{B}\,\bar{C} + A\,\bar{B} + AB\,C\,\bar{D} + \bar{A}\,\bar{B}\,C$

Q. 2. Attempt any four parts of the following : **5 × 4 = 20**

(a) Represent the decimal numbers '–21' in al four methods of negative binary number representation using eight bits.

Ans. Sign-Magnitude representation : The 1 in the MSB (Left most position) indicates that the number is negative.

$(-21)_{10} = (100\ 10101)_2$

One's Complement Representation : First write 21 in binary no. then convert it into it's 1's complement.

$$(21)_{10} = (00\ 010\ 101)_2$$

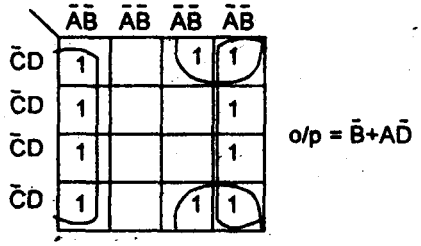
$$(-21)_{10} = (11101010)_2$$

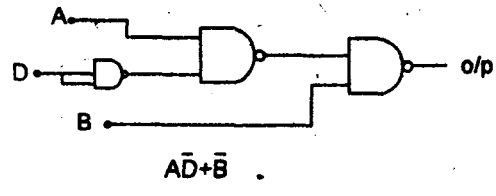
Two's Complement Representation :

MSB

number	1	0	0	1	0	1	0	1
1's comp.	1	1	1	0	1	0	1	0
Add 1	+							1
	1	0	0	1	0	0	0	0

MSB is used for representing sign. 0 for positive 1 for negative.





Q. 2. (b) Perform the following subtraction using 2's complement method :

(1) 110100-101101 **(2) 0011.1001-0001.110**

Ans. Given $M = 110100$, $N = 10101$

As N has one digit less than M. So we can write $N = 010101$
taking 2's compliment of $N = 101011$
Now Add 2's complement of N into M
M 110 100
2's complement of No. 101 011
Carry 1 011 111
Discard carry 1
Ans. 0 $M - N = (011\,111)_2 = 0(31)_{10}$
(ii) 1's complement of 0001.1110 → 1110.0001
for 2's complement of add 1 → + 0001 .0000
2's complement → 1111. 0001
Add 0011.1001 and 1111. 0001
0 0 1 1 . 1 0 0 1]
+ 1 1 1 1 . 0 0 0 1
carry 1 0 0 1 0 . 1 0 1 0
Discard carry Ans is 0 0 10 . 1 0 10

Q. 2, (c) Design a combinational circuit that converts a 3-bit Gray code to 3-bit binary number.

Implement the circuit with exclusive OR gates.

Ans.

Decimal No.	Binary				Gray			
	B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

Truth Table :

K maps are given :

G_1G_0 \ G_3G_2	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	0	1	1
10	0	0	1	1

G_1G_0 \ G_3G_2	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

Simplified expression from K maps

G_1G_0 \ G_3G_2	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	1	0	1	0
10	1	0	1	0

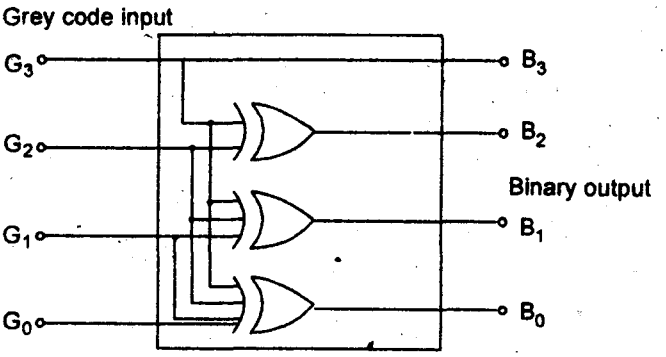
G_1G_0 \ G_3G_2	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

$B_3 = G_3$

$B_2 = G_2 \oplus G_3$

$B_1 = G_1 \oplus G_2 \oplus G_3$

$B_0 = G_0 \oplus G_1 \oplus G_2 \oplus G_3$



Gray to Binary code converter

Q. 2. (d) Show that a full subtractor can be constructed with two half subtractor and an OR gate.

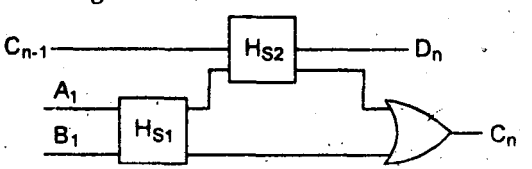
Ans. Truth table for full subtractor

Input			Output	
A_n	B_n	C_{n-1}	D_n	C_n
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

on Similarly $D_n = A_n \oplus B_n \oplus C_{n-1}$

$$C_{11} = \overline{A_n}\, B_n + \overline{B_n} C_{n-1} + A_n \overline{C_{n-1}}$$

using half- subfractors



Q. 2. (e) Implement the following Boolean function with a multiplexer :
F(A, B, C, D) = Σm (1, 3, 4, 11, 12,13, 14, 15)

Ans.

$F(A, B, C, D) = \Sigma m(1, 3, 4, 11, 12, 13, 14, 15)$

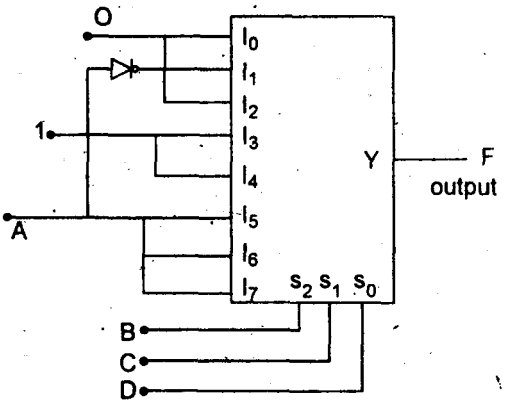
As function has four variable. We need a mix with three selection lines *B, C, D.* Input *A*

Implementation table :

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'	0	(1)	2	(3)	(4)	5	6	7
A	8	9	10	(11)	(12)	(13)	(14)	(15)

A_1, I_3, I_4 are not depends on A so they connected to 1.

I_0, I_2 connected to ground '0' $I_1 = A'$.



Q. 2. (f) Explain the function of PLA with suitable example.

Ans. Programmable Logic Array (PLA) : For cases where the number of don't-care conditions is excessive, it is more economical to use a second type of LSI component called a *programmable logic array,*or PLA. A PLA is similar to a ROM in concept; however, the PLA does not provide full decoding of the variables and does not generate all the minterms as in the ROM, In the PLA, the decoder is replaced by a group of AND gates, each of which can be programmed to generate a product term of the input variables. The AND and OR gates inside the PLA are initially fabricated with fuses among them. The specific Boolean functions are implemented in sum of products from by blowing appropriate fuses and leaving the desired connections.

A block diagram of the PLA is shown in Fig. It consists of n inputs, m outputs, k product terms, and m sum terms. The product terms constitute a group of k AND gates and the sum terms constitute a group of m OR gates. Fuses are inserted between all n inputs and their complement values to each of the AND gates. Fuses are also provided between the outputs of

the AND gates and the inputs of the OR gates. Another set of fuses in the output inverters allows the output function to be generated either in the AND-OR form or in the AND-OR-INVERT form. With the inverter fuse in place, the inverter is bypassed, giving an AND-OR implementation. With the fuse blown, the inverter becomes part of the circuit and the function is implemented in the AND-OR-INVERT form.

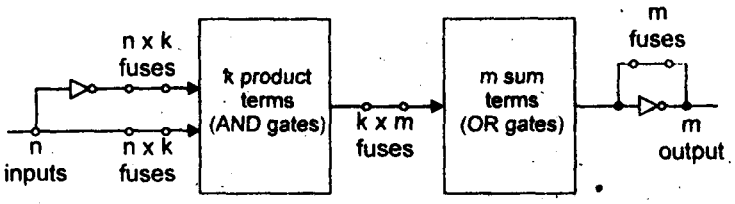


Fig.PLA block diagram

Q. 3. Attempt any two parts of the following : **10 × 2 = 20**

(a) Explain the differences among a truth table, a state table, a characteristic table and an excitation table of flip-flop.

Ans. The time sequence of inputs, outputs, and flip-flop states can be enumerated in a *state table*. The state table for the circuit of Fig. is shown in Table. The table consists of four sections labeled *present state, input, next state,* and *output*. The present state section shows the states of flip-flops A and B at any given time t. The input section gives a value of x for each possible present state. The next-state section shows the states of the flip-flops one clock period later at time $t + 1$. The output section gives the value of y for each present state.

The derivation of a state table consists of first listing all possible binary combinations of present state and inputs. In this case, we have eight binary combinations from 000 to 111. The next -state values are then determined from the logic diagram or from the state equations. The next state of flip-flop A must satisfy the state equation.

$$A(t + 1) = A\bar{x} + Bx$$

The next-state section in the state table under column A has three 1's where the present

Table

State Table for the Circuit of Fig.

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

state and input value satisfy the conditions that the present state of A and input x are both equal to 1 or the present state of B and input x are both equal to 1. Similarly, the next state of flip-flop B is derived from the state equation $B(t+1) = A'x$

It is equal to 1 when the present state of A is 0 and input x is equal to 1. The output column is derived from the output equation $y = Ax' + Bx$

Section Analysis of Clocked Sequential Circuits Table

Second Form of the State Table

	Next State		Output	
Present State	$x=0$	$x=1$	$x=0$	$x=1$
AB	AB	AB	y	y
00	00	01	0	0
01	00	11	1	0
10	00	10	1	0

Characteristic Tables : The characteristic tables of four flip-flops were presented in section. When analyzing sequential circuits, it is more convenient to present the characteristic table in a somewhat different form. The modified form of the characteristic tables of four types of flip-flops are shown in Table. They define the next state as a function of the inputs and present state. $Q(t)$ refers to the present state prior to the application of a pulse. $Q(t+1)$ is the next state one clock period later. Note that the clock-pulse input is not listed in the characteristic table, but is implied to occur between time t and $t+1$.

The characteristic table for the JK flip-flop shows that the next state is equal to the

Table.

Flip-Flop Characteristic Tables

JK Flip-flop

J K	$Q(t+1)$	
0 0	$Q(t)$	No change
0 1	0	Reset
1 0	1	Set
1 1	$Q'(t)$	Complement

RS flip-flop

S R	$Q(t+1)$	
0 0	$Q(t)$	No change
0 1	0	Reset
1 0	1	set
1 0	?	Unpredictable

D flip-flop

D	$Q(t+1)$	
0	0	Reset
1	1	Set

T Flip-flop

T	$Q(t+1)$	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Present state when inputs J and K are both equal to 0. This can be expressed as $Q(t+1) = Q(t)$, indicating that the clock pulse produces no change of state. When $K=1$ and $J=0$, the clock pulse resets the flip-flop and $Q(t+1)=0$. With $J=1$ and $K=0$, the flip-flop sets and $Q(t+1)=1$. When both J and K are equal to 1, the next state changes to the complement of the present state, which can be expressed as $Q(t+1)=Q'(t)$.

Flip-Flop Excitation Tables : The characteristic table is useful for analysis and for defining the operation of the flip flop. It specifies the next state when the inputs and present state are known. During the design process, we usually know the transition from present state to next state and wish to find the flip-flop input conditions that will cause the required transition. For this reason, we need a table that lists the required inputs for a given change of state. Such a list is called an *excitation table.*

Q. 3. (b) What is shift register ? Explain the operation of a 4 bit shift register. The content of a 4 bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift ?

Ans. Shift Registers : A register that is used to store binary information is known as a *memory register.* A register capable of shifting binary information either to the right or to the left is called a *shift register.* The shift register permits the stored data to move from a particular location to some other location within the register. In a shift register, the flip-flops are connected in such a way that the bits of a binary number are entered into the shift register, shifted from one position to another and finally shifted out.

There are two methods of shifting the data viz, (i) serial shifting and (ii) parallel shifting. The *serial shifting* method shifts one bit at a time for each clock pulse in a serial fashion, beginning with either MSB or the LSB. For example, a 4-bit register requires four clock pulse to shift a bit from the input to the output. In *parallel shifting,* operation, all the data (input or output) get shifted simultaneously during a single clock pulse. Hence, the parallel shifting method is much faster than the serial shifting method. These two methods can be used to shift data into a register and out of the register.

Shift registers are classified into the following four types based on how binary information is entered or shifted out :

1. Serial-in-Serial-out (SISO)
2. Serial-in-parallel-out (SIPO)
3. Parallel-in-Serial-out (PISO)
4. Parallel-in Parallel-out (PIPO)

Serial-in-Serial-out Shift Register : This type of shift register accepts data serially, *i.e.,* one bit at a time on a single input line. It products the stored information on its single output also in serial form. Data may be shifted left (from low to high order bits) using *shift-left register* or shifted right (from high to low order bits) using *shift-right register.*

Shift-left register : A shift-left register can be built using $J-K$ flip-flops or D flip-flops as shown in Fig. (a) and (b) respectively. A $J-K$ flip-flop based shift register requires connection of both J and K inputs. Input data are connected to the J and K inputs of the rightmost (lowest order) flip-flop. To input a 1, one should apply a 1 at J input, *i.e.,* $J=1$ and $K=0$; to input a 0, a 0 at

J input, *i.e.*, $J=0$ and $K=1$ should be applied. When the clock pulse is applied, the data will be shifted bit by bit to the left.

In the shift register using D flip-flops delay (D) input of the rightmost flip-flop is used as a serial input line. To input data 1, one should apply a 1 at D input and to input data 0, a 0 at the D input should be applied.

Number of Shift	Input	Context of Before shift	Register After shift
I	1 -	1101	1110
II	0	1110	0110
III	1	0110	1011
IV	1	1011	1101
V	0	1011	0110
VI	1	1101	1011

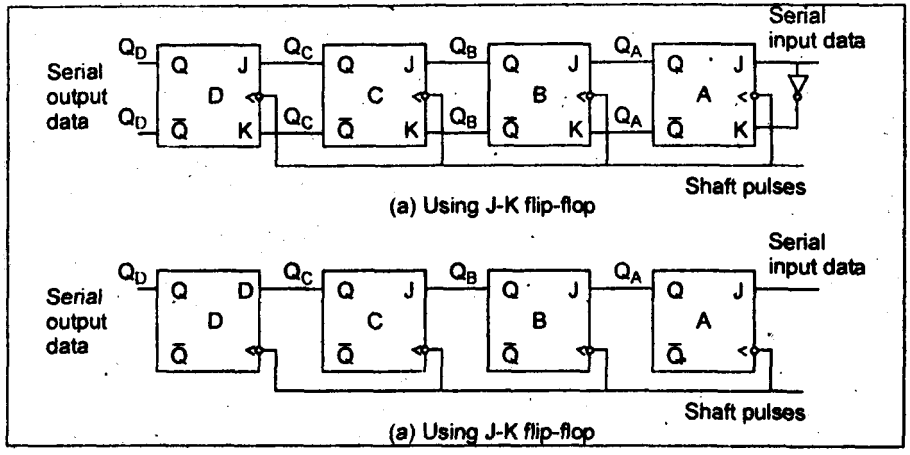


Fig. Shift-left register

As shown in Fig. the clock pulse is applied to all the flip-flop simultaneously. When the shift or clock pulse occurs, each flip-flop is set or reset according to the data at the respective flip-flop input. Thus, the input data bit at serial input line is entered into stage A by the first shift pulse. At the same time, the data of stage A is shifted into stage B and so on for the following stages. For each shift pulse, data stored in the register stage shifts to the left one stage. Now data is entered into stage A, whereas the data present in stage D are shifted out (to the left) for use by some other shift register or other building block of digital system.

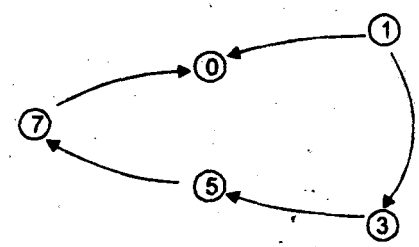
Solution of the Numerical part.

After six shift content of Register 1 0 1 1.

Q. 3. (c) Design a synchronous counter using J-K flip flops with the following repeated binary sequence : " 0, 1, 3, 5, 7".

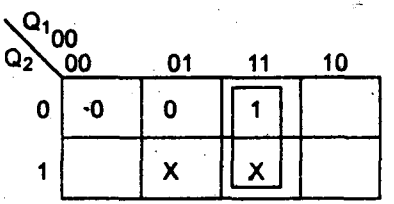
Ans. The largest digit to be represents is 7. To represent 7 in binary form minimum 3 flip flops are needed state diagram is given below

The present state & next state with excited clips J_2K_2, J_1K_1 & J_0K_0 is given below



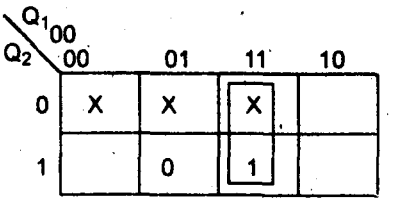
P S			N S								
Q_2	Q_1	Q_0	Q_{2+1}	Q_{1+1}	Q_{0+1}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	×	0	×	1	×
0	0	1	0	1	1	0	×	1	×	×	0
0	1	1	1	0	1	1	×	×	1	×	0
1	0	1	1	1	1	×	0	1	×	×	0
1	1	1	0	0	0	×	1	×	1	×	1

For J_0 :



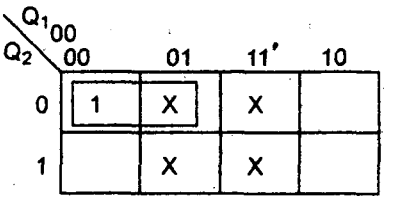
$J_{12} = Q_1 Q_0$

For K_0



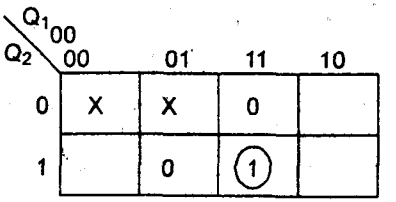
$K_1 = Q_1 Q_0$

For J_1 :



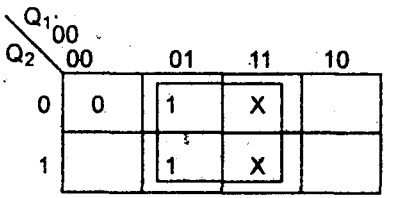
$J_0 = Q_2 Q_1$

For K_1



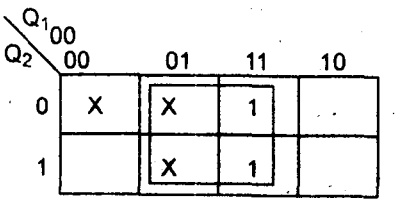
$K_0 = Q_2 Q_1 Q_0$

For J_2 :



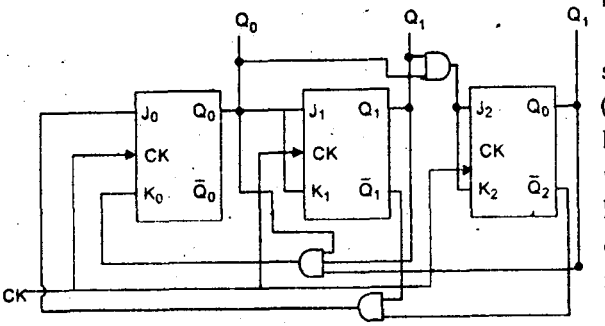
$J_1 = Q_0$

For K_2



$K_1 = Q_0$

Synch. Counter :



Q. 4. Attempt any two parts of the following : $10 \times 2 = 20$

(a) Write short notes on the following :

(1) Read only memories

(2) Sequesntial memories

Ans. Rom : A read only memory is a semiconductor memory device used to store information which is permanent in nature. It has become an important part of many digital system because of its low cost, high speed, system-design flexibility and data non-volatility. The read only memory has a variety of applications in digital systems, such as implementation of combinational logic and sequential logic, character generation, look-up table, microprocessor programme storage, etc.

ROM Organization : A read-only memory is an array of selectively open and closed unidirectional contacts. The address decoder of Fig.is usually divided in two parts for simplifying the decoder design. One half of the address lines are decoded by one decoder used to energize one of the row lines, whereas the other half of the address lines are decoder by another decoder used to activate column lines. This method of addressing is referred to as two-dimensional, $X-Y$, or coincident-selection, addressing. A unidirectional switch is incorporated at the junction of every row and column.

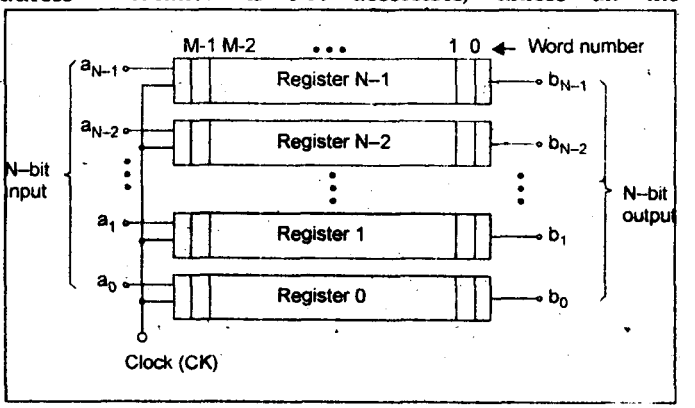
A 16-bit ROM array is shown in Fig.To select any one of the 16 bits, address $(A_3 A_2 A_1 A_0)$ is required. The lower order two bits $(A_1 A_0)$ are decoded by the decoder D_L which selects one of the four rows, whereas the higher order two bits $(A_3 A_2)$ are decoded by the decoder D_H which activates one of the four-column sense amplifiers.

The diode matrix is formed by connecting one diode, along with a switch between each row and column. For example, the diode D_{21} is connected between row 2 and column1.

The output is enabled by applying logic 1 at the chip select (CS) input.

Programming a ROM means to selectively open and close the switches in series with the diodes. For example, if the switch of the diode $D_{21}$is in closed position and if the address input is 0110, row 2 is activated connecting it to column1. Also, the sense amplifier of column 1 is enabled which gives logic 1 output if the chip is selected (CS =1). This shows that a logic 1 is stored at the address 0110. On the other hand, if the switch of diode $D_{21}$is open, logic 0 is stored at the address 0110.

Sequential Memory : In it, the words are stored-in and read out in sequence. pth location is being accessed at a particular time,then $(p+q)$ location is not accessible, unless all the



intermediate location have been accessed one by one. In sequence Shift Register are examples of sequential memories. Another kind of shift registers gaining popularity in recent years are charge-coupled devices (CCDs) and bubble memories. The operation of these devices is entirely different from those using transistors.

A sequential memory of size $M \times N$ is show in Fig. It requires N shift registers, each of M stages. Each register holds one of the N bits of each of the M words. With each clock cycle, the bits in each register will advance towards the right by one bit position, and the stored words will appear sequentially at the output of the registers. This configuration is referred to as *first-in-first-out* (FIFO) sequential-memory system, since the words which is entered first will be the one read out first.In contrast, if the outputs are taken from the $(M-1)$th stage instead of 0th stage, the resulting configuration is called as *last-in-first-out* (LIFO). The shift registers used in this configuration must have a provision of shifting the bits in either direction.In the FIFO sequential-memory system, the word being read may be transferred back to the left-most register position. This is know as a circulating shift register. The circulating feature is not employed in LIFO sequential- memory systems.

$M \times N$ sequential memory.

Static Shift Register : As discussed in Section, a shift register is implemented with FLIP-FLOPs. The information is loaded into it or retrieved from it in a sequential manner in synchronism with clock pulses. The information will remain in the register as long as desired provided power is supplied to the circuit. Both bipolar and MOS devices can be used for implementing shift registers. This type of shift register to as the static shift register.

It is impractical to fabricate static shift registers of large capacities because of excessively large requirements of power and silicon area. An alternative approach, to overcome these difficulties, is to fabricate an I SI dynamic shift register using MOS devices.

Dynamic Shift Register : In a dynamic memory system, the information is stored

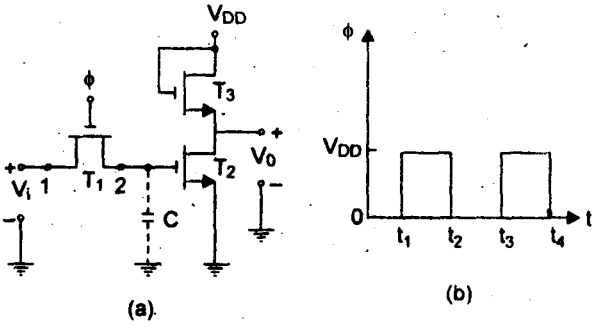


Fig. (a) One-bit dynamicNMOS cell
(b) Clock waveform φ

temporarily by charging the parasitic capacitances of the electronic devices. The MOS device is uniquely suited for this purpose, because at its input it looks like a capacitor (parasitic gate-substrate capacitance) which serves as temporary storage for the incoming data. These capacitors lose their charge due to leakage and, therefore, to maintain the required logic levels, they need to be refreshed continuously . Refreshing is achieved by simply recirculating the data held with in the register. For this reason, dynamic registers must be operated at a minimum operating frequency of about 10 KHz, and these cannot be used for low-frequency applications.

Q. 4. (b) A current pulse of amplitude I is applied to a parallel *RC* circuit a shown in figure below. Plot to scale (approximately) wave forms of the current i_c for the cases.

(i) $t_p < RC$

(ii) $t_p = RC$ and

(iii) $t_p > RC$

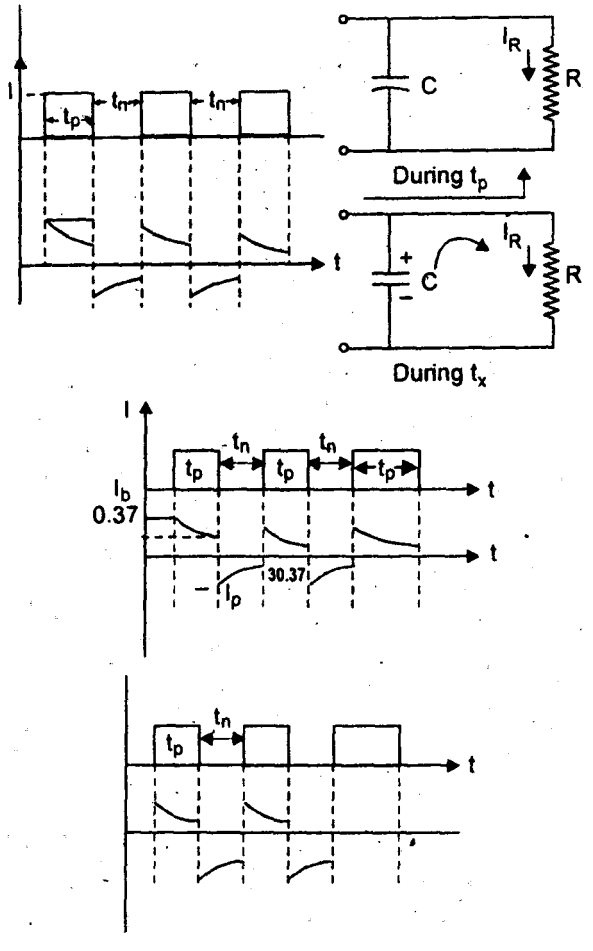
Ans. Charging current of capacitor during $i_c = I(1-e^{-t//jwc})$

when $t_p < RC$

$t_p = RC$

During t_x capacitor will charge to 0.63 V_{max}.

$t_p > RC$



Q. 4. (c) Describe the successive approximation A/D conversion principle. Explain this type of A/D converter with the neat diagram.

Ans. Successive Approximation Type A/D Converter : In successive approximation type A/D converter, the conversion time is constant and proportional to the number of bits in the digital output, unlike the counter and continuous type A/D converters.

The basic principle of this A/D converter is that the unknown analog input voltage has been approximated with an n-bit digital value by trying one bit at a time, beginning with the MSB. This type of conversion process for a 4-bit conversion is shown in Fig. Since the conversion involves single bit at a time, a ring counter can be used.

This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.

1. The ring counter is initially reset to '0'. Normally, ring counter is a part of successive approximation register (SAR).

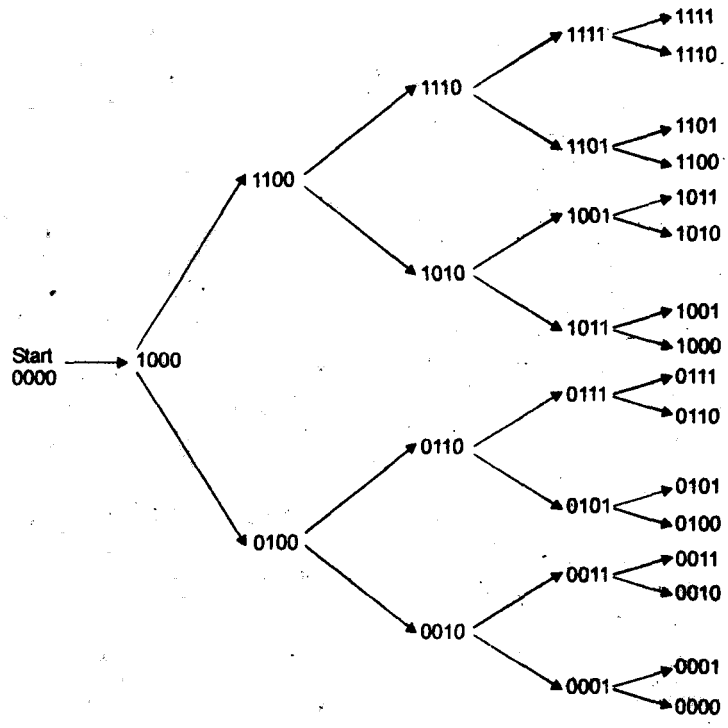
2. The MSB is initially set to '1' and the digital equivalent is compared with the unknown analog input voltage.

3. If the analog input voltage is higher than the digital equivalent, the MSB is retained as '1' and the second MSB is set to '1'. Otherwise, the MSB is reset to '0' and the second MSB is set to '1'.

4. Comparison is made as given in step 2 to decide whether to retain or reset the second MSB and then the third MSB is set to '1'.

5. The above process is repeated down to LSB and by this time the converted digital value is available in the SAR.

From Fig. it can be seen that the conversion time is constant (*i.e.*, four cycles) for various digital outputs. For an 8-bit successive approximation type A/D converter, the conversion requires 8 cycles, irrespective of the amplitude of analog input voltage.



The basic block diagram of successive approximation type A/D converter is shown in Fig. It is constructed using n-bit successive approximation register, which is capable of implementing the successive approximation principle given in Fig. The output of the SAR is given to an n-bit D/A converter whose output acts as the variable reference of the comparator, while t he other input of the comparator is connected with the unknown analog input voltage. Here, the comparator output is used to approximate the unknown analog input voltage with the n-bit digital value of SAR, by following the same five steps discussed earlier.

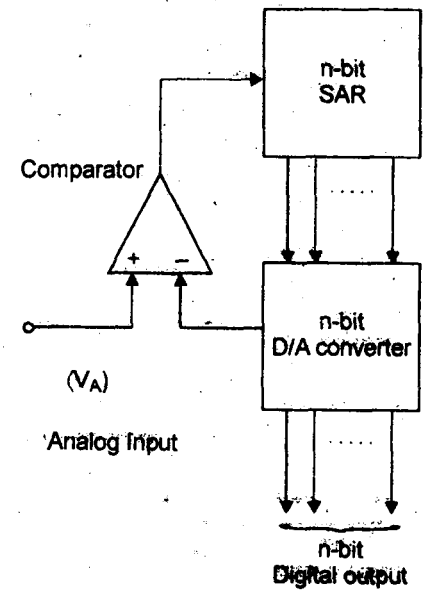


Fig. Block diagram of successive approximation type A/D converter

Q. 5. Attempt any two parts of the following :

(a) What is higher order active filter ? Design a second order low pass filter at a high cut off frequency of 1 kHz.

Ans. Higher-order filters, such as third, fourth, fifth, and so on, are formed simply by using the first-and second-order filters. For example, a third-order low-pass filter is formed by connecting in series or cascading first-and second-order low-pass filters; a

fourth-order low-pass filter is composed of two cascaded second-order low-pass-pass sections, and so on. Although there is no limit to the order of the filter that can be formed, as the order of the filter increase, so does its size. Also, its accuracy declines, in that the difference between the actual stopband response and the theoretical stopband response increase with an increase in the order of the filter. Figure shows third-and fourth-order low-pass

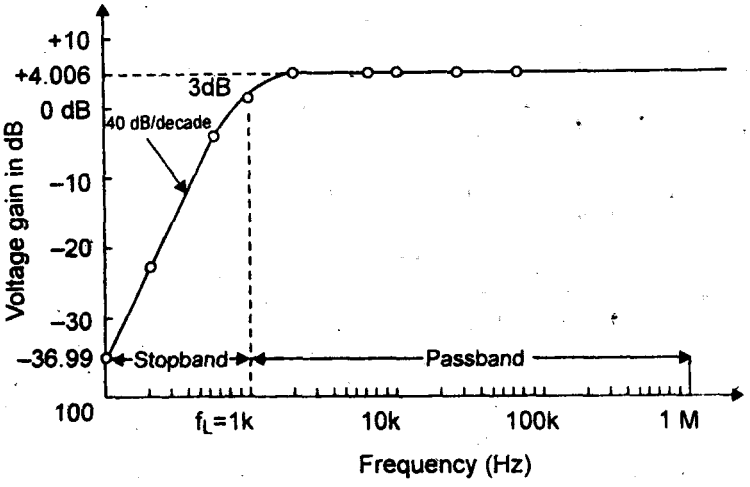


Fig. Frequency resonce for expame7-6

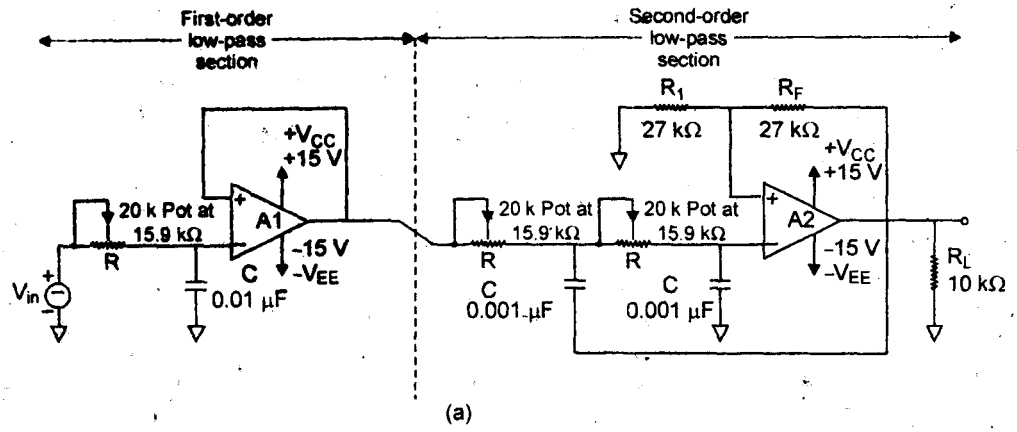
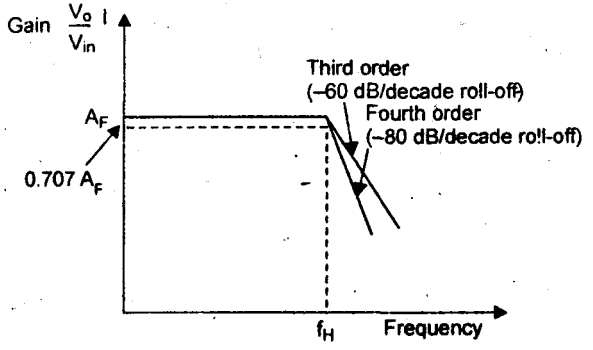


Fig. Third-order and (b) fourth-order low-pass Butterworth filters. (c) Their frequecy responce

A_1 and A_2 dual op-amp

Butterworth filters. Note that in the third-order filter the voltage gain of the first-order section is *one*, and that of the second-order section is *two*.

Since the frequency-determining resistors are equal and the frequency-determining capacitors are also equal, the high cutoff frequencies of the third-and fourth-order low-pass filters in Figure (a) and (b) must also be equal.



(c)

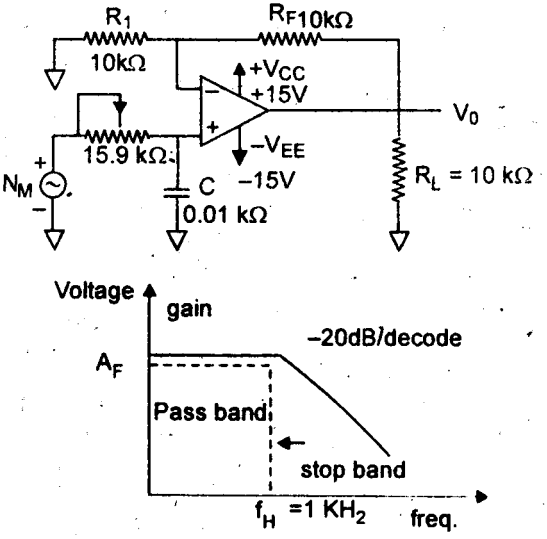
That is, $$F_H = \frac{1}{2\pi RC}$$

As with the first-and second-order filters, the third-and fourth-order high-pass filters are formed by simply interchanging the positions of the frequency-determining resistors and capacitors in the corresponding low-pass filters. The high-order filters can be designed by following the procedures outlined for the first-and second-order filters. However, note that the overall gain of the higher-order filters is *fixed* because all the frequency-determining resistors and capacitors are equal.

Generally, the minimum-order filter required depends on the application specification. Although a higher-order filter than necessary gives a better stop-band response, the higher-order type filter is more complex, occupies more space, and is more expensive.

follow the preceding design steps

1. $F_H = 1$ KHz
2. Let $C = 0.01\,\mu F$
3. Then $R = \frac{1}{2\pi \times 10^3 \times 10^{-8}} = 15.9\ K\Omega$
4. Let $R_1 = R_F = 10\ K\Omega$



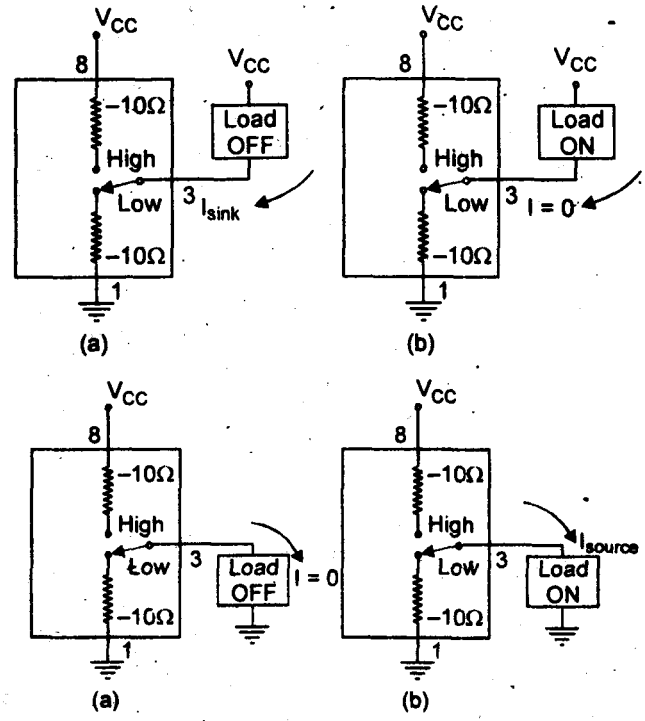
Higher-order filter

Q. 5. (b) What are the basic modes in which the 555 timer operates ? Write few applications of 555 timer and explain any one in detail.

Ans. Two mode of 555 Timer, Given below :

(i) Monostable Multivibrator : A monostable multivibrator circuit using a 555 Timer is shown in Fig. If the trigger input is held HIGH, then under steady-state condition, the transistor, T_1 is ON, the discharge and output terminals are at LOW level. It can be verified that T_1 cannot be OFF under steady-state (Problem). When a negative pulse applied at the trigger input crosses the voltage $V_{CC}/3$, the output of the comparator 2 goes

HIGH which sets the FLIP-FLOP and consequently T_1 turns OFF and the output goes HIGH. The capacitor C starts getting charged to V_{CC} with the time constant, $\tau = R_A C$. The circuit remains in this condition even after the trigger has returned to logic 1. When the increasing capacitor voltage reaches 2/3 V_{CC}, the output of the comparator 1 goes HIGH which resets the FLIP-FLOP. The transistor T_1 goes to saturation, thereby discharging the capacitor and the output goes LOW. The various waveforms are shown in Fig. This is a non-retriggerable monostable multivibrator. This circuit can be converted to a retriggerable type if reset is conected to trigger input instead of to V_{CC} (Problem) and it is triggered at the positive-edge of tl.e trigger pulse.



The output timing interval, T is given by 1.1 R_A . C.

(ii) Astable Multivibrator : An astable multivibrator using 555 timer is shown in Fig. Let us assume that the output is in HIGH state and the capacitor C is charging through resistors R_A and R_B [time constant $\tau_1 = (R_A + R_B)\, C$]. When the voltage across $C(v_C)$ reaches 2/3 V_{CC}, the output goes LOW and C starts discharging through R_B with a time constant $\tau_2 \approx R_B$. C. When v_C drops below V_{CC} /3, the timer is triggered and the output again goes HIGH. The capacitor C now again starts charging towards V_{CC} with the time constant τ_1. The various waveforms are shown in Fig. The charging and discharging time intervals are given by

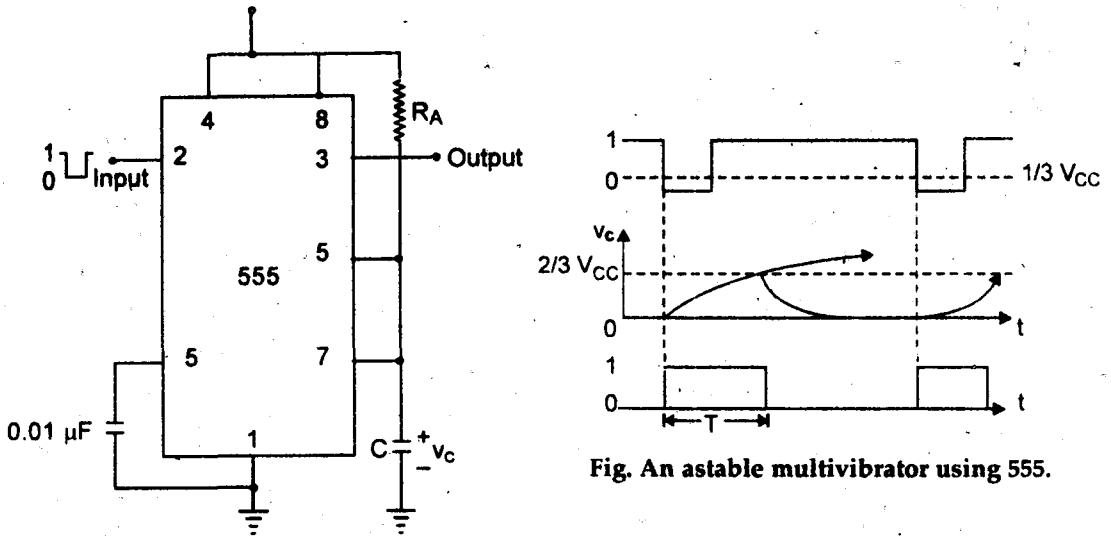


Fig. An astable multivibrator using 555.

Waveforms of monostable multivibrator.

$$T_1 \approx 0.7\, C\,(R_A + R_B)$$

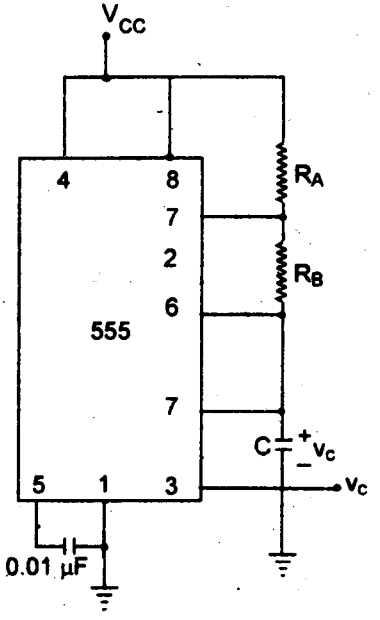
and

$$T_2 = 0.7\, C\, R_B$$

Therefore,

$$f = \frac{1}{T} = \frac{1}{T_1 + T_2} = \frac{14}{C(R_A + 2R_B)}$$

and the duty cycle



$$D = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$

From Eq. we note that the duty cycle is always different from 50%. It can be made 50% (symmetrical square wave) by connecting a diode across R_B, which will clamp the voltage across R_B when the capacitor is charging and therefore if R_A and R_B are equal, τ_1 and τ_2 will be same. It is also possible to generate a symmetrical square wave by using the output of 555 as clock input of a T-type FLIP-FLOP with $T = 1$. The output of the FLIP-FLOP will be a symmetrical square wave.

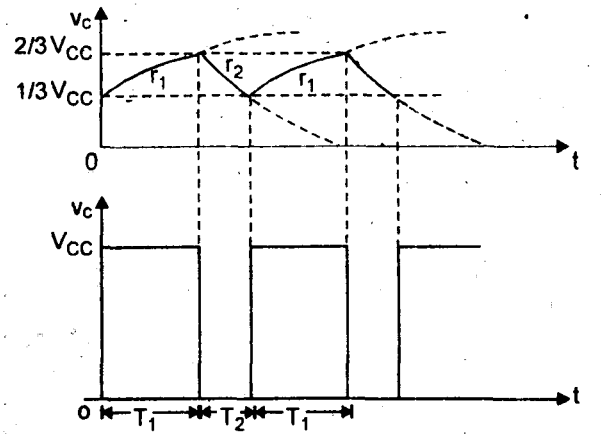


Fig. Waveforms of 555 astable multivibrator.

Q. 5. (c) Describe the fixed voltage IC regulators. Also explain the typical performance parameters for the voltage regulators.

Ans. Power Supply : Application of Voltage Regulators : Since a power supply is a vital part of all electronic systems, it will be discussed first. Most digital ICs, including microprocessors and memory ICs, operate on a ±5-V supply, while almost all linear ICs (op-amps and special-purpose ICs) require ±5-V supplies. Therefore, the power supply presented in this section will have ±5 and ±5.

Figure show the block diagram of a typical power supply. The schematic diagram of a power supply that provides output voltages of ±5 V at 1.0 A and ±15 V at 0.500 A is shown in Fig. In this figure two separate transformers are used because they are readily available; however, it is possible to custom design a single transformer with the same specification to replace the two.

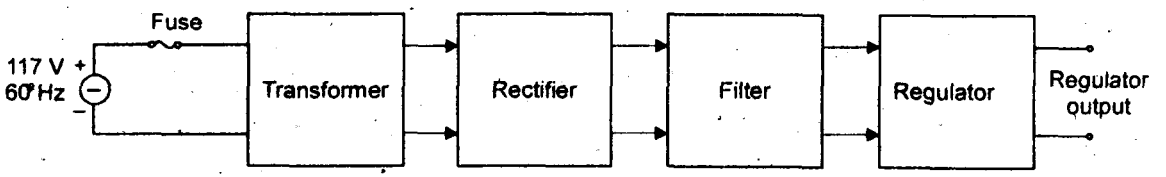


Fig. Block diagram of a power supply

The ± 15 -V supply voltages are obtained from a 26.8-V center-trapped (CT) transformer, and the ± 5 -V supply voltages are obtained from the 12.6-V CT transformer. The output of these secondaries is then applied to the bridge rectifiers, which convert the sinusoidal inputs into full-wave rectified outputs. The filter capacitors at the output of the bridge rectifiers are charged to the peak value of the rectified output voltage whenever the diodes are forward biased. Since the diodes are not forward biased during the *entire* positive and negative half-cycle of the input waveform, the voltage across the filter capacitors is a pulsating dc that is a combination of dc and a ripple voltage. From the pulsating dc voltage, a regulated dc voltage is extracted by a regulator IC.

Consider first how the ± 15 -V supply voltages are obtained in the circuit of Figure. As shown in Section, the 7815 is a ± 15 -V regulator, the 7915 is a − 15-V regulator, and both can deliver output current in excess of 1.0 A. They will hence perform satisfactory in the circuit of Figure by providing ± 15 V at 0.500 A. However, since the drop-out voltage ($V_{in} - V_o$) is 2V, the input voltage for the 7815 must be least +17 V and that for the 7915 must be at least + 17 V. This means that the rectified peak voltage must be greater than +17 V and −17 V, which in turn implies that the secondary voltage must be larger than 34 V peak or 24 V rms, The voltage across the center-trapped secondary in Figure is 26.8 V rms, thus satisfying the minimum voltage requirement of 24 V rms. Also, the peak voltage between either of the secondary terminals and the center-tap (ground terminal) is 13.4 ($\sqrt{2}$) = 18.95 V peak, which is less than the maximum peak voltages of +35 V and −35 V for the 7815 and 7915, respectively.

Note that the voltages across the two halves of the center-trapped secondary are equal in amplitude but opposite in phase. During the positive half-cycle of the input voltage, diode D_1 conducts and capacitor C_1 charges toward a positive peak value ≅ − 18.95V. At the same time, diode D_3 is also conducting; hence capacitor C_3 charges toward a negative peak value ≅ −18.95 V. This means that the voltage across nonconducting diodes D_2 and D_4 is 37.90 V peak, which implies that the peak-reverse-voltage (PRV) rating of the bridge rectifiers must be larger than 37.90 V peak or 26.8 V rms. the PRV rating of the bridge rectifier diodes, also known as a *working inverse voltage* (WIV), is specified on the data sheets. The bridge rectifier, MDA200 (Motorola's rectifier) in Figure, has a PRV rating of 50 V, which is higher than needed. This bridge rectifier is, in fact, used here because it is readily available and more commonly used.

During the negative half-cycle of the input waveform, diodes D_2 and D_4 conduct and charge capacitors C_1 and C_3 toward the peak voltage of 18.95 V with indicated polarities. Note, however, that the diode pair that conducts during either the positive or negative half-cycle does not do so for the entire half-cycle. The diodes conduct only during the time when the anodes are positive with respect to the cathodes. In other words, when the diodes are forward biased, the capacitors are charged by current pulses. Data sheets give the maximum average rectified current $I_{o\,max}$ that the diode can safely handle. For the MDA200, $I_{o\,max}$ is 2.0 A.

I_{max} it is 60 A for the MDA200.

Finally, the size of the filter capacitor depends on the secondary current rating of the transformer. As a rule of thumb, a 1500-μF capacitor should be used for each ampere of current. The working voltage rating (WVDC) of the capacitor, on the other hand, depends on the peak rectified output voltage and must be at least 20% higher than the peak value of the voltage it is expected to charge to. Capacitors C_1 and C_3 satisfy these requirements (see Figure). Capacitors $C_2$and C_4 at the output of 7815 and 7915 regulators, respectively, help to improve the transient response and should be in the range of 1 μF.

power dissipated = (dropout voltage) (current) $= (18.95 - 15)(0.5) = 1.98$ W

Similarly, the power dissipated by the 5-V regulators is $(8.91 - 5)(1.0) \simeq 3.91$W

Besides the ± 15 and ± 5-V regulated supply voltages, there is often a need for a 60-Hz square-wave signal, which is used as a time base in scanning the digital displays and a trigger for sequential and timing circuits.