B. Tech.

THIRD SEMESTER EXAMINATION, 2009-10

Analog and Digital Electronics (EEC-309)

Time : 3 Hours **Total Marks : 100**

Note : Attempt all questions. All questions carry equal marks.

Q. 1. Attempt any four parts of the following :

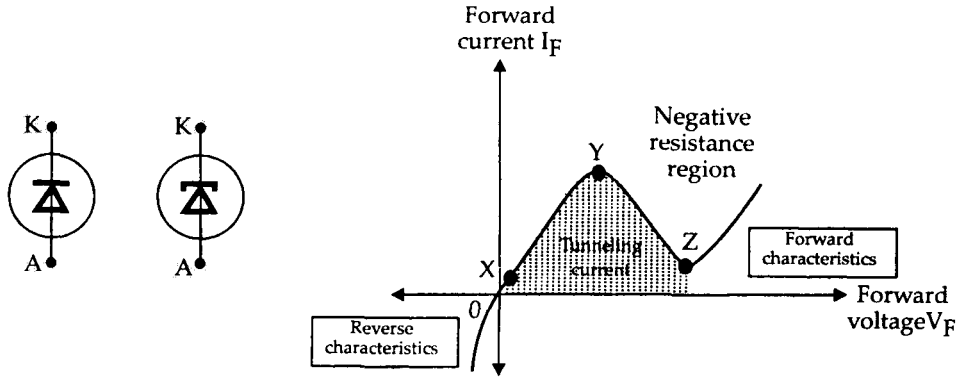
(a) Draw the V-1 characteristics of tunnel diode and indicate the useful region in the curve.

Ans. Tunnel Diode Characteristics :

The voltampere characteristics of a tunnel diode is shown in Fig.(b) and its symbols are shown in Fig.(a).

Reverse characteristics :

1. Due to heavy doping of p and n sides, the depletion region is extremely narrow when the tunnel diode is reverse biased.



(a) Circuit symbols of tunnel diode **(b) Volt-ampere characteristics of a tunnel diode**

2. Therefore the reverse blocking capacity of the junction is lost and reverse current will start flowing as soon as a very small reverse voltage is applied.
3. Thus the tunnel diode allows the conduction to take place for all the reverse voltages. There is no breakdown effect as observed in the conventional rectifier diode.
4. Therefore we can not use the tunnel diode as a rectifier.

Forward characteristics :

- Forward characteristics can be divided into three regions namely X to Y, Y to Z and Z onwards.
- **Region X to Y :** In this region the forward voltage V_F is extremely small. But heavy conduction will take place in this region because electrons "tunnel" through the pn junction. The "tunneling" takes place as a result of heavy doping.

Q.1. (b) Draw the output characteristics of transistor. How it is used as a switch ?

Ans. Transistor in cutoff region (Transistor as an open switch) :

In the cutoff region both the junctions of a transistor are reverse biased and a very small reverse current flows through the transistor.

The voltage drop across the transistor (V_{CE}) is high. Thus in the cutoff region the transistor is equivalent to an open switch.

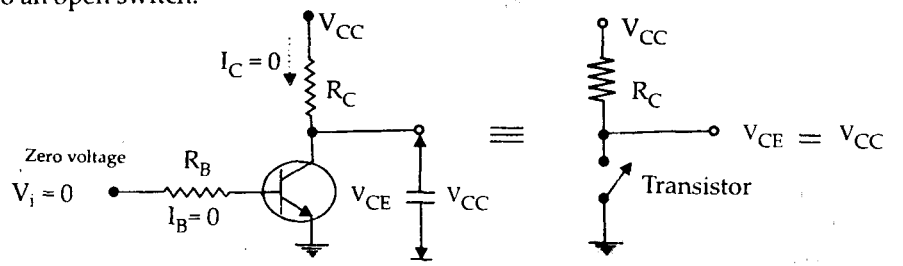


Fig. : Transistor in cutoff is equivalent to an open switch

The input voltage is zero so $I_B = 0$ and $I_C = 0$.

Applying KVL to the collector circuit of Fig. we get,

$$V_{CC} = I_C R_C + V_{CE}$$

But $I_C = 0$

$\therefore$ $V_{CE} = V_{CC}$

The voltage across the transistor is $V_{CE} = V_{CC}$ i.e., high and the current flowing through it $I_C = 0$. This shows that the resistance offered by the transistor is infinite and the transistor operates as an open switch.

Thus in the cut off region, the transistor acts as an open switch as shown in Fig.

(ii) Transistor in the saturation region (Transistor as closed switch) :

Fig. shows the biasing of transistor in the saturation region. A high input voltage V_{in} is applied at the base.

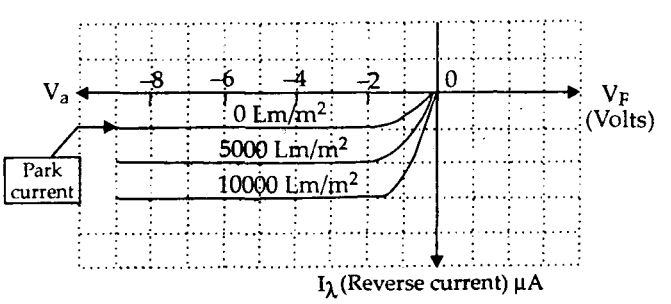
The value of V_{in} and resistance R_B are adjusted such that a large I_B flows. This will saturate the transistor. The value of I_B should be such that the following condition should be satisfied.

$$I_B \geq \frac{I_{C\,(sat)}}{\beta}$$

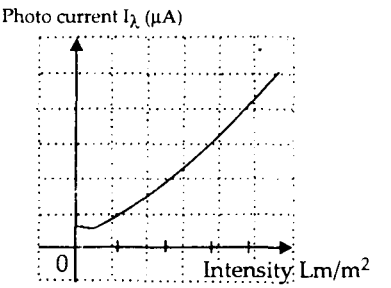
In the saturation region both the junctions of a transistor are forward biased. The voltage drop across the transistor (V_{CE}) is very small of the order of 0.2V to 1V depending on the type of transistor and collector current is very large.

Q.1. (c) Describe the characteristics and application of photo-diode.

Ans. Photo-diode Characteristics :



(a) V-I characteristics of a photodiode



(b) Variation of photocurrent with intensity of light

The photodiode V-I characteristics are as shown in Fig. (a) and the variation of photo current with light intensity is as shown in Fig.(b).

Dark current : It is the current flowing through a photodiode in the absence of light (See Fig. **(a)**). Dark current flows due to the thermally generated minority carriers, and hence increases with increase in temperature. Dark current should be as low as possible.

The reverse current I_λ (photocurrent) depends only on the intensity of light incident on the junction. It is almost independent of the reverse voltage.

Applications of Photodiode

A popular application of the photodiode is an object counting system shown in Fig.

This system is used for counting the number of objects that are passing on a conveyer belt.

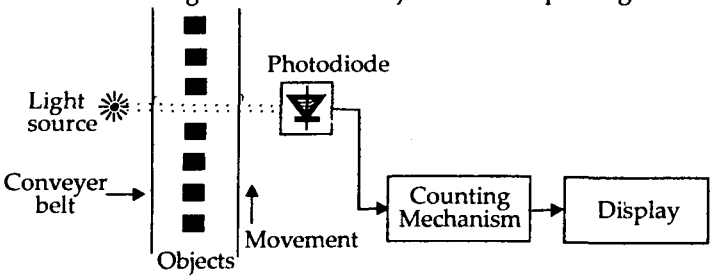


Fig. : Object counting system using photodiode

A light beam is focussed continuously on the photodiode and the reverse photocurrent is flowing through it.

As soon as an object passes and interrupts the beam of light, the photocurrent flowing through the photodiode will reduce to zero.

Q.1. (d) An LED is connected across a voltage source of + 10V through a series resistance of 820 Ω. Calculate the LED current. Assume the voltage drop across an LED of 1.5 volt.

Ans. LED is connected across + 10V.

Series Resistance = 820 Ω

Voltage drop LED = 1.5 V

LED current $I_D = ?$

$$I_D = \frac{10 - 1.5}{820}$$

$$I_D = 10.36 \text{ mA}$$

Q.1. (e) Explain the working of tunnel diode. Give its two applications.

Ans. Tunnel Diode :

The operation of a tunnel diode is based on a special characteristic known as the negative resistance.

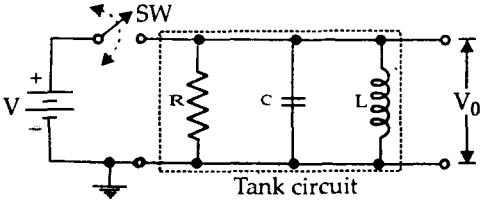
The semiconductor materials used for constructing the tunnel diodes are Germanium or Gallium Arsenide.

Construction of a tunnel diode is similar to that of a p-n junction diode but both p and n sides are very heavily doped, than the conventional rectifier diodes.

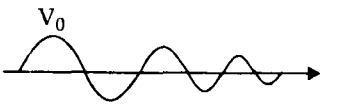
The heavy doping of both the sides of junction results in extremely narrow depletion region when the tunnel diode is reverse biased. This is shown in the tunnel diode characteristics of Fig. (b).

Application of Tunnel Diode as an Oscillator :

1. Fig. (a) shows a parallel resonant circuit which is also called as the tank circuit.
2. If the switch SW is closed momentarily, then a current pulse is applied to the tank circuit.
3. The capacitor charges and discharges sinusoidally to produce damped oscillations across the tank circuit as shown in Fig.(b).



(a) Tank circuit



(b) Damped oscillations across the tank circuit

4. The frequency of the damped oscillations is fixed and it is decided by the RLC components but the amplitude decreases as the time progresses.

Q.1. (f) Why photodiode is used in reverse bias conditions ? Give any two applications of it.

Ans. Why is the photodiode Operated in Reverse Biased Condition :

In the reverse biased condition the only current flowing through the diode in absence of light is the reverse saturation current which is very small in magnitude.

Hence the change in diode current due to the light incident on it, is significant, (photocurrent is in μA).

If the diode were forward biased then the forward current in absence of light would be in mA and the change in forward current due to light will not even be noticeable.

Hence the photodiode is operated in the reverse biased condition.

Application of Photodiode :

1. In the camera for sensing the light intensity.
2. In fibre optic meters.

Q.2. Attempt any four parts of the following :

(a) An amplifier has a midband gain of 1500 and a bandwidth of 4.0 MHz, the midband gain reduces to 150 when a negative feedback is applied. Determine the value of feedback factor and Bandwidth.

Ans. midband gain A = 1500

band width Bw = 4.0 MHz

when the negative feedback is applied then the midband gain Af(mid) = 150

$$A_f(\text{mid}) = \frac{A\,mid}{1 + Amid\,.\,\beta}$$

$$150 = \frac{1500}{1+1500\times\beta}$$

$$\beta = 150$$

$$150 + 150 \times 1500 \times \beta = 1500$$

$$\beta = \frac{1500 - 150}{150 \times 1500}$$

$$\beta = \frac{1350}{150 \times 1500}$$

$$\beta = \frac{3}{500}$$

Band width A_f / *cr* feedback = $Bw \times (1 + BA)$

$$= 4.0 \times 10^6 (1 + 150 \times \frac{3}{500})$$

$$= 4.0 \times 10^6 \times 10$$

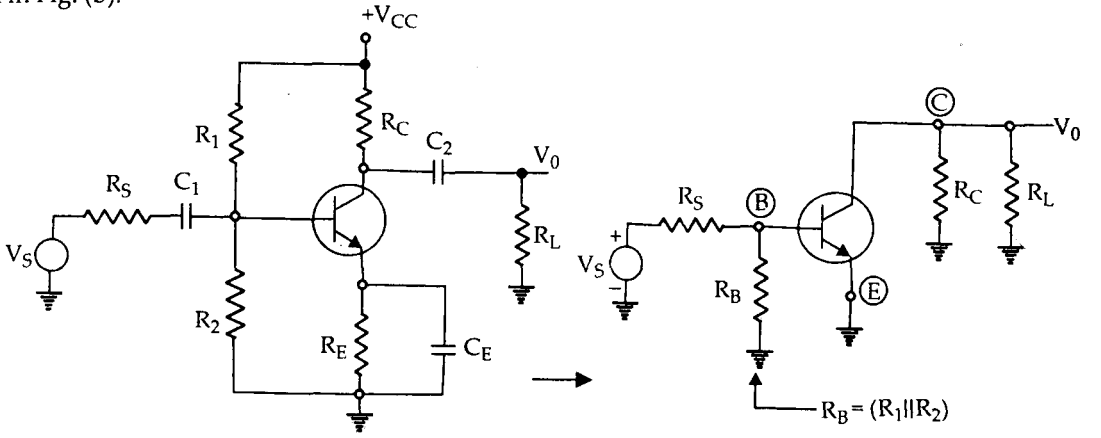
$$= 40 \text{ MHz.}$$

Q.2. (b) Draw the high frequency equivalent circuit for the typical RC coupled common emitter amplifier.

Ans. High frequency equivalent circuit of Common Emitter Amplifier :

Step 1: draw the ac equivalent circuit :

The ac equivalent circuit, obtained by replacing all the dc sources and capacitors by short circuit is shown in Fig. (b).



(a) CE amplifier with bypassed R_E **(b) AC equivalent circuit**

Step 2 : Draw the hybrid-π equivalent circuit :

Replace the transistor in ac equivalent circuit by the hybrid π equivalent circuit as shown in Fig.

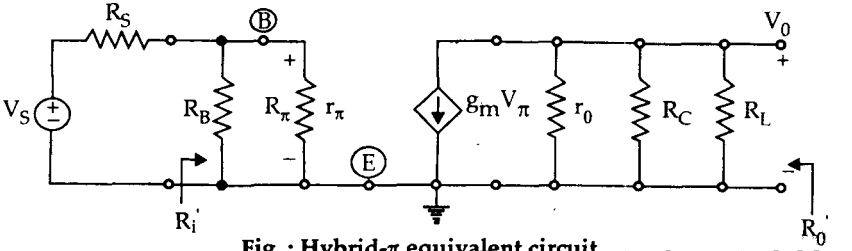


Fig. : Hybrid-π equivalent circuit

Q.2. (c) Explain the effect of negative feedback on various characteristics of the amplifier.

Ans. Effect of Negative feedback :

(1) Reduce the voltage gain

$$A_f = \frac{A}{1 + A\beta}$$

the feedback gain A_f Reduce by factor $(1 + A\beta)$

(2) Improve the stability of system.

(3) Reduce the noise by factor $(1+\beta A)$.

(4) Reduce the distortion by factor $(1+\beta A)$.

(5) Improve the Bandwidth Band width $Bw = f_H - f_L$

after Negative feedback

$$f_{Hf} = (1 + \beta A) . f_H$$

and

$$f_{Lf} = \frac{f_L}{(1+\beta A)}$$

the Band width alter Negative feedback

$$= f_{Hf} - f_{Lf}$$

$$= (1 + \beta A) . f_H - \frac{1}{(1+\beta A)} . f_L$$

Q.2. (d) An RC coupled amplifier has a voltage gain of 1000, $f_1 = 50 Hz$, $f_2 = 200\ kHz$ and a distortion of 5% without feedback. Find the amplifier voltage gain, f'_1, f'_2 and distortion when negative feedback is applied with feedback ratio of 0.01.

Ans. Voltage gain A = 1000,

$$f_1 = f_L = 50\ Hz, \quad f_2 = f_H = 200\ kHz$$

feedback Ratio $\frac{A_f}{A} = 0.01$

$$A_f = \frac{A}{(1 + \beta A)}$$

$$\frac{A_f}{A} = \frac{1}{(1+A\beta)} = 0.01$$

$$(1+A\beta) = \frac{1}{0.01} = 100$$

we know $f_{Lf} = \frac{f_L}{(1 + A\beta)}$

$$f'_1 = f_{Lf} = \frac{50}{100} = 0.5\ \text{Hz}$$

$$f'_2 = f_{Hf} = 200 \times 10^3\ Hz \times (1 + A\beta)$$

$$= 200 \times 10^3 \times 100$$

$$= 20000 \times 10^3$$

$$f'_2 = 20\ \text{MHz}$$

Q.2. (e) Calculate the voltage gain, input and output resistances of a voltage series feedback amplifier having

$$A_v = 300,\ R_i = 1.5\ k\Omega,\ R_o = 50k\Omega \text{ and } \beta = \frac{1}{15}$$

Ans. For voltage series feedback

$$\text{Avf} = \frac{AV}{1 + A_v\beta}$$

$$\phi = \frac{300}{1 + 300 \times \frac{1}{15}} = \frac{300}{21}$$

voltage gain Avf = 14.28

Input Resistance $R_{Lf} = R_L \times (1 + A_v\beta)$

$$= 1.5 \times 10^3 \times (1 + 300 \times \frac{1}{15})$$

$$= 1.5 \times 10^3 \times 21$$

$$= 31.5 k\Omega$$

Output Resistance $Ro_f = \frac{R_o}{1 + A_v\beta}$

$$= \frac{50 \times 10^3}{1 + 300 \times \frac{1}{15}} = \frac{50 \times 10^3}{21}$$

$$Ro_f = 2.38 k\Omega$$

Q.2. (f) Describe the properties of series-shunt and shunt-shunt feedback amplifier.

Ans. Proportions of Series–Shunt and Shunt–Shunt feedback :

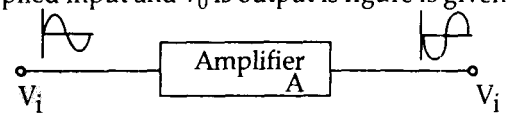
Sr. No.	Topology Characteristics	Series shunt (1)	Shunt shunt (4)
1.	Feedback signal (X_f)	Voltage	Current
2.	Sampled signal (X_0)	Voltage	Voltage
3.	To find input loop, set	$V_0 = 0$	$V_0 = 0$
4.	To find output loop, set	$I_i = 0$	$V_i = 0$
5.	Signal source	Thevenin	Norton
6.	$\beta = \frac{X_f}{X_0}$	$\frac{V_f}{V_0}$	$\frac{I_f}{V_0}$
7.	$A = \frac{X_0}{X_i}$	$A_V = \frac{V_0}{V_i}$	$R_M = \frac{V_0}{I_i}$
8.	$D = 1 + \beta A$	$1 + \beta\ A_V$	$1 + \beta\ R_M$
9.	A_f	$\frac{A_V}{D}$	$\frac{R_M}{D}$

10.	R_{if}	$R_i D$	R_i / D
11.	R_{of}	$\frac{R_o}{1+\beta A_V}$	$\frac{R_o}{1+\beta R_m}$
12.	$R'_{of} = R_L \parallel R_{of}$	$\frac{R'_o}{D}$	$\frac{R'_o}{D}$

Q.3. Attempt any two parts of the following :

(a) What is Barkhausen criterion for the Feedback oscillator ? Draw a neat diagram of a phase-shift oscillator using BJT. Derive an expression for its frequency of oscillation.

Ans. Barkhausen criterion : This is simple amplifier with gain A, the other with feedback Network attenuation factor β . V_i is applied input and V_0 is output is figure is given—

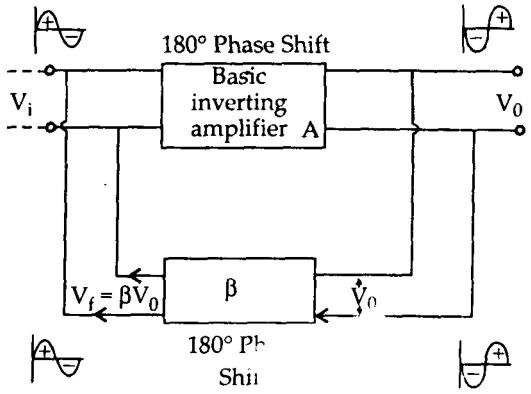


Interting amplifier

$\therefore$ $V_0 = AV_i$ ...(1)

in feedback Network $V_f = \beta V_0$

than $V_f = A\beta V_i$ ...(2)



For the oscillator.

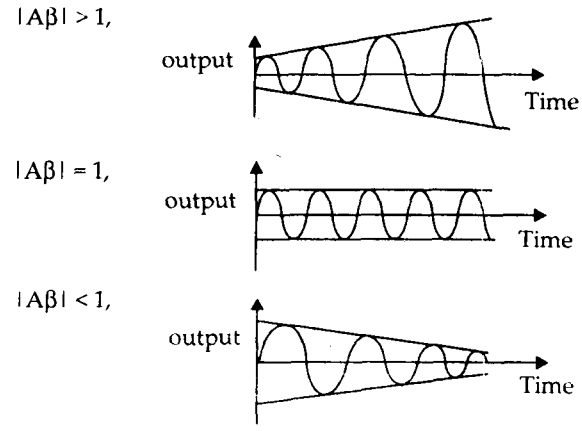
$$|A\beta| = 1$$

the phase of V_f is come as V_i i.e feedback Network should introduce 180° phase shift in addition to 180°. 180° Phase shift introduce by inverting amplifier thus the total Phase shift 360°.

Barkhausen Criterion States that

1. The total phase shift around a loop as the signal proceeds from input through amplifier, feedback Network back to input again, completing a loop is precisely 0° or 360°.

2. The magnitude of the product of **the open loop gain of amplifier (A)** and **Magnitude of the feedback factor** β is unity i.e. $|A\beta| = 1$

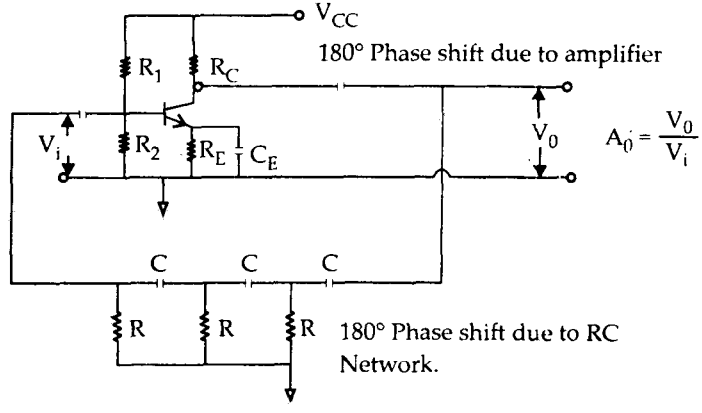


If any circuit works as an oscillator producing sustained oscillation of constant frequency and amplitude.

By using the proper value of R and C angle ϕ practice equal to 60°.

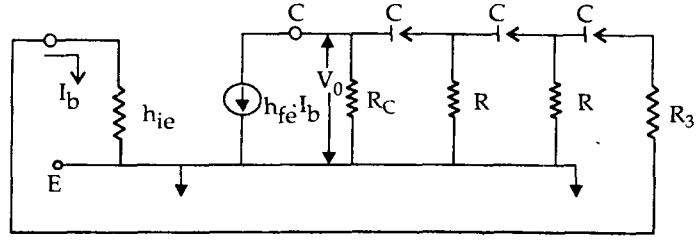
$$V_O = IR \qquad V_C = IV_C$$

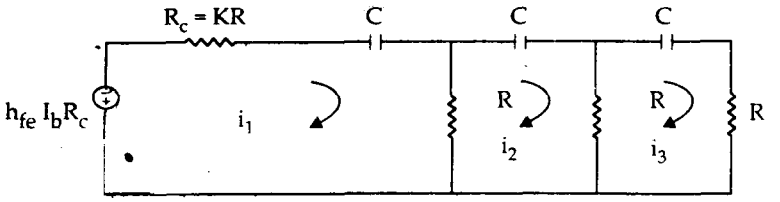
Phase Shift oscillator by using Transistor and it derivation : The given Network consist 3 RC Section each producing 60° phase shift and BJT is used here the total phase shift around the loop is 360°. This is sufficient condition for positive feedback and for oscillator.



Let's analysis of frequency, amplitude, open loop gain, closed loop gain etc.

We replace the transistor modal in h-parameter modal.





we can Put $R = h_{ie} + R_3$ ...(1)

we can not Neglect the Transistor R_1 and R_2

so, $R_1' = R_1 \| R_2 \| h_{ie}$

and we can put also $K = \frac{RC}{R}$

$\Rightarrow$ $R_G = KR$ ...(2)

the modified circuit of oscillator–

applying KVL in all the loops and find-

$$-h_{fe} I_b R_c - i_1 KR - \frac{i_1}{i\omega_c} - L_1 R + L_2 R = 0$$

Put $\omega_c = S_c$

$$+ i_1 \left[(K+1)R + \frac{1}{SC} \right] - I_2 R = -h_{fe} I_b R_c \quad ...(3)$$

loop (2)

$$-\frac{i_2}{i\omega c} - i_2 R + i_3 R - i_2 R + i_1 R = 0$$

$$-i_1 R + i_2 \left[\frac{1}{SC} + 2R \right] - i_3 R = 0 \quad ...(4)$$

in loop (3)

$$-\frac{i_3}{i\omega c} - i_3 R - i_3 R + i_2 R = 0$$

$$-i_2 R + i_3 \left[2R + \frac{1}{SC} \right] = 0 \quad ...(5)$$

using Cramer's rule to Solve the current

$$D = \begin{vmatrix} (K+1) + \frac{1}{SC} & -R & 0 \\ -R & 2R + \frac{1}{SC} & -R \\ 0 & -R & 2R + \frac{1}{SC} \end{vmatrix}$$

$$= \left[(K+1)R + \frac{1}{SC} \right] \left[2R + \frac{1}{SC} \right]^2 - R^2 \left[(K+1)R + \frac{1}{SC} \right] - R^2 \left[2R \frac{1}{SC} \right]$$

by solving this we will find–

$$D = \frac{S^3C^3K^3(3K+1) + S^2C^2R^2(4K+6) + SRC(S+K) + 1}{S^3C^3}$$

$$D_3 = \begin{vmatrix} (K+1)+\frac{1}{SC} & -R & -h_{fe} I_B R_C \\ -R & 2R+\frac{1}{SC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$D_3 = -R^2 (h_{fe}\ I_b\ KR)$$

$$D_3 = -KR^3\ h_{fe}\ I_b$$

than $$I_3 = \frac{D_3}{D}$$

$$I_3 = \frac{-KR^3 h_{fe} I_b}{S^3C^3R^3(3K+1)+S^2C^2R^2(4K+6)+SCR(5K+1)+1}$$

$I_3 \rightarrow$ output current of the feedback

$I_b \rightarrow$ input current of the amplifier

$I_c \rightarrow h_{fe} I_b \rightarrow$ input current of the beedback circuit

$$\beta = \frac{\text{out of feedback}}{\text{input of feedback}} = \frac{I_3}{h_{fe} I_b}$$

$$A = \frac{\text{output of amplifier}}{\text{input of amplifier}} = \frac{I_3}{I_b} = h_{fe}$$

$$A\beta = \frac{I_3}{h_{fe} I_b} \times h_{fe} = \frac{I_3}{I_b}$$

$$A\beta = \frac{-KR^3 h_{fe} \times C^3S^3 \times I_b}{[S^3C^3R^3(3K+1)+S^2C^2R^2(4K+6)+SCR(SK+1)+1] \times I_b}$$

Substituting $S = i\omega$, $S^2 = -\omega^2$, $S^3 = -i\omega^3$ in the above equation

$$A\beta = \frac{-i\omega^3 KR^3C^3h_{fe}}{[i\omega^3C^3R^3(3K+1)-\omega^2C^2R^2(4K+6)+i\omega CR(SK+1)+1]}$$

Separating real and imaginary part

$$A\beta = \frac{-i\omega^3 KR^3C^3h_{fe}}{[1-4K\omega^2C^2R^2-6\omega^2C^2R^2]-i\omega(3K\omega^2R^3C^3+\omega^2R^3C^3-5RC-KRC]}$$

Dividing Nomirator and Denominator by

$i\omega^3R^3C^3$, and Replacing $-\frac{1}{i} = i$

$$A\beta = \frac{Kh_{fe}}{i\left[\frac{1}{\omega^3R^3C^3}-\frac{4K}{\omega RC}-\frac{6}{\omega RC}\right]+\left[3K+1-\frac{5}{\omega^2R^2C^2}-\frac{K}{\omega^2R^2C^2}\right]}$$

for Simplicity Putting $\alpha = \frac{1}{\omega RC}$

$$A\beta = \frac{K h_{fe}}{[3K+1-5\alpha^2-K\alpha^2]+i[\alpha^3-4K\alpha-6\alpha]}$$

As per Barkhausen criterion $\angle A\beta = 0°$ so Put the imaginary part equal to zero.

$$\alpha^3 - 4K\alpha - 6\alpha = 0$$

$$\alpha[\alpha^2 - 4K - 6] = 0$$

$$\alpha^2 - 4K - 6 = 0$$

$$\alpha^2 = 4K + 6$$

$$\alpha = \sqrt{4K=6}$$

$$\frac{1}{\omega RC} = \sqrt{4K+6}$$

$$\boxed{\omega = \frac{1}{RC\sqrt{4K+6}}}$$

$$\boxed{f = \frac{1}{2\pi RC\sqrt{4K+6}}}$$

$\angle A\beta = 0°$ But $(A\beta) = 1$, than

$$A\beta = \frac{Kh_{fe}}{3K+1-(4K+6)(5+K)}$$

$$A\beta = \frac{Kh_{fe}}{-4K^2-23K-29}$$

$|A\beta| = 1$, then

$$1 = \left|\frac{kh_{fe}}{-4K^2-23K-29}\right|$$

$$Kh_{fe} = 4K^2+23K+29$$

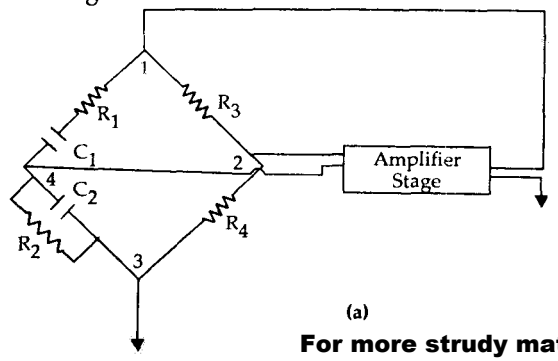
$$\boxed{h_{fe} = 4K+23+\frac{29}{K}}$$

this is value of h_{fe} for oscillation.

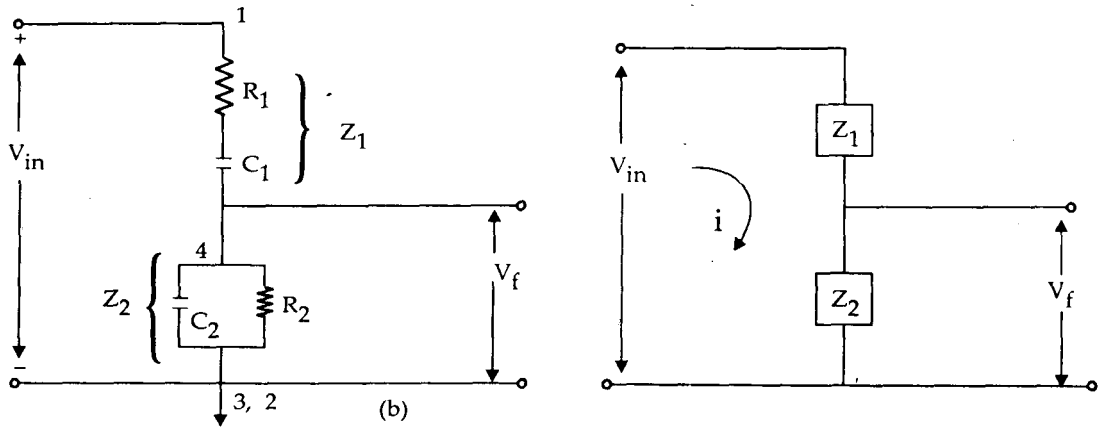
Q.3. (b) Explain the working of Wein-bridge oscillator. Derive formula for the frequency of oscillation.

Ans. Wein Bridge oscillator :

In wein Bridge oscillator Non-inverting amplifier used and total 360° phase shift done by basic circuit of wien Bridge oscillator the figure Shown the basic circuit-



(a)



The output of amplifier is applied between the Terminal 1,3, which is the input to the feedback network. In the figure (b) R_1 and C_1 is in the series and R_2 and C_2 are in parallel these two arm called frequency sensitive arm.

Description of frequency of oscillation :

from the figure $$Z_1 = R_1 + \frac{1}{i\omega C_1} = \frac{1 + i\omega R_1 C_1}{i\omega C_1}$$

Replace $i\omega = S$

$$Z_1 = \frac{1 + S R_1 C_1}{S C_1}$$

$$Z_2 = R_2 \| \frac{1}{i\omega_2} = \frac{R_2}{1 + i\omega C_2 R_2} = \frac{R_2}{1 + S C_2 R_2}$$

in the figure

$$I = \frac{V_{in}}{Z_1 + Z_2} \quad \text{and } V_f = IZ_2$$

$$V_f = \frac{V_{in}\, Z_2}{Z_1 + Z_2}$$

and $$\beta = \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1 + Z_2}$$

$$\beta = \frac{\left[\frac{R_2}{1 + S R_2 C_2}\right]}{\left[\frac{1 + S R_1 C_1}{R_1}\right] + \left[\frac{R_2}{1 + S R_2 C_2}\right]}$$

$$\beta = \frac{S C_1 R_1}{1 + S(R_1 C_1 + R_2 C_2 + C_1 R_2) + S^2 R_1 R_2 C_1 C_2}$$

putting $S = i\omega$ then

$$\beta = \frac{i\omega C_1 R_1}{(1-\omega^2 R_1 R_2 C_1 C_2)+i\omega(R_1 C_1 + R_2 C_1 + C_1 R_2)}$$

Rationalizing the expression.

$$\beta = \frac{i\omega C_1 R_2[(1-\omega^2 R_1 R_2 C_1 C_2)-i\omega(R_1 C_1 + R_2 C_2 + C_1 R_2)]}{(1-\omega^2 R_1 R_2 C_1 C_2)^2+\omega^2(R_1 C_1 + R_2 C_2 + C_1 R_2)}$$

$$\beta = \frac{i\omega[(1-\omega^2 R_1 R_2 C_1 C_2)+\omega^2(R_1 C_1 + R_2 C_2 + C_1 R_2)]C_1 R_2}{(1-\omega^2 R_1 R_2 C_1 C_2)+\omega^2(R_1 C_1 + R_2 C_2 + C_1 R_2)}$$

to phase shift equal to zero, Put imaginary part equal to zero

$$\omega(1-\omega^2 R_1 R_2 C_1 C_2) = 0$$

$$\omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\boxed{f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}}$$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$$f = \frac{1}{2\pi RC}$$

and

$$\beta = \frac{\omega^2 RC(3RC) + i\omega RC(1-\omega^2 R^2 C^2)}{(1-\omega^2 R^2 C^2)^2+\omega^2(3RC)^2}$$

Putting $f = \frac{1}{2\pi RC}$ or $\omega = \frac{1}{RC}$

$$\beta = \frac{\frac{1}{(RC)^2}\times RC\times 3RC + i\omega RC\left(1-\frac{1}{(RC)^2}R^2C^2\right)}{\left(1-\frac{1}{(RC)^2}\times R^2C^2\right)+\frac{1}{(RC)^2}\times(3)^2\times R^2C^2}$$

$$\beta = \frac{3+0}{0+9} = \frac{3}{9} = \frac{1}{3}$$

$$\boxed{\beta = \frac{1}{3}}$$

by Barkhausen criterion $|A\beta| \geq 1$

$$|A| \geq \frac{1}{|\beta|} \geq \frac{1}{(1/3)}$$

$$\boxed{|A| \geq 3}$$

If $R_1 \neq R_2$ and $C_1 \neq C_2$ than

$$\boxed{f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}}$$

$$\boxed{\beta = \frac{C_1 R_2}{(R_1 C_1 + R_2 C_2 + C_1 R_2)}}$$

Q.3. (c) A Colpitt's oscillator is designed with C_1 = 100 pf and C_2 = 7500 pf. The inductance is variable.

Determine the range of inductance values, if the frequency of oscillation is to vary between 950 kHz and 2050 kHz ?

Ans. In Colpitt oscillator

$$C_1 = 100\,\text{pf and } C_2 = 7500\,\text{pf}$$

the frequency of oscillation is vary to 950 KHz to 2050 KHz.

$$f = \frac{1}{2\pi\sqrt{L\frac{C_1 \cdot C_2}{C_1 + C_2}}}$$

$$\frac{C_1 \cdot C_2}{C_1 + C_2} = \frac{100\,\text{PF} \times 7500\,\text{PF}}{100\,\text{PF} + 7500\,\text{PF}} = \frac{100\,\text{PF} \times 7500\,\text{PF}}{7600\,\text{PF}}$$

$$= 98.68\,\text{PF}$$

L_1 when f is 950×10^3 Hz,

$$950 \times 10^3 = \frac{1}{2\pi\sqrt{L_1 \times 98.68\,\text{PF}}}$$

$$\sqrt{L_1 \times 98.68 \times 10^{-12}} = \frac{1}{2\pi \times 950 \times 10^3}$$

$$L_1 \times 98.68 \times 10^{-12} = \frac{1}{4\pi^2 \times 950 \times 950 \times 10^6}$$

$$L_1 = \frac{1}{98.68 \times 10^{-12} \times 4\pi^2 \times 950 \times 950 \times 10^6}$$

$$L_1 = 2.85 \times 10^{-4}\,\text{H}$$

L_2 when f = 2050 KHz

$$2050 \times 10^3 = \frac{1}{2\pi\sqrt{L_2 \times 98.68 \times 10^{-12}}}$$

$$\sqrt{L_2 \times 98.68 \times 10^{-12}} = \frac{1}{2050 \times 10^3 \times 2\pi}$$

$$L_2 \times 98.68 \times 10^{-12} = \frac{1}{2050 \times 2050 \times 10^6 \times 4\pi^2}$$

$$L_2 = \frac{1}{2050 \times 2050 \times 10^6 \times 4\pi^2 \times 98.68 \times 10^{-12}}$$

$$L_2 = 6.10 \times 10^{-5}\,\text{H}$$

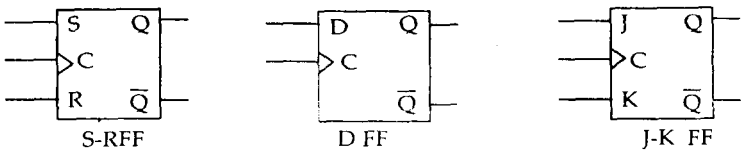
the inductance range will vary 2.85×10^{-4}H to 6.10×10^{-5}H.

Q.4. Attempt any two parts of the following :

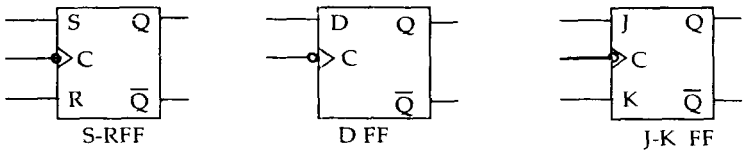
(a) What do you mean by flip-flops ? Describe the edge triggered flip-flops. Convert SR flip-flops into JK flip-flops.

Ans. The flip-flops using the clock signal are called the clocked flip-flops. Control signals are effective only if they are applied in synchronization with the clock signal. The clock signal is distributed

to all parts of the system and most of the system outputs can change state only when the clock makes a transition. Clocked flip-flops may be positive edge-triggered or negative edge-triggered. Positive edge-triggered flip-flops are those in which 'state transitions' take place only at the positive-going (0 to 1, or LOW to HIGH) edge of the clock pulse and negative edge-triggered flip-flops are those in which 'state transitions' take place only at the negative-going (1 to 0, or HIGH to LOW) edge of the clock signal. Positive-edge triggering is indicated by a 'triangle' at the clock terminal of the flip-flop. Negative-edge triggering is indicated by a 'triangle' with a bubble at the clock terminal of the flip-flop. Thus edge-triggered flip-flops are sensitive to their inputs oniy at the transition of the clock. flip flops : S-R, J-K, and D (a). Of these, D and J-K flip-flops are the most widely used ones and readily available in the IC form than is the S-R type. But the S-R flip-flop is also covered here because it is a good base upon which to build both the D and the J-K flip-flops, having been derived from the S-R flip-flop. The edge-triggeringis also called dynamic triggering



(a) Logic symbols of positive edge-triggered FFs



(a) Logic symbols of negative edge-triggered FFs

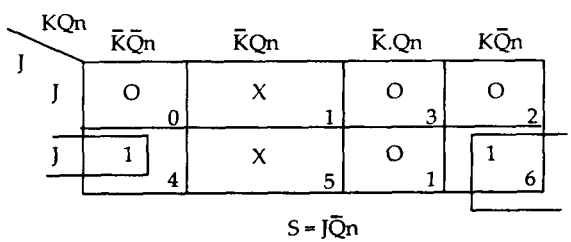
Fig.(a) Edge-triggered flip-flops

Conversion of SR Flip-Flop into JK Flip Flop :

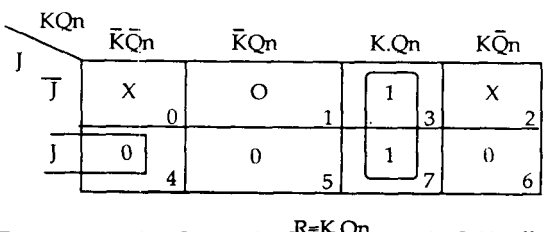
Conversion Table

J-K input		Outputs		S-R inputs	
J	**K**	Q_n	Q_{n+1}	**S**	**R**
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

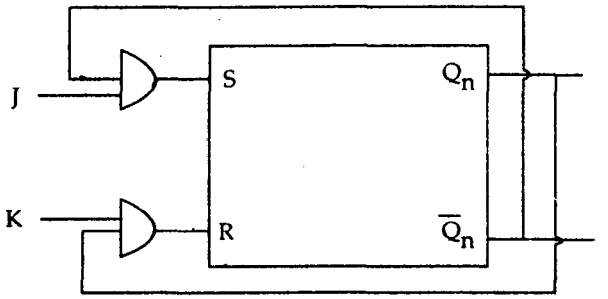
Kmap for S-R



$S = J\bar{Q}n$



$R = KQn$



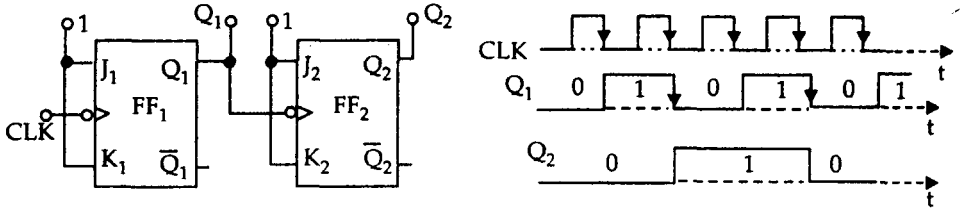
(c) Logic diagram

Q.4. (b) Implement the boolean function using 8:1 multiplexer.

$$F(A,B,C,D)=\overline{A}B\overline{D}+ACD+\overline{B}CD+\overline{A}\overline{C}D$$

Describe the working of counter.

Ans. Working of Counters : The 2-bit up-counter counts in the order 0, 1, 2, 3, 0, 1,...., i.e. 00, 01, 10, 11, 00, 01,....,etc. Figure shows a 2-bit ripple up-counter, using negative edge-triggered J-K FFs, and its timing diagram. The counter is initially reset to 00. When the first clock pulse is applied, FF_1 toggles at the



(a) Logic diagram (b) Timing diagram

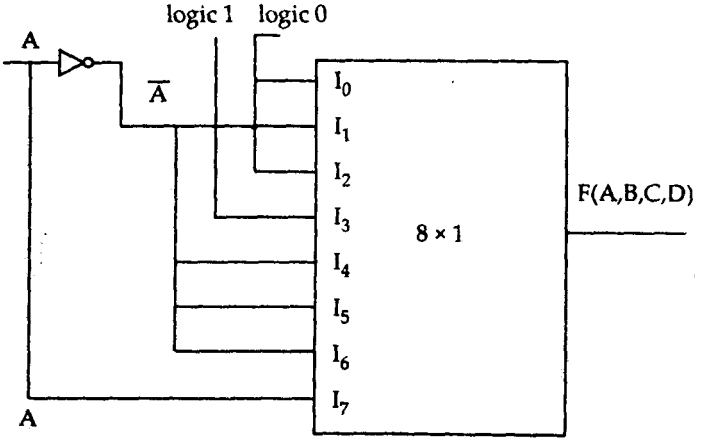
negative-going edge of this pulse, therefore, Q_1 goes from LOW to HIGH. This becomes a positive-going signal at the clock input of FF_2. So, FF_2 is not affected, and hence, the state of the counter after one clock pulse is $Q_1 = 1$ and $Q_2 = 0$, i.e. 01. At the negative-going edge of the second clock pulse, FF_1 toggles. So, Q_1 changes from HIGH to LOW and this negative going signal applied to CLK of FF_2 activates FF_2, and hence, Q_2 goes from LOW to HIGH. Therefore, $Q_1 = 0$ and $Q_2 = 1$, i.e. 10 is the state of the counter after the second clock pulse. At the negative-going edge of the third clock pulse, FF_1 toggles, so, Q_1 changes from a 0 to a 1. This becomes a positive-going signal to FF_2, hence, FF_2 is not affected. Therefore, $Q_2 = 1$ and $Q_1 = 1$, i.e. 11 is the state of the counter after the third clock pulse. At the negative-going edge of the fourth clock pulse, FF_1 toggles. So, Q_1 goes from a 1 to a 0. This negative-going signal at Q_1 toggles FF_2, hence, Q_2 also changes from a 1 to a 0. Therefore, $Q_2 = 0$ and $Q_1 = 0$, i.e. 00 is the state of the counter after the fourth clock pulse. For subsequent clock pulses, the counter goes through the same sequence of states. So, it acts as a mod-4 counter with Q_1 as the LSB and Q_2 as the MSB. The counting sequence is thus 00, 01, 10, 11, 00, 01,....etc.

$$F(A,B,C,D)=\overline{A}B\overline{D}+ACD+\overline{B}CD+\overline{A}\overline{C}D$$
$$=\overline{A}B\overline{D}(C+\overline{C})+ACD(B+\overline{B})+\overline{B}CD(A+\overline{A})+\overline{A}\overline{C}D(B+\overline{B})$$
$$=\overline{A}BC\overline{D}+\overline{A}B\overline{C}\overline{D}+ABCD+A\overline{B}CD+A\overline{B}CD+\overline{A}\overline{B}CD+\overline{A}B\overline{C}D+\overline{A}\overline{B}\overline{C}D$$

in minterm $= 0110 + 0100 + 1111 + 1011 + 0011 + 0101 + 0001$

K-map form $\sum m(1,3,5,6,4,11,15)$

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\overline{A}$	0	(1)	2	(3)	(4)	(5)	(6)	7
A	8	9	10	(11)	12	13	14	(15)
	0	$\overline{A}$	0	1	$\overline{A}$	A	$\overline{A}$	A



Q.4. (c) Draw and explain the working of 4-bit up and down synchronous counter. Also describe the working of shift register.

Ans. Four-bit Synchronous Up/Down Counter :

A 4-bit synchronous up/down counter can be obtained by combining the up-counting and down-counting operations in a single counter using control or mode signal. Let us say, we want the counter to count up when mode signal M = 1 and count down when mode signal M = 0. We can obtain the expressions for excitations of an up/down counter by combining the excitations of up- and down-counters using the mode signal. Therefore, the design equations for an up/down counter are;

$$J_1 = K_1 = 1$$

$$J_2 = K_2 = (Q_1 \cdot U_p) + (\overline{Q}_1 \cdot Down) = Q_1 M + \overline{Q}_1 \overline{M}$$

$$J_3 = K_3 = (Q_1 \cdot Q_2 \cdot U_p) + (\overline{Q}_1 \cdot \overline{Q}_2 \cdot Down) = Q_1 Q_2 M + \overline{Q}_1 \overline{Q}_2 M$$

$$J_4 = K_4 = (Q_1 \cdot Q_2 \cdot Q_3 \cdot U_p) + (\overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot Down) = Q_1 Q_2 Q_3 M + \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{M}$$

The logic diagram of a 4-bit synchronous up/down counter is shown in Fig. Most up/down counters can be reversed at any point in the sequence.

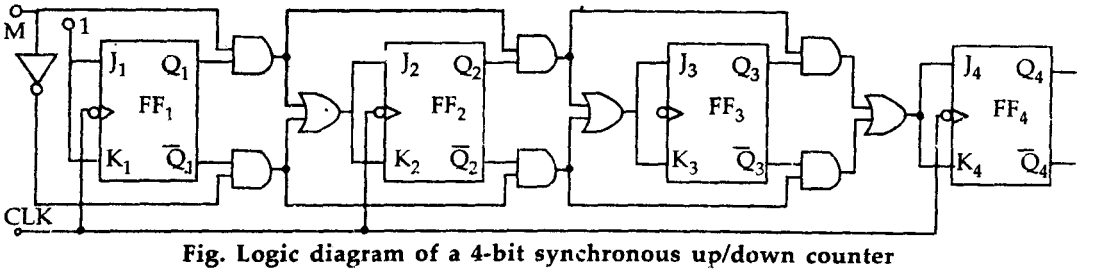
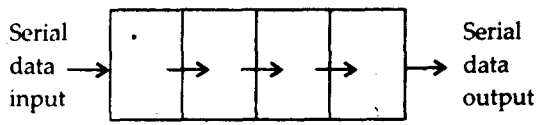


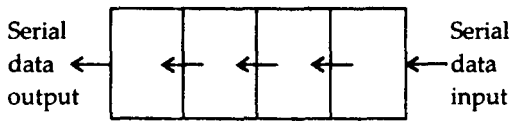
Fig. Logic diagram of a 4-bit synchronous up/down counter

Working of Shift Register :

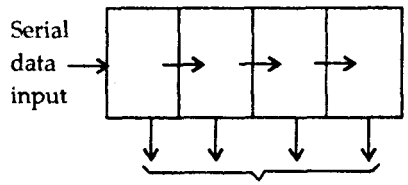
A number of FFs connected together such that data may be shifted into and shifted out of them is called a shift register. Data may be shifted into or out of the register either in serial form or in parallel form. So, there are four basic types of shift registers: serial-in, serial-out; serial-in, parallel-out; parallel-in, serial-out; and parallel-in, parallel-out. The process of data shifting in these registers is illustrated in Fig. All of these



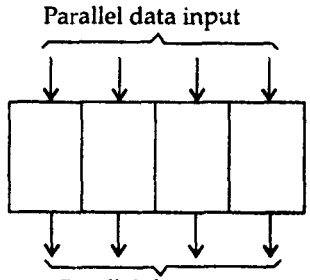
(a) Serial-in, serial-out, shift-right, shift register



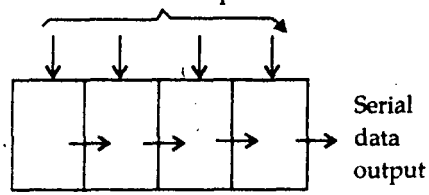
(b) Serial-in, serial-out, shift-right, shift register



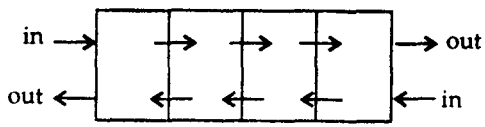
(c) Serial-in, parallel-out, shift register



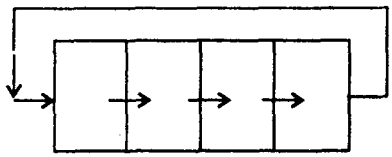
(d) Parallel-in, parallel-out,shift register



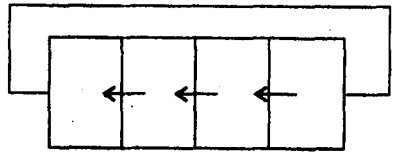
(e) Parallel-in, serial-out, shift register



(f) Serial-in, serial-out,shift-left, shift-right, (bidirectional) shift register



(g) Rotate-right shift register



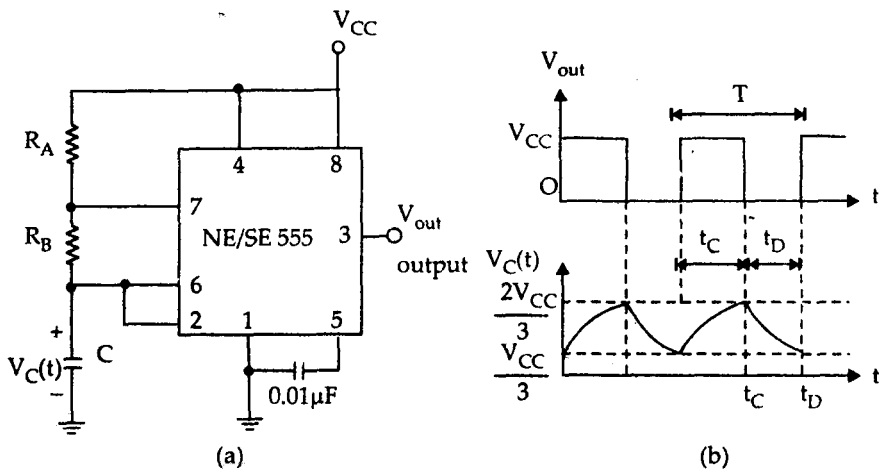
(h) Rotate-left shift register

Q.5. Attempt any two parts of the following :

Q.5. (a) Describe the working of 555 timer. How it works in A-stable operation ?

Ans. A Stable Multivibrator

A stable multivibrator has no stable state both the states are quasi-stable state hence it is also known as a free running multivibrator. As the wave is generated utilizing charging and discharging of capacitor so free running multivibrator falls in the category of relaxation oscillator. A 555 timer connected as an astable multivibrator is shown in Fig.(a). The duration for which output voltage remains high or low is



determined by externally connected resistors R_A and R_B and capacitor C. When the output is high, capacitor C changes towards V_{CC} through resistors (R_A + R_B). When the voltage across capacitor equal 2 V_{CC}/3, the output switches back to low state and capacitor C discharges through R_B and discharging transistor Q_D. When the voltage across capacitor equals V_{CC} /3, which sets the internal flip-flop, with $\overline{Q}$ = 0 discharge transistor is turned OFF and output goes high, the capacitor now charges through R_A and R_B. Then the cycle repeats. The related waveforms are shown in Fig.

Referring to Fig. we can notice that the capacitor is charged and discharged periodically between 2 V_{CC}/3 and V_{CC}/3 .

During time t_C capacitor charges from V_{CC} /3 to 2 V_{CC} /3. Let us assume the initial voltage across capacitor is V_{CC} /3 , then capacitor voltage V_C (t) is given as

$$V_C(t) = V_{CC} - 2V_{CC}/3e^{-t}/(R_A + R_B)C \quad ...(1)$$

at $t = t_C$, $V_C(t) = 2V_{CC}/3$ then equation (1) is reduced to

$$2V_{CC}/3 = V_{CC} - 2V_{CC}/3e^{-t_C}/(R_A + R_B)C \quad ...(2)$$

Thus equation (2) gives the charging time t_C, *i.e.*

$$t_C = (R_A + R_B)\,C \ \text{In}\,(2)$$

or

$$t_C = 0.69\,(R_A + R_B)\,C \quad ...(3)$$

During time t_D, Capacitor discharges from 2 V_{CC} /3 to V_{CC} /3 through resistor R_B let us assume, the initial voltage across capacitor is 2 V_{CC} /3, the capacitor voltage V_C (t) is given as,

$$V_C(t) = 2V_{CC}/3\,e^{-t/R_BC} \quad ...(4)$$

At $t = t_D$, $V_C(t) = V_{CC}$ /3, then equation (4) is reduced to

$$V_{CC}/3 = 2V_{CC}/3e^{-t_D/R_BC} \quad ...(5)$$

Equation (5) gives the discharging time

$$t_D = R_BC \ \text{In}\,(2)$$

or $t_D = 0.69\ R_B C$ ...(6)

using equation (4) and (6) we can obtain the period of output wave form i.e. $T = t_C + t_D$

$$= 0.69\,(R_A + R_B)C + 0.69\,R_B C$$

$$T = 0.69\,(R_A + 2R_B)C \quad ...(7)$$

The frequency of output waveform is therefore given as

$$f_0 = \frac{1}{T} = \frac{1}{0.69(R_A + 2R_B)C} = \frac{1.45}{(R_A + 2R_B)C} \quad ...(8)$$

Duty cycle of output waveform is the ratio of charging time t_C to its period T i.e.

$$D = \frac{t_C}{T} \quad ...(9)$$

using equation (3) and (7) in equation (9), we get

$$\%D = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

Thus duty cycle can be set by selecting R_A and R_B.

Q.5. (b) Explain A/D converter using voltage to frequency converter. Describe any one method of A/D converter.

Ans. **The Dual-Slope Type A/D Converter**

The dual-slope converter is one of the slowest converters, but is relatively inexpensive because it does not require precision components such as a DAC or VCO. Another advantage of the dual-slope ADC

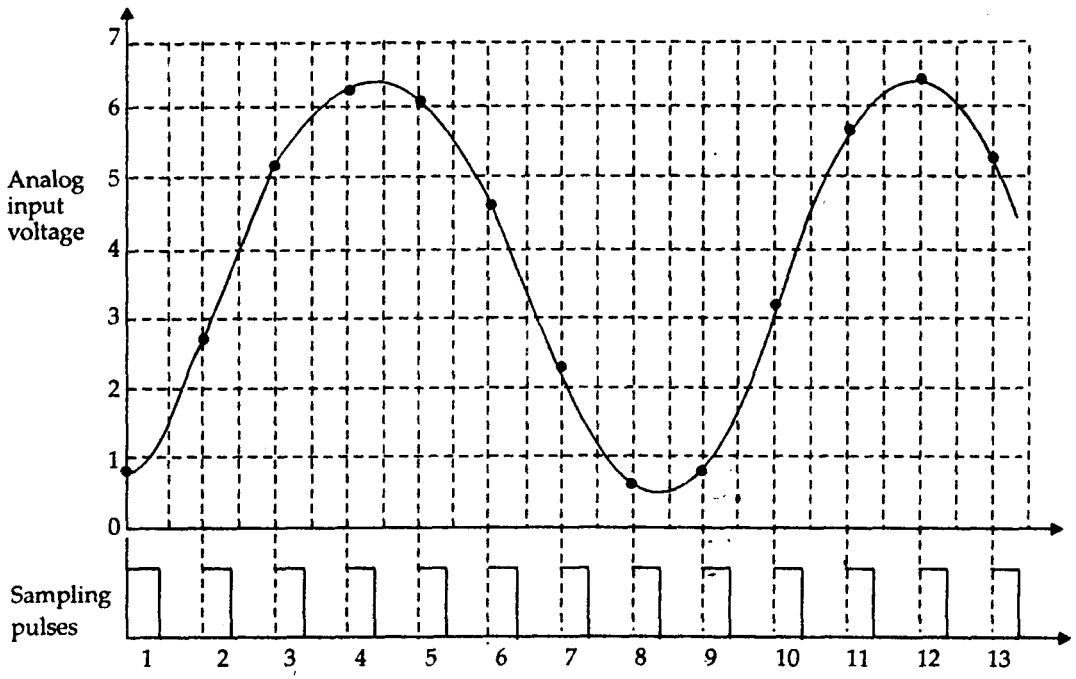
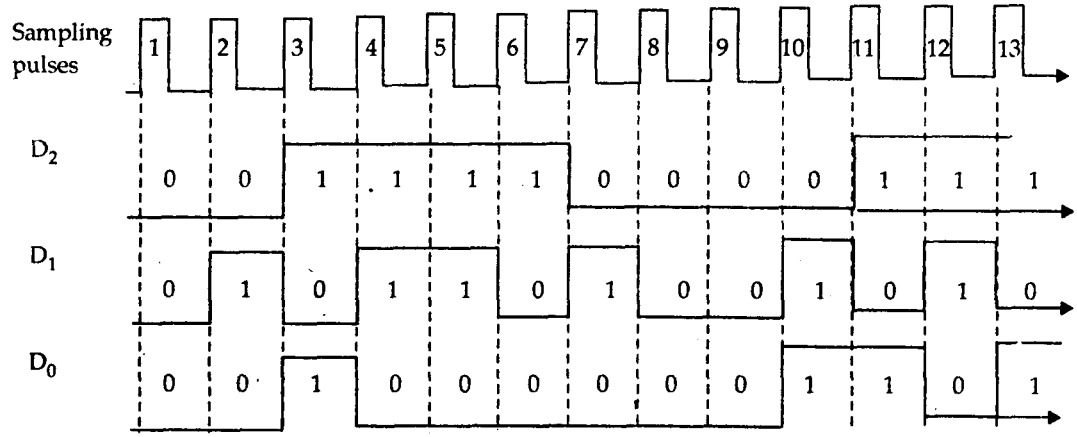


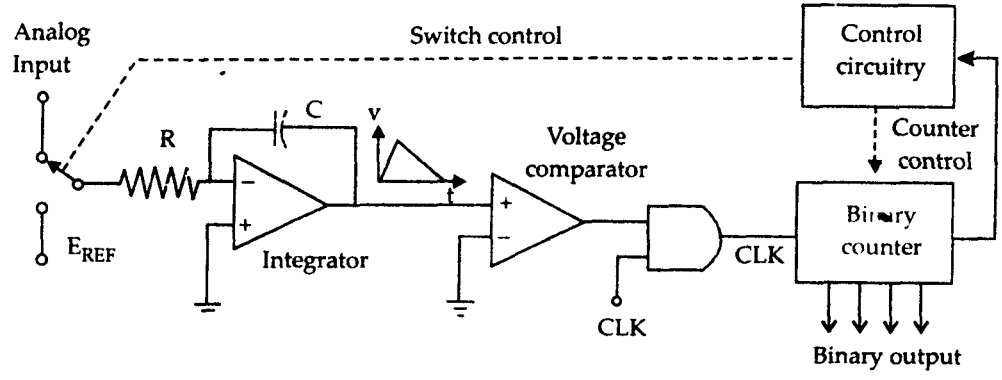
Fig. Waveforms



is its low sensitivity to noise, and to variations in its component values caused by temperature changes. Because of its large conversion time, the dual-slope ADC is not used in any data acquisition applications. The major application this type of converter are in digital voltmeters, multimeters, etc. where slow conversation of input are not a problem. Since it is not fast enough, its use is restricted to signals having input to medium frequencies.

A dual-slope ADC uses an operational amplifier to integrate the analog input. The output of the integrator is a ramp, whose slope is proportional to the input signal E_{in}, since the components R and C are fixed. If the ramp is allowed to continue for a fixed time, the voltage it reaches in that time, depends on the slope of the ramp and, therefore, on the value of E_{in}. The basic principle of the integrating ADC is that, the voltage reached by the ramp controls the length of time that the binary counter is allowed to count. Thus, a binary number proportional to the value of E_{in} is obtained. In the dual-slope ADC, two integrations are performed.

Figure shows the functional block diagram of a dual-slope ADC. Assume that the counter is reset and the output of the integrator is zero.



Connected to the analog input. Assume that the input is a negative voltage and is constant for a period of time; so, the output of the integrator is a positive ramp. The ramp is allowed to continue for a fixed time and the voltage it reaches in that time is directly dependent on the analog input. The fixed time

is controlled by sensing the time when the counter reaches a particular count. At that time, the counter is reset and the control circuitry causes the switch to be connected to a reference voltage E_{REF}, having a polarity opposite to that of the analog input; in this case a positive reference voltage. Therefore, the output of the integrator is a negative going ramp, beginning from the positive value it reached during the first integration. The AND gate is enabled and the counter starts counting. When the ramp reaches 0 V, the voltage comparator switches to LOW, inhibiting the clock pulses and the counter stops counting. The binary count is latched, thus, completing one conversion. The count it contains at that time js proportional to the time required for the negative ramp to reach zero, which is proportional,to the positive voltage reached during the first integration, which in turn is proportional to the analog input.

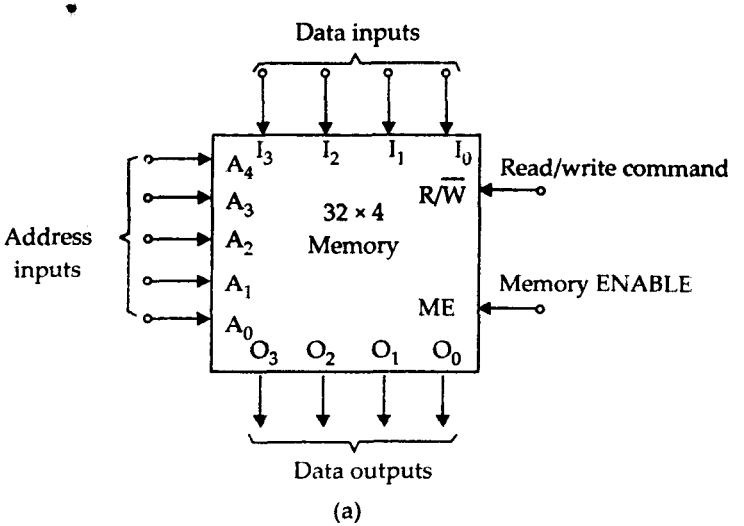
Q.5. (c) Explain the organisation of RAM with the help of neat diagram. Also describe the switching regulators.

Ans. Memory organization : The word size—the number of bits in a word—varies among computer systems and may range from 4 to 64 or more bits. The word size is usually expressed as a certain number of bytes. For example, a 16-bit word is 2 bytes.

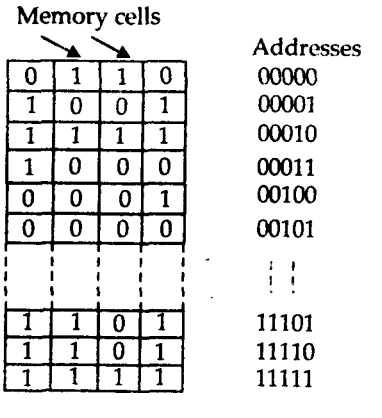
A memory location is thus a set of devices capable of storing one word. For example, each memory location in an 8-bit microcomputer (one that uses 8-bit words) might consist of eight latches. Each latch, stores one bit of a word, and is referred to as a cell. The capacity or size of a memory is the total number of bits or bytes or words that it can store. For convenience, the size of a memory is expressed as a multiple of $2^{10} = 1024$, which is abbreviated K. For example, a memory of size $2^{11} = 2048$ is said to be 2K. A memory of size 2^{14} (16,384) is 16K, and a memory of size 2^{16} (65,536) is 64K.

Every memory system requires several different types of input and output lines to perform the following functions.

1. Select the address in memory that is to be accessed for a read or write operation.
2. Select either a read or a write operation to be performed.
3. Supply the input data to be stored in memory during a write operation.



(a)



(b)

4. Hold the output data coming from memory during a read operation.

5. Enable (or disable) the memory, so. that it will (or will not) respond to the address inputs and read/write command.

Figure illustrates these basic functions in a simplified diagram of a 32 × 4 memory that stores 32 4-bit words. Since the word size is 4-bits, there are four data input lines I_0 to I_3 and four data output lines O_0 to O_3. During a write operation, the data to be stored in memory have to be applied to the data input lines. During a read operation, the word being read from memory appears at the data output lines.