**Roll No. ……………………………………………………………**

**NEELKANTH INSTITUTE OF TECHNOLOGY**

**B.Tech ECE (Semester VII)**

**FIRST SESSIONAL EXAMINATION 2015-2016**

**VLSI Design (EEC-703)**

***Time: 1:30 Hours Total Marks 30***

***NOTE: - i.*** *Be precise in your Answer*

***ii.*** *All section are compulsory*

**SECTION A**

1. **Attempt all the Questions: 1X10=10**
2. In Y Chart Behavior domain deals with
3. Algorithm and FSM
4. Transistor gates
5. Mask and layout
6. Floor-plan
7. Identify the largest component of power in a digital CMOS circuit
8. Dynamic
9. Short-circuit
10. Leakage
11. Glitch
12. Which is the most effective method for reducing the power consumption of a CMOS logic circuit
13. Increase threshold voltage
14. Reduce threshold voltage
15. Reduce clock frequency
16. Reduce VDD
17. Write down the two importance of Silicon dioxide layer\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.
18. Draw the band diagram of NMOS under external bias under depletion mode.
19. If the body-bias voltage increase with reference to source the threshold voltage **Increase/Decrease**
20. Consider a MOS System tox=200A0 ,Φgc= -0.85 V , NA= 2 X 1015 cm-3, Qox= 2qX1011 C/cm2

Determine the Threshold voltage under zero bias at room temperature. ᶓox=3.97ᶓo , ᶓsi=11.7ᶓo.

1. The electrical channel length related to mask channel length by \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.
2. If the scaling factor is ‘S’, and say design rule change from 1 µm to 1/S µm then in Constant E scaling the power density will be \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.
3. Equation for the trans-conductance is \_\_\_\_\_\_\_\_\_\_\_.

**SECTION B**

1. **Attempt any Five Question : 2X5=10**
2. Draw the Y chart and explain the VLSI Design process.
3. What are the various process of CMOS fabrication?
4. Draw the variation of MOSFET Capacitance in different region of operation.
5. Explain the scaling down of Mos-transistor using constant Voltage scaling and its effects on delay and power delay product limitations.
6. Explain the structure and operation of NMOS transistor. What is meant by Zpu and Zpd? If a MOS inverter is to be driven from another NMOS inverter, find the ratio of Zpu to Zpd ?
7. Derive an expression for depletion width.

**SECTION C**

1. **Attempt any Two Questions: 5X2=10**
2. Derive the expression for VIH, VIL, Vth, NML and NMH for resistive load inverter with required diagram.
3. Explain the operation of the MOSFET and derive an expression for the current in linear and saturation region also draw Ids Vs Vgs & Ids Vs Vds.
4. Measured voltage and current data for Mosfet are given below. Assume фF=-0.3V.

|  |  |  |  |
| --- | --- | --- | --- |
| **Vgs(V)** | **Vds(V)** | **Vsb(V)** | **Id(uA)** |
| 3 | 3 | 0 | 97 |
| 4 | 4 | 0 | 235 |
| 5 | 5 | 0 | 433 |
| 3 | 3 | 3 | 59 |
| 4 | 4 | 3 | 173 |
| 5 | 5 | 3 | 347 |

Determine the type of the device and calculate the parameter Kn, VT and.