**Roll No. ……………………………………………………………**

**NEELKANTH INSTITUTE OF TECHNOLOGY**

**B.Tech ECE (Semester VII)**

**SECOND SESSIONAL EXAMINATION 2015-2016**

**VLSI Design (EEC-703)**

***Time: 2:00 Hours Total Marks 60***

***NOTE: - i.*** *Be precise in your Answer*

***ii.*** *All section are compulsory*

**SECTION A**

1. **Attempt all the Questions: 2X10=20**
2. Prove that in CMOS inverter the ratio of W/L of PMOS to NMOS is 2.5
3. A clock driver has a total output capacitance of 50pF. The supply voltage is 0.9V and the clock frequency is 2GHz. Calculate the power consumption of the clock signal.
4. Using the Elmore delay formula, the delay of a long interconnect of length s is proportional to\_\_\_\_\_\_\_\_\_\_\_\_.
5. What determines the upper bound and lower bound for VDD in CMOS circuit?

* **Statement:-**The following network supplies clock to flip-flops connected to nodes 1, 2 and 3. Use the Elmore delay formula to compute the source to clock delays for the three flip-flops?

R = 3Ω

C = 2pF

1

R = 3Ω

C = 2pF

2

R = 3Ω

C = 2pF

3

Clock

source

1. Define the Short circuit power consumption in CMOS circuit. Draw the CMOS NAND gate.
2. If the scaling factor is ‘S’, and say design rule change from 1 µm to 1/S µm then in Constant E scaling What will be the power density.
3. Design a transmission gate (symbolic) based 2 input XOR gate.
4. Prove that a CMOS gate consumes no short-circuit power when VDD ≤ Vtn + |Vtp|, i.e., supply voltage is below the sum of the threshold voltage magnitudes for the n and p channel MOSFETs.
5. Draw the device structure of CMOS inverter.
6. Performance parameter in CMOS digital circuit design.

**SECTION B**

1. **Attempt any Five Question : 4X5=20**
2. Derive an expression for the Average power consumption in CMOS inverter. And also explain the effect of frequency on power and energy and Energy delay product.
3. Implement the following equation using **CMOS**

**Z= (A+D+E)(B+C)**

Also find the equivalent **W/L** of PMOS and NMOS network if W/L of NMOS and PMOS are 10 and 15 respectively.

1. Consider a CMOS inverter circuits with the following parameter Vdd =3.3 V, VT,on = 0.6V, VT,op=-0.7V,   
   Calculate the noise margin of the circuit.
2. Consider a CMOS inverter, does the inverter with lower VOL always have the shorter high to low switching time? Justify your answer.
3. Explain the working principle of Transmission gate with all relevant equations.
4. Design a full adder circuit with CMOS such a way that minimum number of transistor are used.
5. What is meant by Zpu and Zpd? If a Depletion load inverter is to be driven from another inverter having a chain of Pass transistor in between them, find the ratio of Zpu to Zpd?

**SECTION C**

1. **Attempt any Two Questions: 10X2=20**
2. Derive the expression for VIH, VIL, Vth, for CMOS inverter with required diagram.
3. Draw a two input CMOS NOR gate and its stick diagram. Also derive an expression for Vth.
4. Derive an expression for **tPLH** of CMOS inverter.