Course Handout

CHITKARA UNIVERSITY
HIMACHAL PRADESH
NAAC A+ ACCREDITED

Institute/ School Name	School of Engineering and Technology		
Department Name	Department of Computer Science & Engineering		
Program Name	Bachelor of Engineering (Computer Science & Engineering): B.E (CSE)		
Course Code	24CS016	Course Name	Computer System Architecture
L-T-P (Per Week)	3-0-0	Course Credits	03
Academic Year	2024-25	Semester/Batch	4th /2023-2027
Course Coordinator	Dr. Navneet Kaur		

1. Course Outline:

Introduction to Computer Organization and Evolution of Computers, Introduction to digital computers, Basic Computer Organization, Timing and Control, Microprogrammed Control, Design of Control unit, Central Processing Unit, Pipeline Processing, Program Interrupts & Types, Input-Output Organization, Memory Organization, Associate Memory, Virtual Mapping.

2. Programme Outcomes (POs):

At the end of the programme, students will be able to	
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
PO 6	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	**Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO 8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO 9	**Individual and teamwork**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	**Life-long learning**: Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

3. Course Learning Outcomes (CLO):

After completing the course, the students will be able to:

- **CLO1:** Understand the basic structure and operation of a digital computer system.
- **CLO2:** Acquire the skills to analyze the design of the various functional units and components of a computer.
- **CLO3:** Analyze the architecture and functionality of central processing unit.
- **CLO4:** Implement the concept of pipeline and the different ways of computer I/O.
- **CLO5:** Comprehend the structure and functioning of hierarchical memory organization, emphasizing environment and sustainability through energy-efficient designs.

4. CLO-PO Mapping Matrix:

Course Learning Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CLO1	M				H	L						
CLO2	H	L			L							
CLO3	H	M	M	H	H							M
CLO4	L	H		M								M
CLO5		H	M	M			H					M

5. ERISE Grid Mapping:

Feature Enablement	Level (1-5, 5 being highest)
Entrepreneurship	1
Research/Innovation	3
Skills	5
Employability	3

6. Recommended Books (Reference Books/Text Books):

B01: Hamacher, C., & Vranesic, Z., Computer organization and embedded system (6th Edition). Tata McGraw Hill.

B02: Bulic, P., Understanding computer organization: A guide to principles across RISC-V, ARM Cortex, and Intel architectures (1st Edition). Springer-Nature New York Inc.

B03: Mano, M. M., Computer system architecture (Revised 3rd Edition). Prentice-Hall of India.

B04: Patterson, D. A., & Hennessy, J. L., Computer organization and design ARM edition: The hardware/software interface (1st Edition). Morgan Kaufmann.

B05: Tanenbaum, A. S., Structured computer organization (6th Edition). Prentice-Hall of India.

7. Other readings and relevant websites:

Resources	Link of Journals, Magazines, Websites and Research Papers
R1	Hwang, I., Lee, J., Kang, H., Lee, G., & Kim, H. (2024). Survey of CPU and memory simulators in computer architecture: A comprehensive analysis including compiler integration and emerging technology applications. Simulation Modelling Practice and Theory, 103032.
R2	https://www.geeksforgeeks.org/generations-of-computers-computer-fundamentals/
R3	https://www.techtarget.com/whatis/definition/logic-gate-AND-OR-XOR-NOT-NAND-NOR-and-XNOR
R4	https://www.electronicsforu.com/technology-trends/learn-electronics/flip-flop-rs-jk-t-d
R5	https://www.ebrary.net/206239/computer_science/mapping_schemes

R6	https://www.synopsys.com/glossary/what-is-risc-v.html#:~:text=As%20an%20open%2Dstandard%20architecture, new%20degrees%20of%20design%20freedom
Resources	**Link of Audio-Video resources**
V1	https://archive.nptel.ac.in/courses/106/105/106105163/
V2	https://www.digimat.in/nptel/courses/video/106105163/L01.html
V3	https://nptel.ac.in/courses/108105132
V4	https://onlinecourses.nptel.ac.in/noc25_cs01/preview

8. Course Plan:

Lecture Number	Topics	Weightage in ETE (%)	Instructional Resources
1	Introduction to Computer Organization and Evolution of Computers from 1st Generation to Present generation	22	B01, B03, B05, R2, V1, V2
2	Von-Neumann Architecture		B02, B03, R2, V1, V2
3	Introduction to digital computers, Introduction to number system		B01, B03, B05, V3, V4
4	Octal and Hexadecimal Numbers, Decimal Representation		B02, B03, V3, V4
5	Logic gates (AND, OR, NOT, NAND, NOR, EX-OR and Ex-NOR). Introduction to combinational and sequential circuits		B02, B03, R3, V3, V4
6	Flip Flops (SR, D)		B02, B03, R4, V3, V4
7	Flip Flops (T, JK)		
8	Registers (SISO, PISO, SIPO, PIPO)		
9-10	Basic Computer Organization: Instruction Codes, Computer Registers, Computer Instructions	20	B04, B05, V1, V2
11-12	Timing and Control, Instruction Cycle		
13-14	Memory Reference Instructions, Input Output and Interrupt		B04, V1, V2
15	Complete Computer Description		
16-17	Microprogrammed Control: Control Memory, Address Sequencing	8	B01, B04, V1, V2
18-19	Micro program Example		
20-21	Central Processing Unit: Introduction, General Register Organization, Stack Organization	19	B03, B05, R1, V1, V2
22-23	Instruction Format (Three address, Two Address, one address, zero address)		
24	Addressing Modes, Data Transfer and Manipulation		
25	Program Control: Status bits, Conditional Branch Instructions		
26	Program Interrupts & Types		B03, B05, V1, V2
27	RISC/CISC Characteristics		B03, B05, R2, V1, V2
28	Pipeline Processing and Parallel processing, Flynn's Classification	8	
29	Pipelining General considerations		
30	Arithmetic Pipeline, Floating point addition and subtraction, Instruction Pipeline		
31	Input-Output Organization, Peripheral Devices, I/O Interface	12	

32-33	Asynchronous Data Transfer, Strobe control, Handshaking, Asynchronous serial transfer, Asynchronous serial interface, Modes of data Transfer		
34	Direct Memory Access (DMA), DMA Controller		
35-36	Input-Output Processor (IOP), CPU-IOP Communication		
37-38	Memory Organization: Memory Hierarchy, Main Memory (RAM & ROM Chips)	11	B03, B05, R5, V1, V2
39	Associative Memory: Hardware Organization		
40-41	Cache Memory, Associative Mapping		
42	Direct Mapping, Set-Associative Mapping		
43	Virtual Memory		
44-45	Emerging Technologies in computer system architecture: RISC-V Open-Source Architectures, Introduction to quantum computing		B02, R6, V3, V4

9. Innovative Pedagogies:

- Collaborative learning (Annexure-I)

10. Action plan for different types of learners

Slow Learners	Average Learners	Advanced Learners
Remedial Classes	Practice Assignment (Annexure-II)	Report on current trends in Computer System Architecture (Annexure-III)

11. Evaluation Scheme & Components:

Evaluation Component	Type of Component	No. of Assessments	Weightage of Component	Mode of Assessment Offline/Online
Internal Component 1	Formative Assessment (FA)	01*	10%	Offline
Internal Component 2	Sessional Tests (STs)	03**	30%	Offline
External Component	End Term Examination (ETE)	01	60%	Offline
	Total	100%		

*Formative assessment is mandatory

**Out of 03 STs, best 02 ST marks will be considered to evaluate final marks.

12. Details of Evaluation Components:

Evaluation Component	Description	Syllabus Covered (%)	Timeline of Examination	Weightage (%)
Internal Component 1	FA	Up to 40% (Lecture 1- 19)	Will be intimated one week prior	10
Internal Component 2	ST 1	Up to 40% (Lectures 1-18)	7th Week	30
	ST 2	41% - 80% (Lectures 19-36)	14th Week	
	ST 3	Up to 100% (Lectures 1-45)	17th Week	
External Component	End Term Examination*	100%	As Notified by the Exam Cell	60
Total				100

* Minimum 75% attendance is required to become eligible for appearing in the End Semester Examination

13. Format of Evaluation Components:

Type of Assessment	Total Marks	Quiz (Closed-ended)	Assignment	1 Marks	2 Marks	5 Marks	10 Marks
Formative Assessment	20	10	10	10	-	-	-
Sessional Tests	40	-	-	5	5	3	1
End Term Examination	60	-	-	5	5	5	2

14. Revision (if any):

Academic Year of Previous Version	2023-2024	Percentage of Revision	7%
Topics:			
• Emerging Technologies in computer architecture: RISC-V Open-Source Architectures, Introduction to Quantum Computing (Added) • Design of Control Unit (Removed), as the details will be covered under Central Processing Unit.			

15. This Document is:

Designation	Name	Signature
Prepared by Course Coordinator	Dr. Navneet Kaur	Navneet Kaur
Verified by Program Incharge/HoD	Dr. Hakam Singh	For: Hakam
Approved by Pro VC	Prof. (Dr.) Meenu Khurana	Meenu
Date:	January 2, 2025	

Annexure-I

Sr. No	Topics
1.	Collaborative learning: Addressing Modes

Description: Students will explore the fundamental concepts of addressing modes, focusing on their significance and applications in understanding computer organization. Through collaborative group discussions, they will deepen their understanding of how addressing modes operate within computer architecture.

Procedure:

1. **Group Formation:** Students will form teams of 3 to 4 members.
2. **Provide a common problem:** Each group will add two numbers and store the result in the register and memory locations. Each group will implement the task using different addressing modes, such as:
   - Immediate Addressing
   - Direct Addressing
   - Indirect Addressing
   - Register Addressing
   - Indexed Addressing
3. **Implementation:** Write assembly code, explain data processing involved in each addressing mode, and compare performance.
4. **Discussion:** Each group will share their findings with other groups and collaborate to determine the optimal addressing mode for specific applications.

Expected Outcomes:

- Students will develop a clear understanding of different addressing modes and their applications.
- This activity will enhance students' collaboration and problem-solving skills.

Annexure-II

Sr. No	Topics
1.	Octal and Hexadecimal Numbers, Decimal Representation, Logic gates, combinational and sequential circuits, Flip Flops, Registers

Description: Students will be given a numerical based assignment focusing on the above-mentioned topics.

Annexure-III

Sr. No	Topics
1.	Emerging technologies in computer system architecture

Description: Students will write a report on emerging technologies in computer system architecture such as quantum computing, edge computing, RISC-V Open-Source Architectures and neuromorphic computing.