Curriculum Vitae

Verilog Projects Showcase

Verilog Projects

- **4-bit ALU (Arithmetic Logic Unit)**: Designed a combinational ALU supporting ADD, SUB, AND, OR, XOR, NOT, and shift operations. Verified functionality using a modular testbench and GTKWave simulation.
- **Digital Clock**: Implemented a 24-hour digital clock with seconds, minutes, and hours counters. Used clock division and multiplexed 7-segment display logic.
- **Binary to BCD Converter**: Developed a binary-to-BCD conversion module using the double-dabble algorithm. Tested with multiple input widths and verified with waveform simulations.
- **Traffic Light Controller**: Created an FSM-based traffic signal controller for a two-way intersection. Ensured proper state transitions and timing using a 1s/1ms simulation scale and GTKWave.
- **UART Transmitter/Receiver**: Built a serial communication module supporting UART protocol. Included baud rate generator and FIFO buffer. Simulated and verified TX/RX functionality.
- **Stopwatch with Start/Stop/Reset**: Designed a stopwatch system using state machines and counters. Implemented debouncing for button input and multiplexed output display.
- **Pipelined RISC Processor**: Implemented a 5-stage pipelined RISC processor supporting R-type and I-type instructions. Handled hazards using forwarding and stalling mechanisms. Simulated with custom testbenches.
- **VGA Controller**: Developed a VGA signal generator to display patterns and characters on screen. Implemented 640x480 resolution timing logic and sync signal generation.
- **SPI/I2C Communication Interface**: Created Verilog modules for SPI and I2C master-slave communication. Verified protocol correctness and handshaking logic via simulation.
- **Edge Detection on FPGA**: Implemented real-time image processing (Sobel filter) in Verilog. Processed grayscale image data on FPGA using line buffer and parallel computation logic.