CAWS Lab (Day - 1)

December 21, 2020

Task-I

The goal of this lab is to determine the size of L1D, L2, and the last-level cache (LLC, a.k.a. L3). This can be done by using variations of a program that accesses an array of a specific size, say 16KB, 32KB, or 64KB, and then observing the instruction per cycle (IPC) difference. If at a specific cache size, there is an IPC drop, then that means that the previous cache size was the size of the cache. Going from 4KB to 4MB, you will first get the size of L1D, then L2, and finally LLC.

You need to do the following steps:-

1. Clone this GitHub repository: https://github.com/vishalgupta97/CAWS-LAB.git
2. Go through `cache-code.c` in the repository.
3. Generate traces using cache-code.c to access different array sizes (Input parameter to the program : `log2` of the array size to be accessed, 4KB: 12, 8KB: 13, and so on). Generate traces to access array sizes starting from 4KB to 8MB with different names (use -o parameter with the Pintool to specify the output trace name). Skip the first 10 million instructions and generate traces for the next 2 million instructions. Use -ifeellucky parameter with the Pintool. Compress the trace files to .gz format.
4. Build ChampSim with LRU replacement policy and no prefetchers.
5. Run the generated traces with a warmup of one million and simulation of one million instructions.
6. Note the difference in IPC, find the size of the caches, and verify the sizes by checking in the ChampSim file: inc/cache.h
7. Double the sizes of L1D, L2, and LLC by doubling the number of sets or ways and then repeat steps 3-5.

Task-II (optional)

1. In the cache-code.c file, make the following changes: comment line no. 20-23 and un-comment line no. 25-34. Repeat steps 2-5 mentioned above to generate and run the traces. Observe the change in IPC and reason about it.
2. Repeat steps 3-5 to generate and run the traces with the IP stride prefetcher at L1D. Observe the change in IPC and reason about it. Ensure line no. 20-23 are un-commented and line no. 25-34 are commented in cache-code.c file before generating the traces for this part.