Rajesh Saha

Project Engineer cum Ph.D (Part-Time) Scholar at NIT Uttarakhand
Area of Interest: Digital VLSI design and Embedded System
Phone (Mob):+91-9759794625- **Email:** rajeshsaha29@gmail.com, **DOB:** 29/12/1988

Summary

- Pursuing Ph.D. with experience of writing SPICE netlists to characterize CMOS and memory as storage & computing circuits (SRAM, nv-memory (STT-MRAM, SOT-MRAM and FLASH)) and design compact model using Verilog-A, MATLAB programming to develop Magnetic Tunnel Junction (MTJ) device.
- More than 4.5 years of experience in RTL coding (Verilog, SV and VHDL) to develop interfacing controls unit to interface different sensors (Fingerprint, Temperature and Humidity), LCD, GSM, ADC module and their verification. Developed RTL coding for hardware accelerator (Matching algorithm) and communication protocol (UART). Also possess a basic of interconnection protocol AXI, Xilinx SDK/VITIS.
- Possess a knowledge of VLSI Tool Flow **Full Custom Design** (Cadence Virtuoso) and **Semi-Custom** design (***ASIC***) (Cadence tools and Opensource tool; openlane), **FPGA design Flow** (Xilinx-Vivado), Static Timing Analysis (Cadence, OpenSTA and Vivado), code debugging (ILA, VIO), MATLAB scripting and C++ coding, python, and gem5 tool for computer architecture design.
- Experienced in scripting for automation for physical design in EDA tools (**linux-shell and Tcl**), installation of EDA tools (Cadence, Synopsys and Xilinx) and network administration.
- 1.5 year of hands-on experience in VLSI technology process optimization for sensors at CSIR-CEERI.
- Completed full time courses on Low Power VLSI design and Analog Integrated Circuits in NIT Uttarakhand with valid college credits.

Research Publications

- **Rajesh *at. el.,*** "Design of an Area and Energy-Efficient Last-Level Cache Memory using STT-MRAM" in Journal of Magnetism and Magnetic Materials, Elsevier, Feb, 2021.
- **Rajesh *at. el.,*** "Impact of Size, Latency of Cache-L1 and Workload over System Performance" In International Conference on Advances in Computing, Communication & Materials (ICACCM), pp. 390-393, IEEE, Nov.2020.
- **Rajesh *at. el.,*** "Classification of human heart signals by novel feature extraction techniques for rescue application." in Fifth International Conference on Image Information Processing (ICIIP), pp. 156-160 IEEE, 15 Nov.2019.
- **Rajesh Saha,** "On-Chip Bus Arbiter Testing and Verification in FPGA," *in International Journal of Advanced Engineering and Management",* Vol. 2, No. 8, pp. 196-199, 2017.
- **Rajesh Saha**, Vishwajit Nandi, Sahadev Roy, and Chandan Tilak Bhunia "Design and verifications of efficient arbiter of SoC's on-chip bus," In Proceeding of the 3rd International conference on Electronics and Communication System, pp. 989-992. IEEE, Feb 2016.

Education

- ***X and XII:*** Percentage: **71.50 and 65.20**, year: 2005 and 2007, SEBA and AHSEC board, Assam
- ***B. Tech in Electronics and Communication Engg:*** CGPA=**8.14/10**, Year=2008-12, The ICFAI University, Dehradun.
- ***M. Tech in Electronics and Communication Engg:*** CGPA=**9.4/10**, Year=2014-16, National Institute of Technology, Arunachal Pradesh.
- ***Ph.D in VLSI and Microelectronics*:** *Pursuing (Start date: 10th Oct. 2017 and expected to end Dec.* 2021), National Institute of Technology, Uttarakhand.
- ***Other qualification:*** GATE-2013, 14, 16 and NET-2017

Skills & Expertise

- Digital System Design
- HDL (Verilog, System-Verilog VHDL), MATLAB (scripting, ML tools, Simulink, XSG)
- FPGA (Artix, Zynq, Microblaze), Oscilloscope and signal generator (Xilinx-Analog Discovery Kit, Agilent-Keithley), TI-TM4C Launchpad and NodeMCU module.
- Basics of Python and C++
- Xilinx-ISE, VIVADO,VITIS/SDK, ALTERA-Quartus
- gem5 for computer system architecture design and simulation
- memory circuits design; Synopsys-HSPICE, and NV-sim
- VLSI design flow; Full Custom, Semi-custom and FPGA; Cadence, Openlane and Xilinx-Vivado
- RHEL/CentOS, Shell and Tcl scripting
- Cloud tools (Tinkercad, Thingspeak, Nodred)

Professional course and Certifications

- VLSI Chip Design Hands-on Using Open-Source EDA Tools (Openlane, OpenSTA)
- Full custom and Semi-custom Design Flow in VLSI using Cadence Tools with Entuple, Bengalore
- Artificial Intelligence and Neuromorphic Computing in collaboration with Intel, India
- Analog IC Design: Specification to Chip in collaboration with ISRO-SCL Chandigarh

Experience

Project Engineer/ Lab Engineer at NIT Uttarakhand

June 2016 to still (4 Years and 10 months)

- Responsibilities to develop RTL code to interface various modules like ADC module, LCD control unit, UART module, matching accelerator for matching data, Integration, functional and static timing analysis (STA) of developed module. (For data acquisition system)
- To develop embedded systems on Zynq Board.
- Installation and support to clients in VLSI Lab for EDA tools like Cadence, Synopsys and Xilinx. Developing scripts for automation in EDA tools.
- Demonstration of hardware implementation of developed modules to project sponsors.
- Work summary at github: https://github.com/rajeshsaha29/rajeshsaha29.git

Project Fellow at CSIR-CEERI, Pilani

March 2013 – August 2014

- Responsibilities to enhancement of process optimization, working to handle and to maintain micromachining, oxidation, deposition and lithography.
- Characterization of sensors & devices using two or four probe Keithley characterization systems.

Personal Details

- Name: Rajesh Saha
- Father's Name: Shri Prakash Saha
- Mother's Name: Smt. Chaina Saha
- Languages Known: Assamese, Bengali, English and Hindi

Declaration

I hereby declare that all the above information is correct to the best of my knowledge and believe.

Date: 14.05.2021
Place: Srinagar Garhwal, Uttarakhand