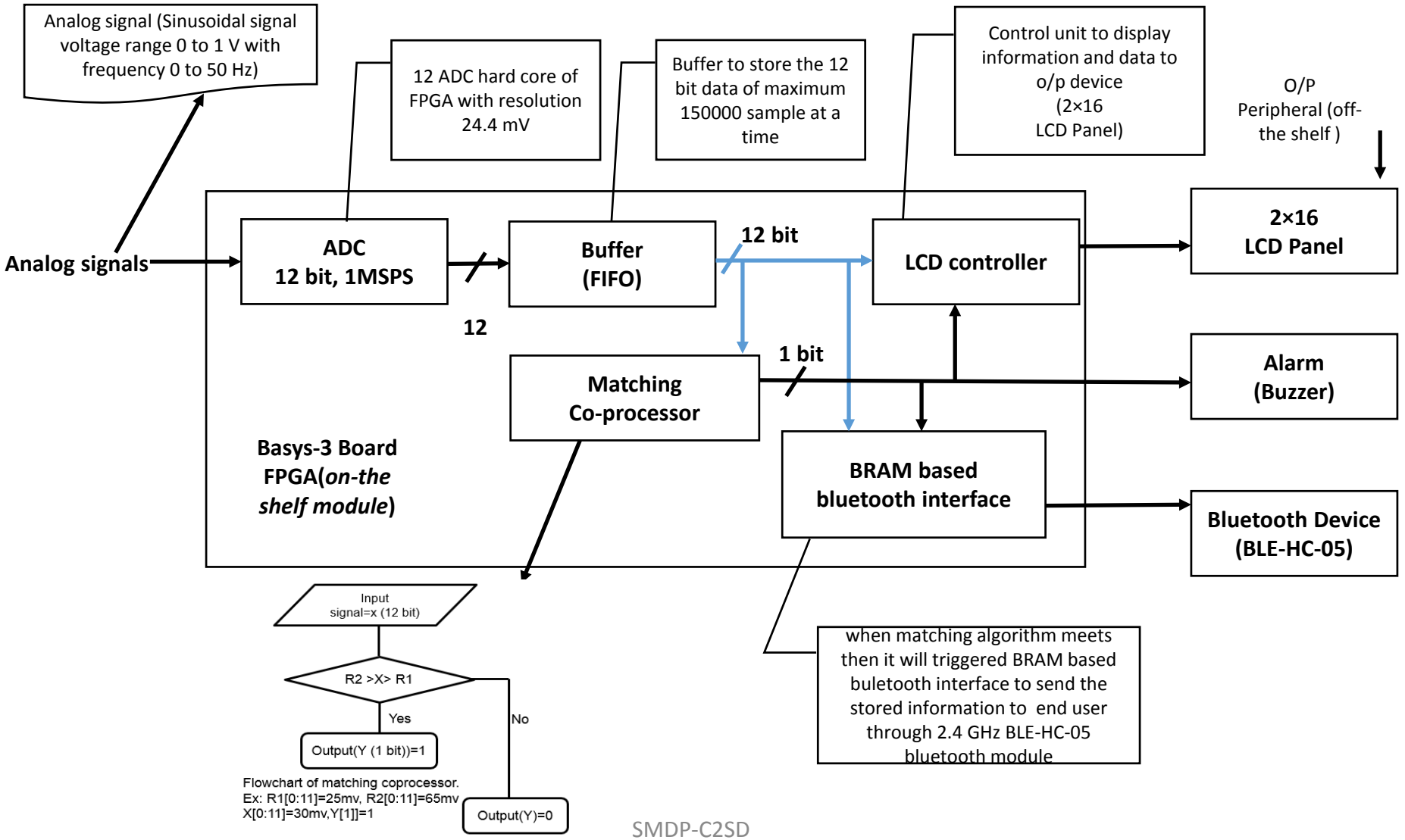
FPGA board level integration of module (Cluster part of NIT-Uttarakhand)

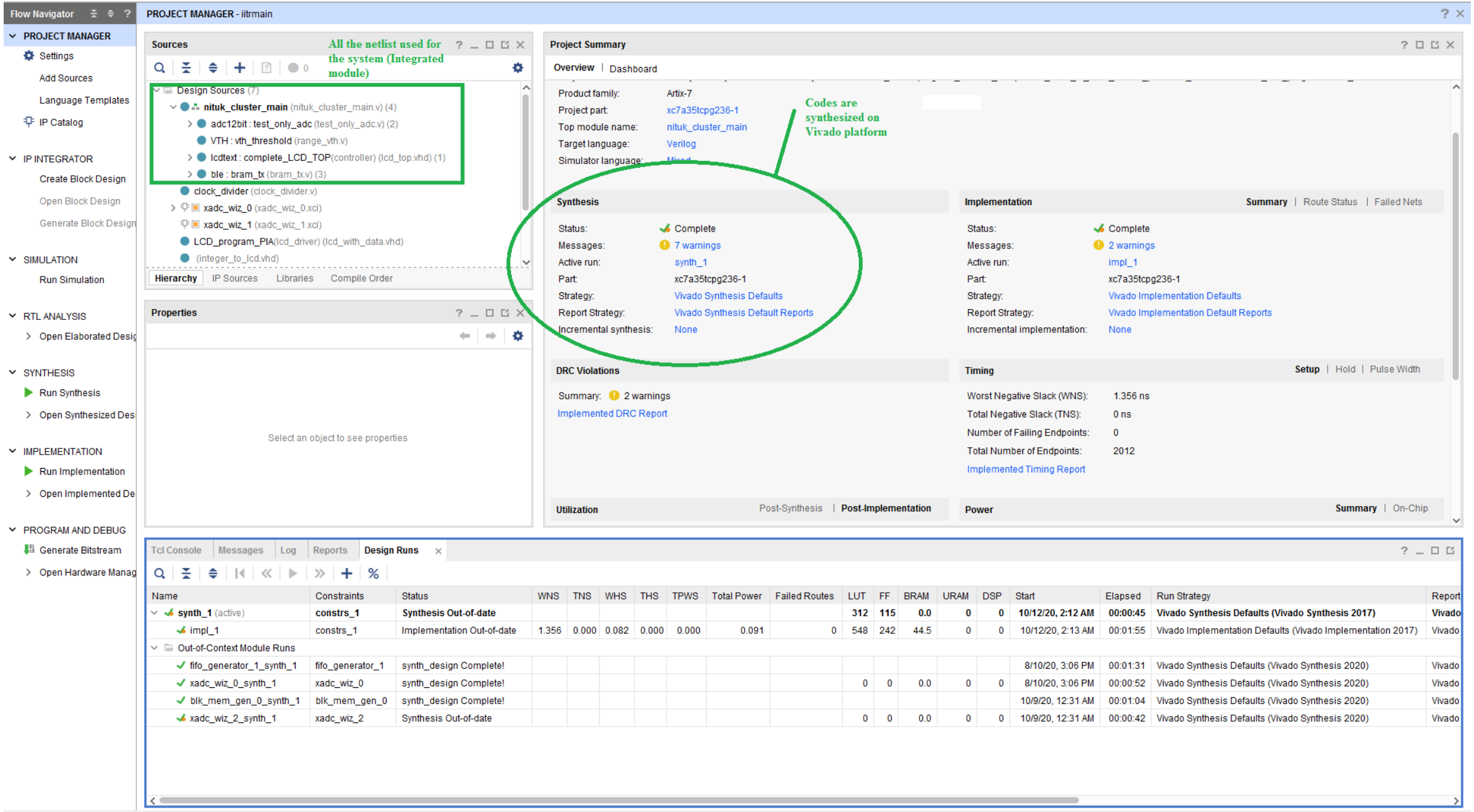


NB:
Hard core IP is used for this system:

1. ***BRAM and BRAM based FIFO*** for data storage.
2. ***12 bit ADC*** for converting analog sensor signals

NB:
All the module (i.e. control unit and communication protocol of each block) has been written in Verilog-HDL on ***Xilinx vivado platform*** and ***synthesized***. Also shows the demo of implementation on FPGA using developed synthesized codes.

Synthesized result



Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report
synth_1 (active)	**constrs_1**	**Synthesis Out-of-date**								**312**	**115**	**0.0**	**0**	**0**	**10/12/20, 2:12 AM**	**00:00:45**	**Vivado Synthesis Defaults (Vivado Synthesis 2017)**	**Vivado**
impl_1	constrs_1	Implementation Out-of-date	1.356	0.000	0.082	0.000	0.000	0.091	0	548	242	44.5	0	0	10/12/20, 2:13 AM	00:01:55	Vivado Implementation Defaults (Vivado Implementation 2017)	Vivado
Out-of-Context Module Runs																		
fifo_generator_1_synth_1	fifo_generator_1	synth_design Complete!													8/10/20, 3:06 PM	00:01:31	Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado
xadc_wiz_0_synth_1	xadc_wiz_0	synth_design Complete!								0	0	0.0	0	0	8/10/20, 3:06 PM	00:00:52	Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado
blk_mem_gen_0_synth_1	blk_mem_gen_0	synth_design Complete!													10/9/20, 12:31 AM	00:01:04	Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado
xadc_wiz_2_synth_1	xadc_wiz_2	Synthesis Out-of-date								0	0	0.0	0	0	10/9/20, 12:31 AM	00:00:42	Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado

Integration of modules for Data acquisitions (DAQ):

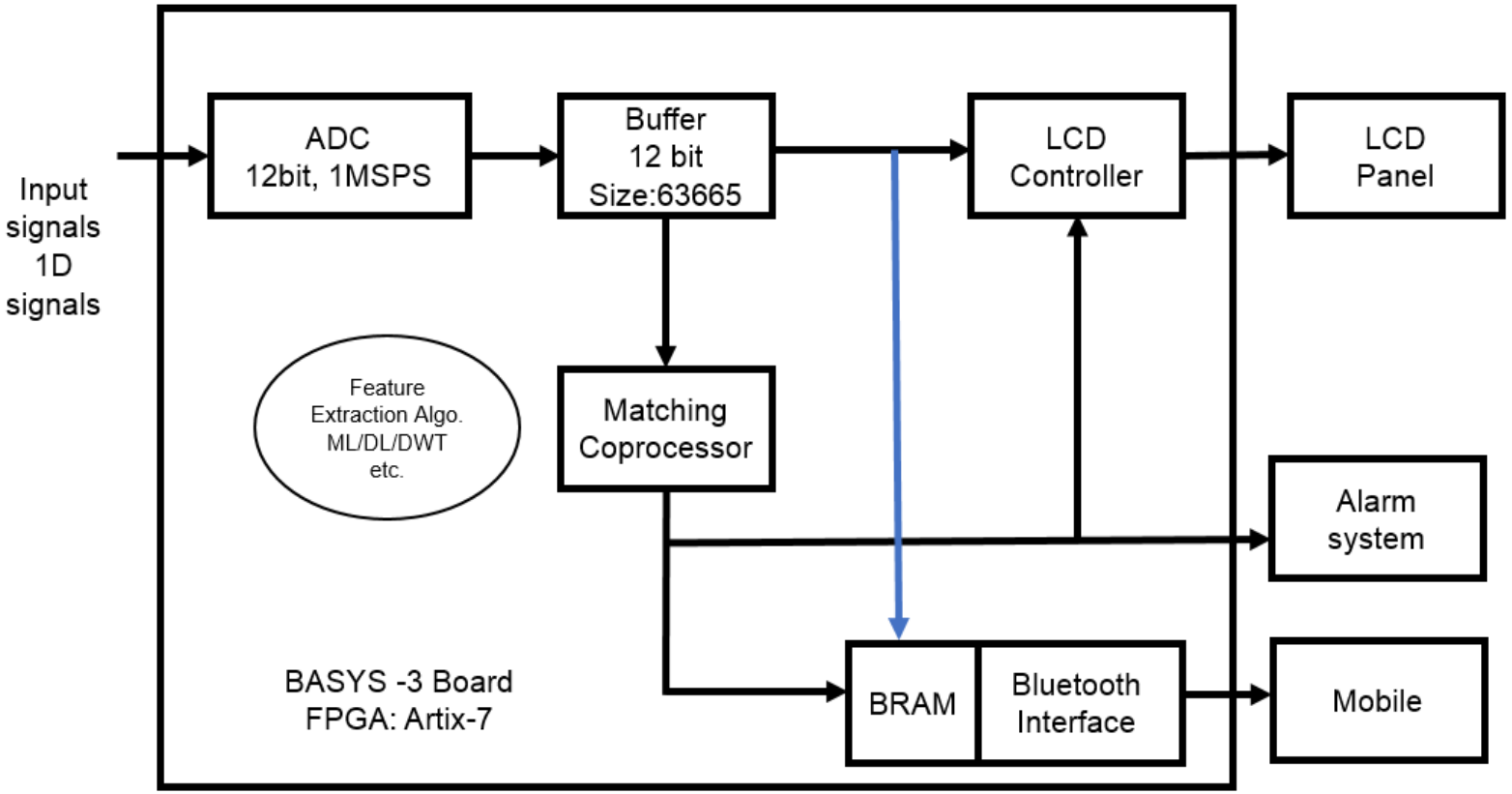


Fig.21: Block diagram of DAQ

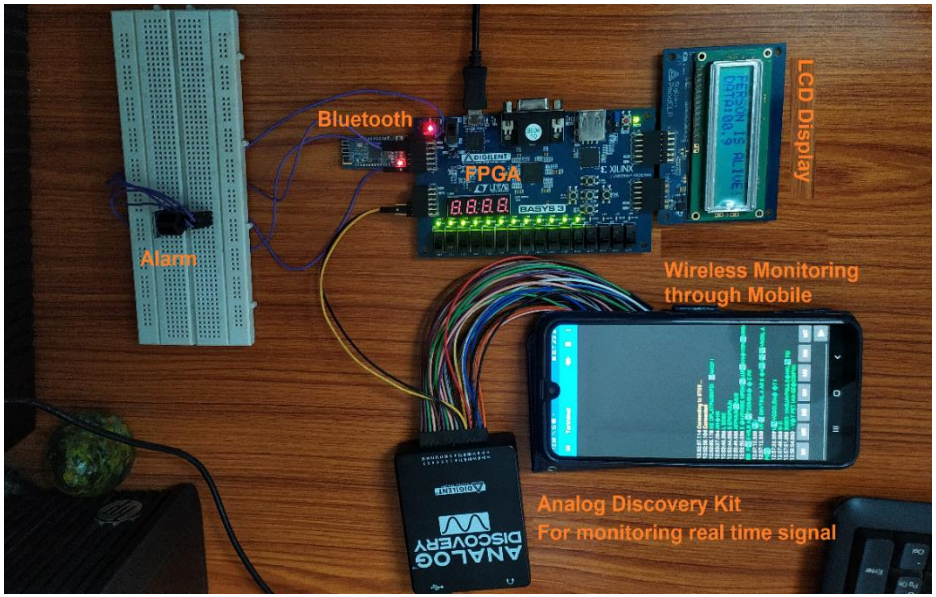


Fig.22: Real-time implementation DAQ

Resource	Utilized	Available
LUT	355	208000
FF	243	41600
BRAM	44.50	50
IO	33	106

Fig.23: Resource utilization

Total power consumption=83 mW

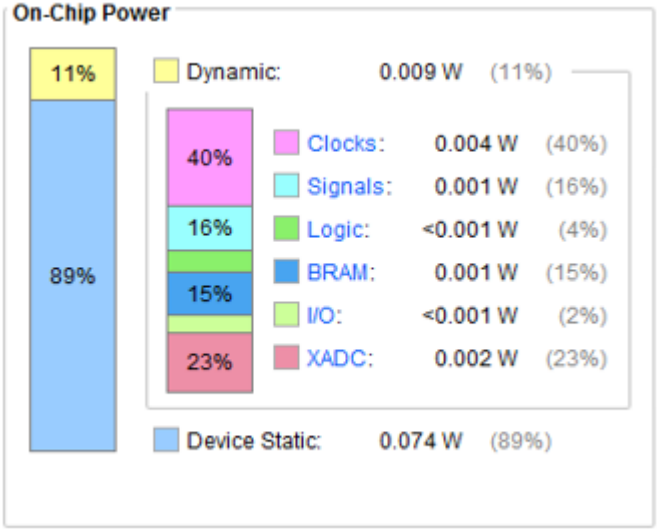


Fig.24: Power analysis of DAQ

Maximum operating Frequency=0.182 GHz

Setup Slack	Hold Slack	Pulse width
1.407ns	0.043na	5.5ns

Fig.25: Timing analysis