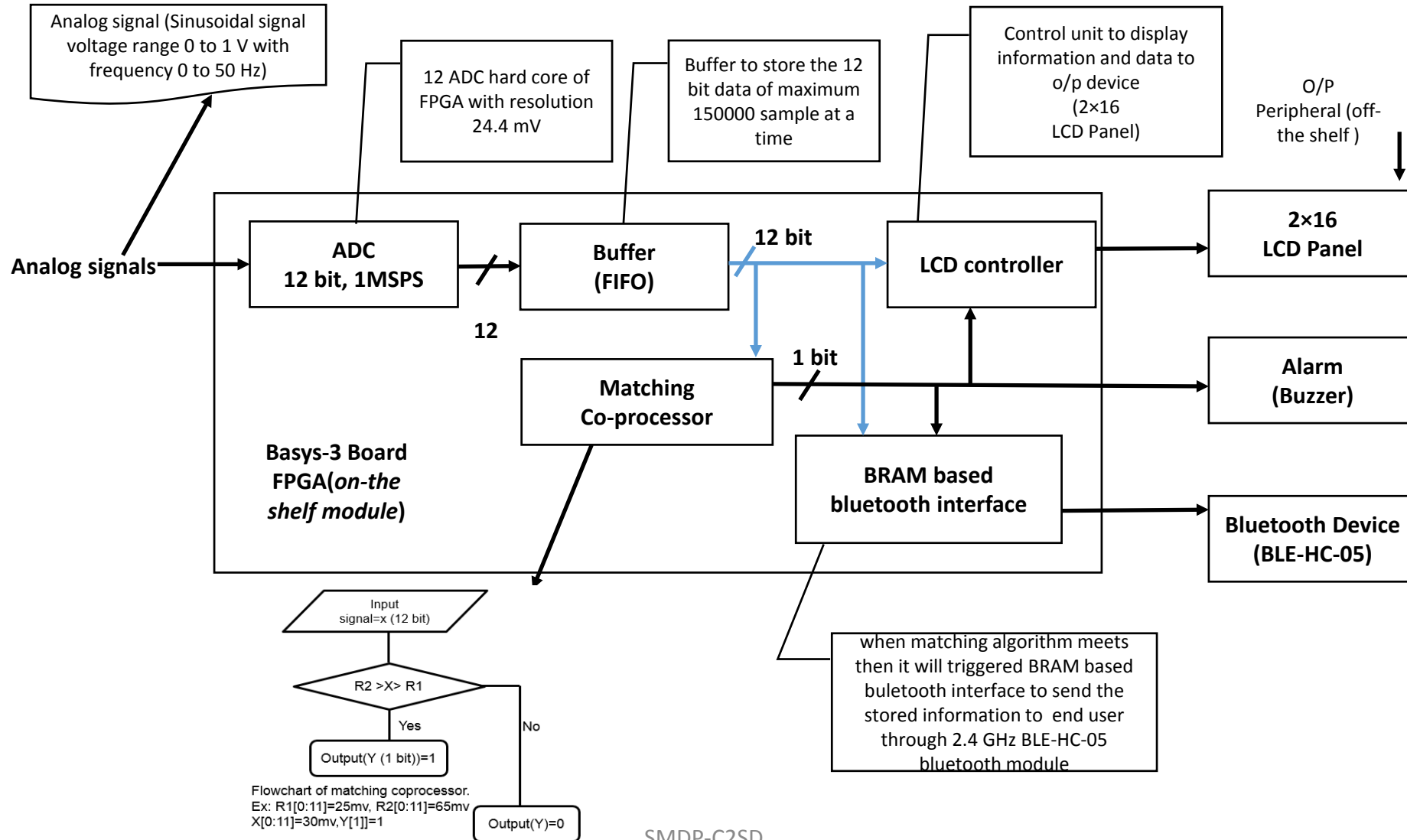


FPGA board level integration of module (Cluster part of NIT-Uttarakhand)



Synthesized result

Flow Navigator

PROJECT MANAGER

Settings

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

Open Elaborated Design

SYNTHESIS

Run Synthesis

Open Synthesized Design

IMPLEMENTATION

Run Implementation

Open Implemented Design

PROGRAM AND DEBUG

Generate Bitstream

Open Hardware Manager

PROJECT MANAGER - iitrmain

Sources

All the netlist used for the system (Integrated module)

Design Sources (7)

nituk_cluster_main (nituk_cluster_main.v) (4)

adc12bit : test_only_adc (test_only_adc.v) (2)

VTH : vth_threshold (range_vth.v)

lcdtext : complete_LCD_TOP(controller) (lcd_top.vhd) (1)

ble : bram_tx (bram_tx.v) (3)

clock_divider (clock_divider.v)

xadc_wiz_0 (xadc_wiz_0.xci)

xadc_wiz_1 (xadc_wiz_1.xci)

LCD_program_PIA(lcd_driver) (lcd_with_data.vhd)

(integer_to_lcd.vhd)

Hierarchy

IP Sources

Libraries

Compile Order

Properties

Select an object to see properties

Project Summary

Overview | Dashboard

Product family: Artix-7

Project part: xc7a35tcpg236-1

Top module name: nituk_cluster_main

Target language: Verilog

Simulator language: Vivado

Synthesis

Status: Complete

Messages: 7 warnings

Active run: synth_1

Part: xc7a35tcpg236-1

Strategy: Vivado Synthesis Defaults

Report Strategy: Vivado Synthesis Default Reports

Incremental synthesis: None

Implementation

Status: Complete

Messages: 2 warnings

Active run: impl_1

Part: xc7a35tcpg236-1

Strategy: Vivado Implementation Defaults

Report Strategy: Vivado Implementation Default Reports

Incremental implementation: None

DRC Violations

Summary: 2 warnings

Implemented DRC Report

Timing

Setup | Hold | Pulse Width

Worst Negative Slack (WNS): 1.356 ns

Total Negative Slack (TNS): 0 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 2012

Implemented Timing Report

Utilization

Post-Synthesis | Post-Implementation

Power

Summary | On-Chip

Tcl Console | Messages | Log | Reports | Design Runs

Name

Constraints

Status

WNS

TNS

WHS

THS

TPWS

Total Power

Failed Routes

LUT

FF

BRAM

URAM

DSP

Start

Elapsed

Run Strategy

Report

synth_1 (active)

constrs_1

Synthesis Out-of-date

312

115

0.0

0

0

10/12/20, 2:12 AM

00:00:45

Vivado Synthesis Defaults (Vivado Synthesis 2017)

Vivado

impl_1

constrs_1

Implementation Out-of-date

1.356

0.000

0.082

0.000

0.000

0.091

0

548

242

44.5

0

0

10/12/20, 2:13 AM

00:01:55

Vivado Implementation Defaults (Vivado Implementation 2017)

Vivado

Out-of-Context Module Runs

fifo_generator_1_synth_1

fifo_generator_1

synth_design Complete!

8/10/20, 3:06 PM

00:01:31

Vivado Synthesis Defaults (Vivado Synthesis 2020)

Vivado

xadc_wiz_0_synth_1

xadc_wiz_0

synth_design Complete!

0

0

0.0

0

0

8/10/20, 3:06 PM

00:00:52

Vivado Synthesis Defaults (Vivado Synthesis 2020)

Vivado

blk_mem_gen_0_synth_1

blk_mem_gen_0

synth_design Complete!

10/9/20, 12:31 AM

00:01:04

Vivado Synthesis Defaults (Vivado Synthesis 2020)

Vivado

xadc_wiz_2_synth_1

xadc_wiz_2

Synthesis Out-of-date

0

0

0.0

0

0

10/9/20, 12:31 AM

00:00:42

Vivado Synthesis Defaults (Vivado Synthesis 2020)

Vivado

Integration of modules for Data acquisitions (DAQ):

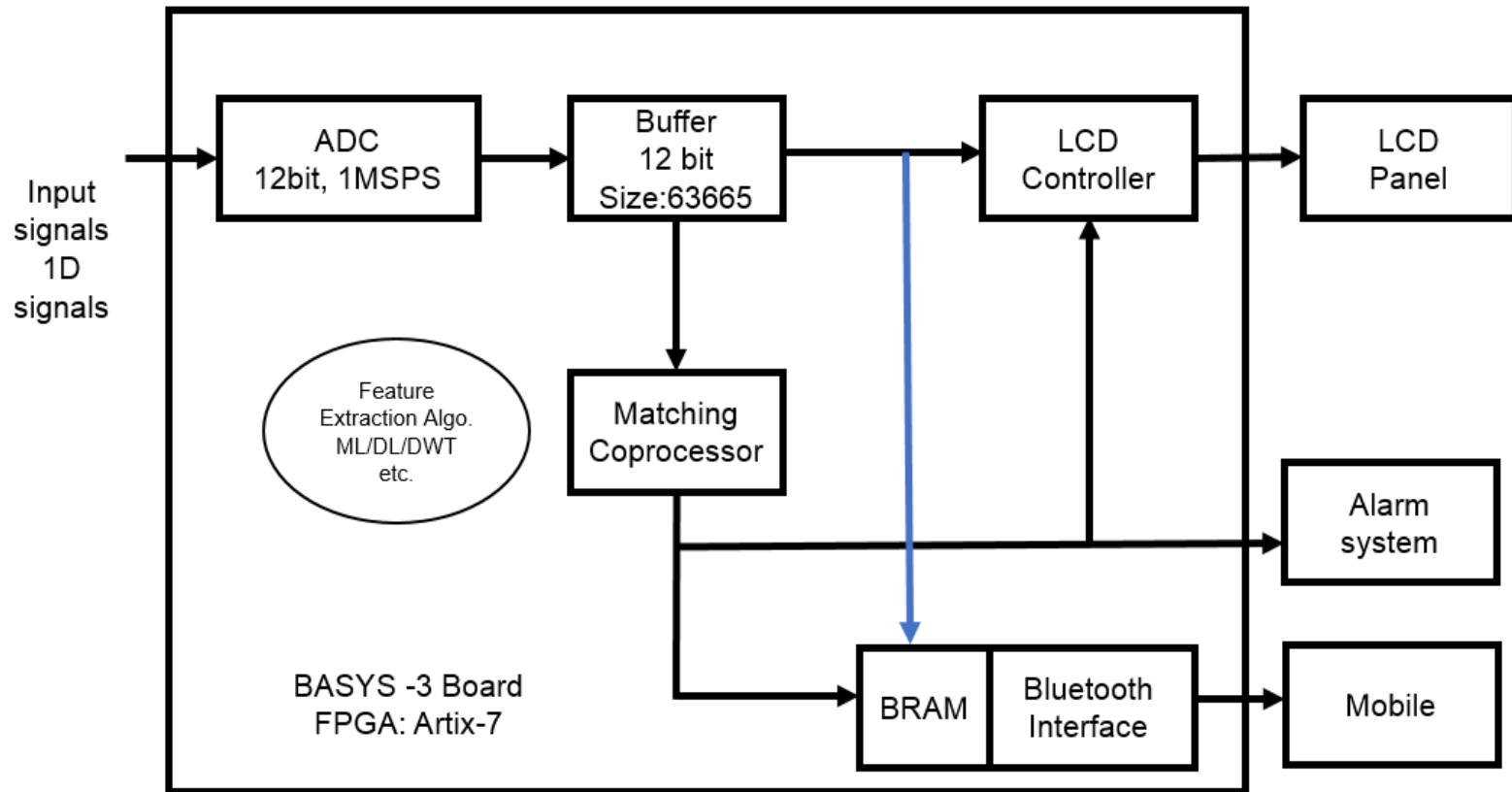


Fig.21: Block diagram of DAQ

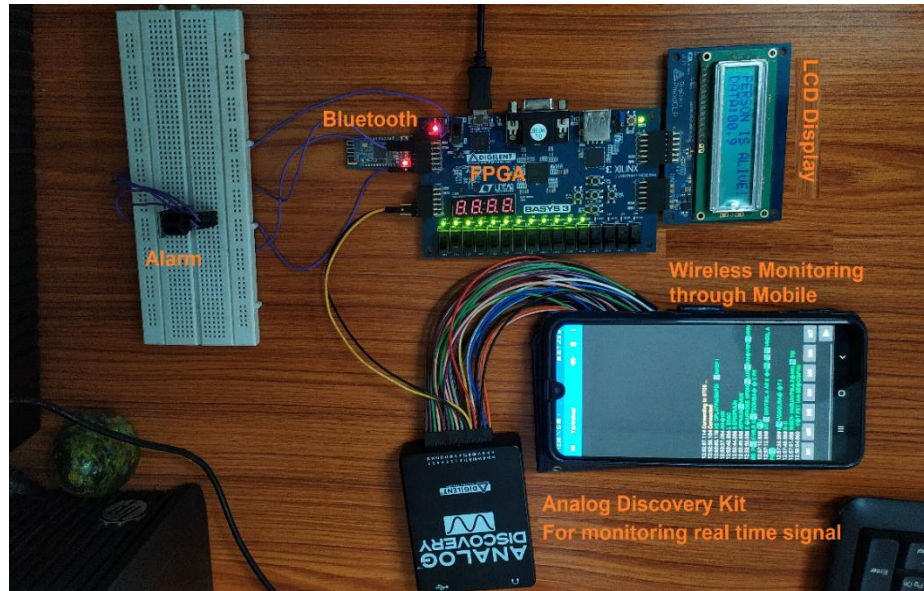


Fig.22: Real-time implementation DAQ

Resource	Utilized	Available
LUT	355	208000
FF	243	41600
BRAM	44.50	50
IO	33	106

Fig.23: Resource utilization

Total power consumption=83 mW

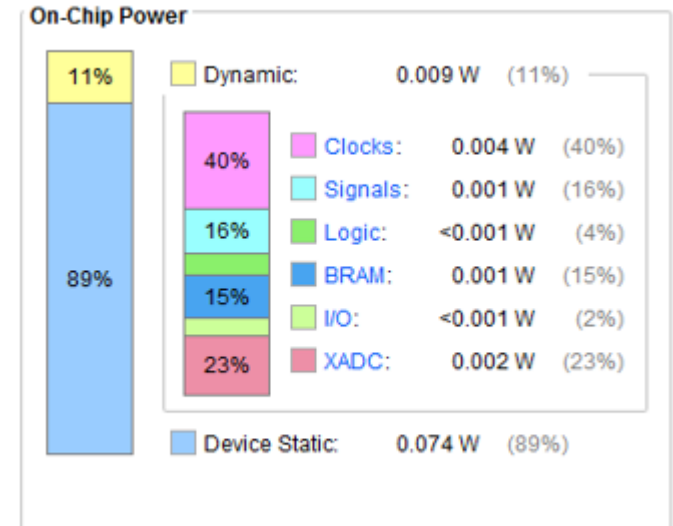


Fig.24: Power analysis of DAQ

Maximum operating Frequency=0.182 GHz

Setup Slack	Hold Slack	Pulse width
1.407ns	0.043na	5.5ns

Fig.25: Timing analysis