Variable Dependency Extractor Development

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DC Evaluation

CONTENT

Cone of Influence

The Cone of Influence refers to the set of variables that can be influenced by a given variable within a digital circuit. The Cone of Influence captures the downstream impact of a variable within a course.

For eg:- If there is a signal A that drives the inputs of multiple gates, and those gates further drive other gates and signals in the circuit, the COI of signal A would include all the gates and signals that the changes can influence in signal A.

Cone of Dependency

The Cone of Dependency(COD) refers to the set of variables that directly or indirectly influence a given variable within a digital circuit. The COD captures the upstream dependencies of a variable within a circuit.

For eg:- If there is a signal Z that is driven by multiple inputs, and those inputs are dependent on other gates and signals in the circuit, the COD of signal Z would include all the gates and signals that contribute to the value of signal Z.

CODE BRIEFING

- The code includes necessary header files and declares several sets and maps to store variables, operators, keywords, and dependencies.

- There are utility functions like if_variable, operator_check, keyword_check, var_num, variable_check, and number_check that are used to identify variables, operators, keywords, and numbers within the Verilog code.

CODE BRIEFING

- The read_line function is the main function that processes each line of the Verilog code. It splits the line into tokens and performs various checks to identify variables, keywords, operators, and other elements. It also updates the dependency information based on variable assignments.

CODE BRIEFING

- The COI_bfs function performs a breadth-first search to find the dependencies of a given variable. It starts from the specified variable and traverses its dependencies in a level-by-level manner. The dependencies are stored in a string and printed as output.

- The removeComments function is a helper function that removes comments from the Verilog code using simple string manipulation.

THANK'S FOR WATCHING

The output of the code is given in Report