University of Central Florida

Department of Computer Science

CDA 5106: Fall 2020

Machine Problem 1: Cache Design, Memory Hierarchy Design

by

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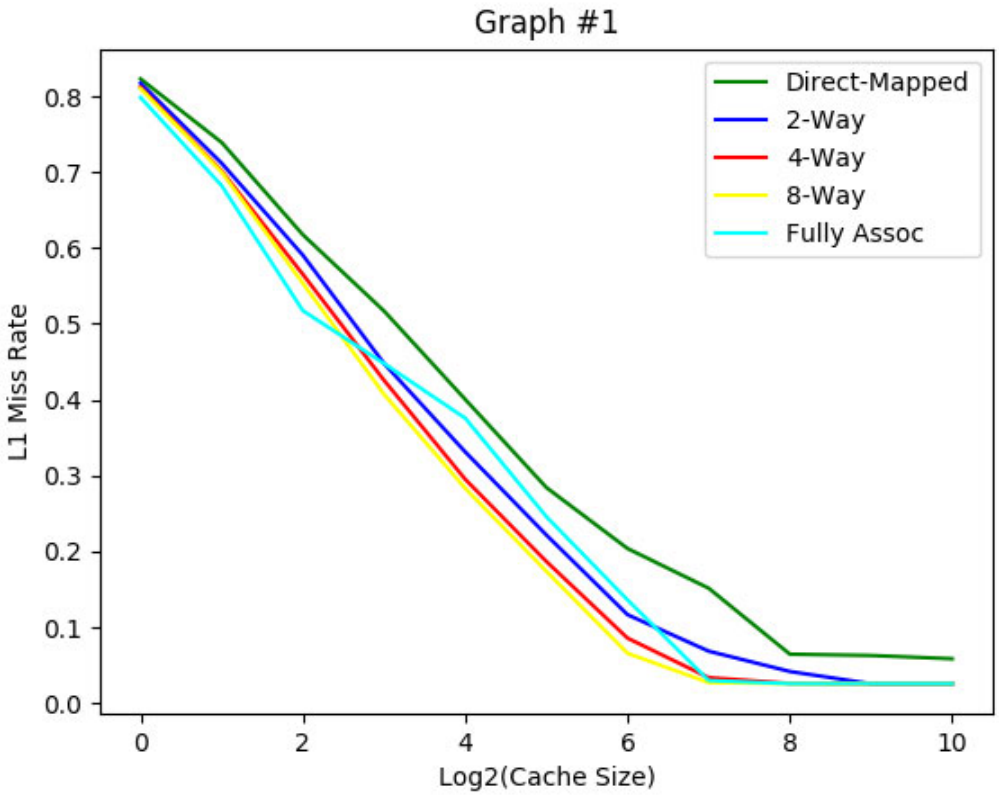
Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

Student's electronic signature: Rajib Dey

8.1. L1 cache exploration: SIZE and ASSOC

GRAPH #1

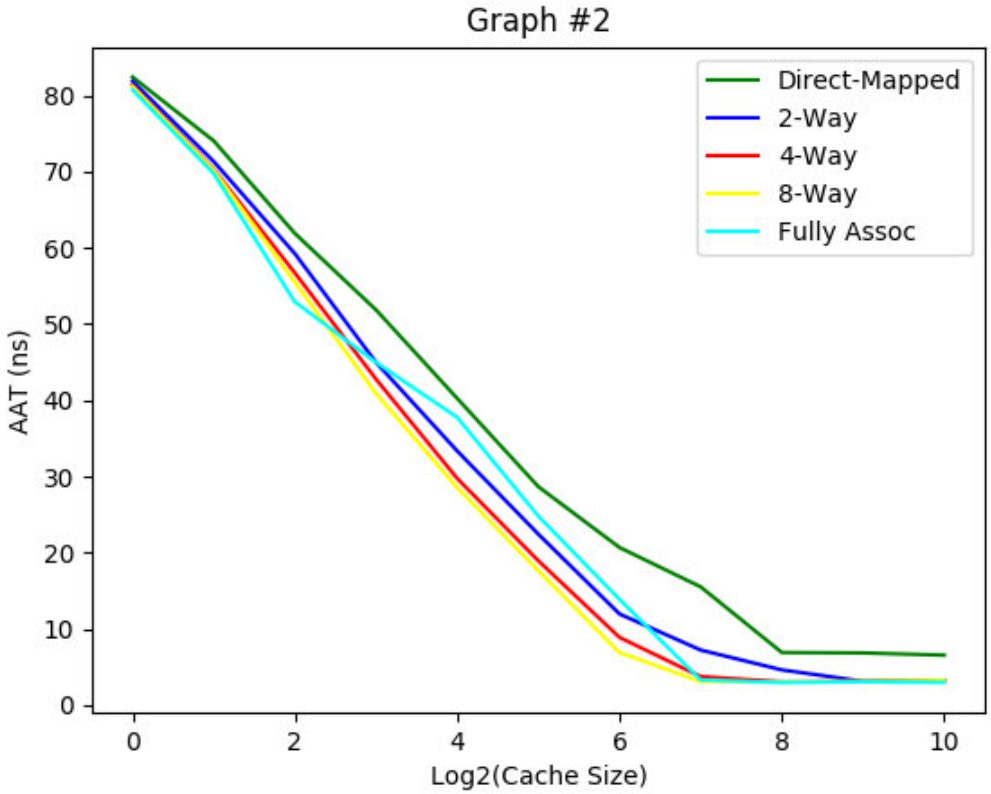


Discussion:

1. For any given associativity, increasing the cache size reduces the miss rate. Which is very much visible from the graph as we can see the miss rate going down while we increase the cache size on the x-axis.

   For any given cache size, increasing the associativity results in reducing the miss rate. It is also visible from the graph that, if the cache size is large increasing the associativity does not affect the miss rate that much.
2. Estimated Compulsory miss rate = 0.0258
3. Estimated conflict miss rate can be calculated by subtracting compulsory miss rate from the miss rate. The results are the following:
   I. Direct-mapped: 0.79696
   II. 2-way: 0.79121
   III. 4-way: 0.78598
   IV. 8-way: 0.78425
   V. Fully-associative: 0.78218

GRAPH #2

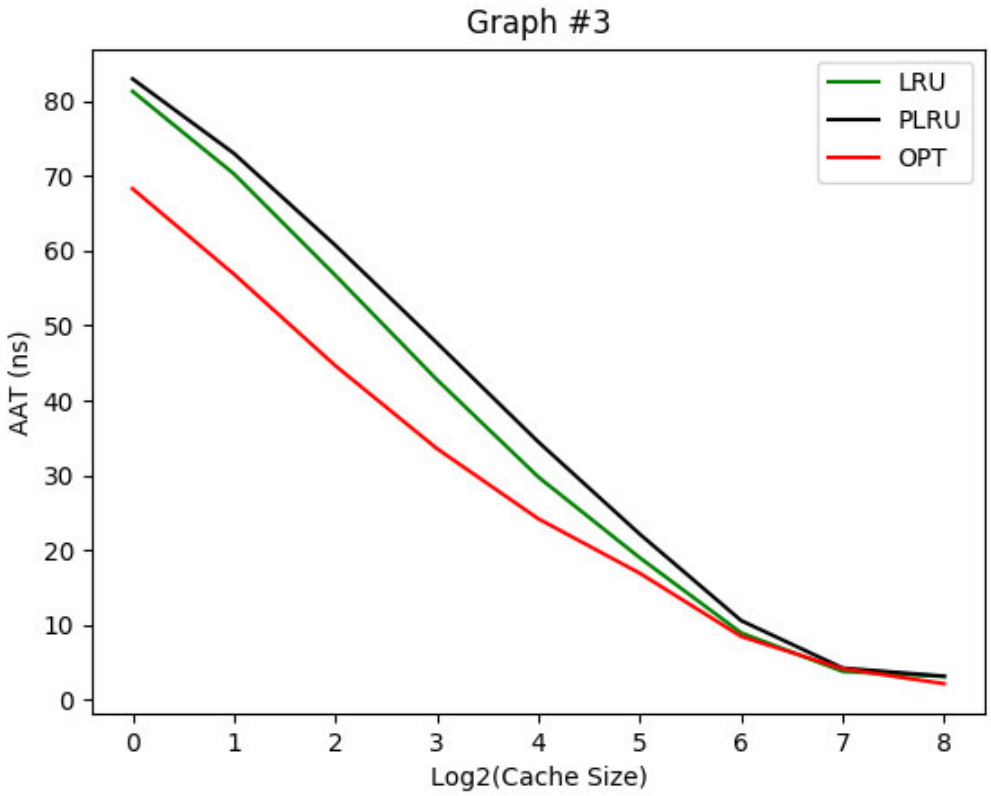


Discussion:

For a memory hierarchy with only an L1 cache and blocksize 32, Fully Associative cache will give us the lowest AAT. This is in sync with the understanding that higher associativity will lead to lower AAT.

8.2. Replacement policy study

GRAPH #3

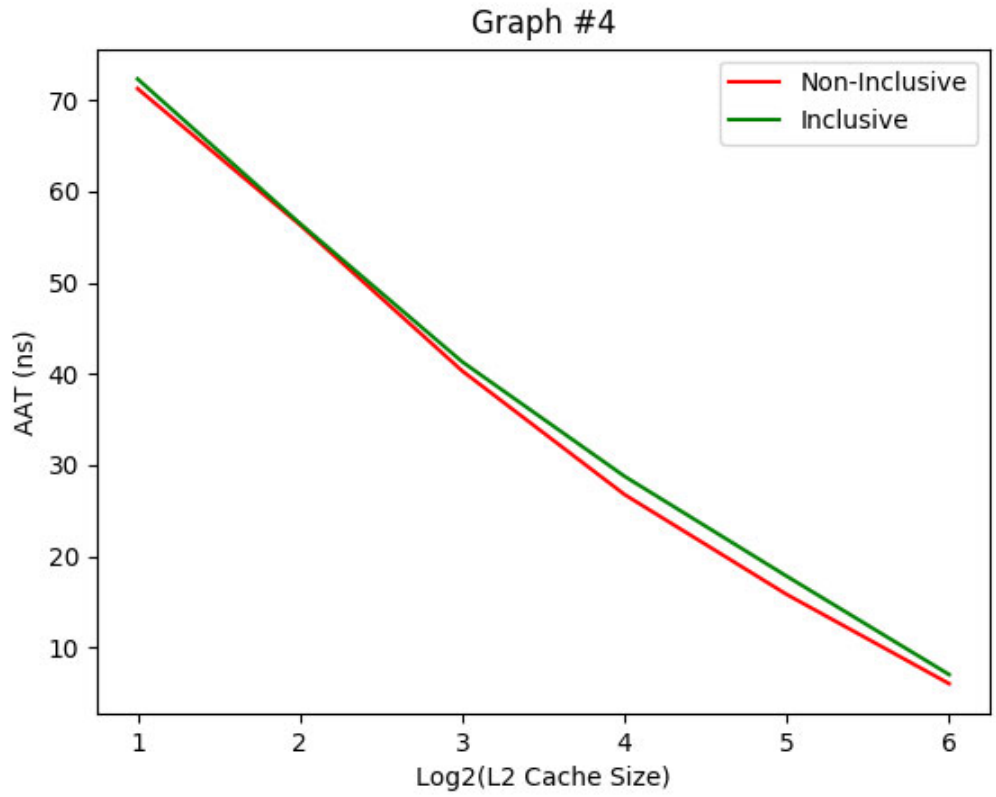


Discussion:

By definition, Optimal policy will give us the lowest AAT, even though it is not possible to implement this in real life. My simulator for the optimal policy confirms that theory, which is also visible from the graph. It is also visible from the graph that, if you increase the cache size, optimal policy becomes less and less effective.

8.3. Inclusion property study

GRAPH #4



Discussion:

The trend in the graph clearly tells us that, the non-inclusive inclusion property will give us lower AAT when compared to inclusive inclusion property.