Single-Stage Amplifier Design and Analysis

Rajinthan Rameshkumar

September 7, 2025

Introduction

Single-stage CMOS amplifiers are fundamental building blocks in analog IC design. In this report, we design and analyze three configurations of the Common Source (CS) amplifier using Skywater 130nm technology: resistive load, PMOS current source load, and current mirror (active) load. The objective is to maximize the Gain Bandwidth Product (GBW) while meeting the given specifications.

Project Requirements

- Supply Voltage (V_{DD}): 1.8 V
- Input Common-Mode Voltage: 0.9 V
- Minimum DC Gain: ≥ 40 dB
- Output Swing: 0.2–1.6 V
- Load Capacitance: 7 pF
- Unity Gain Bandwidth: 80 MHz

Initial Calculations

The given technology parameters for nMOS and pMOS are:

Parameter	nMOS	pMOS
V_{th} (V)	0.49439	-1.0652
μ_0 (cm^2/V·s)	301.97	124.424
t_{ox} (nm)	4.148	4.23
λ (V^{-1})	0.0381	0.0696

Table 1: Technology parameters used for calculations

The permittivity of oxide is given by:

$$\varepsilon_{ox} = \varepsilon_r \cdot \varepsilon_0 = 3.9 \times 8.8541 \times 10^{-12}\ F/m = 3.453 \times 10^{-11}\ F/m$$

The oxide capacitance per unit area is:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

For nMOS:

$$C_{ox,n} = \frac{3.453 \times 10^{-11}}{4.148 \times 10^{-9}} = 8.325 \times 10^{-3}\ \frac{F}{m^2}$$

For pMOS:

$$C_{ox,p} = \frac{3.453 \times 10^{-11}}{4.23 \times 10^{-9}} = 8.163 \times 10^{-3}\ \frac{F}{m^2}$$

Next, the output resistance required for the frequency response is calculated using:

$$f_{\text{pole}} = \frac{f_u}{A_v'} \qquad \Rightarrow \qquad R_o = \frac{1}{2\pi f_{\text{pole}} C_L} = \frac{A_v'}{2\pi f_u C_L}$$

Substituting the given values:

$$f_u = 80\,\text{MHz}, \quad C_L = 7\,\text{pF}, \quad A_v' = 100$$

$$R_o = \frac{100}{2\pi(80 \times 10^6)(7 \times 10^{-12})} = 2.84 \times 10^4\ \Omega$$

Thus, the output resistance required to be less than:

$$\boxed{R_o \approx 28.4\ k\Omega}$$

to make sure f_u be greater than 1MHz.

Design of Common Source Amplifiers

1 Resistive Load

1.1 Schematic

The schematic of the resistive-load common source amplifier is shown in Fig. 1.

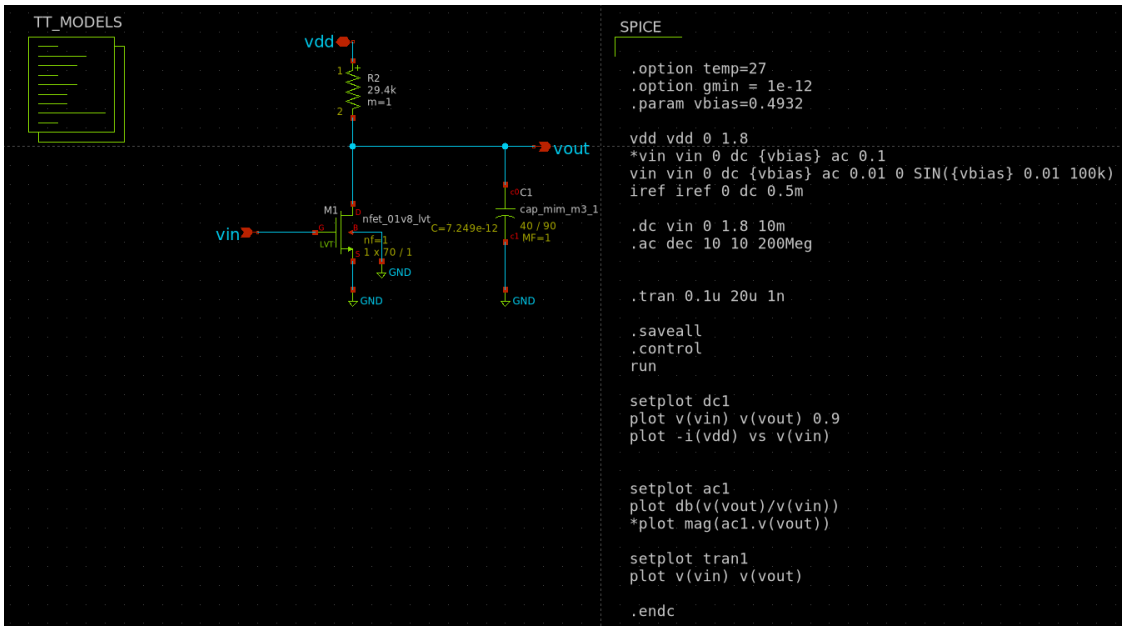

Figure 1: Xschem setup of resistive-load NFET amplifier.

For the resistive-load NFET configuration the design bias current is given by the relation provided:

$$I_B = \frac{1}{R_0\left(\lambda_n + \dfrac{1}{0.9}\right)}.$$

Using

$$R_o = 2.84 \times 10^4\ \Omega, \qquad \lambda_n = 0.0381,$$

we evaluate the denominator:

$$\lambda_n + \frac{1}{0.9} = 0.0381 + 1.111111\ldots = 1.149211\ldots$$

so

$$I_B = \frac{1}{(2.84 \times 10^4) \times 1.149211} = 3.06395 \times 10^{-5}\ \text{A}.$$

$$\boxed{I_B \approx 3.06 \times 10^{-5}\ \text{A} = 30.6\ \mu\text{A}.}$$

Load resistor for NFET resistive-load configuration

Choose the DC output operating point at mid-rail:

$$V_{out} = \frac{V_{DD}}{2} = 0.9 \text{ V}.$$

The load resistor R that sets the bias current I_B is:

$$R = \frac{V_{DD} - V_{out}}{I_B}.$$

With $V_{DD} = 1.8$ V, $V_{out} = 0.9$ V and $I_B \approx 3.06 \times 10^{-5}$ A,

$$R = \frac{0.9}{3.06395 \times 10^{-5}} \approx 2.94 \times 10^4 \ \Omega.$$

$$\boxed{R \approx 29.4 \text{ k}\Omega}$$

Next, the required transconductance (from the midband gain target) is

$$g_m = \frac{A_v'}{R_o}.$$

For $A_v' = 100$,

$$g_m = \frac{100}{2.84 \times 10^4} = 3.52113 \times 10^{-3} \text{ S} = 3.521 \text{ mS}.$$

$$\boxed{g_m \approx 3.52 \text{ mS}}$$

The NMOS aspect ratio for M1 is then approximated by the square-law relation (first-order estimate):

$$\left(\frac{W}{L}\right)_1 = \frac{g_m}{\mu_{0,n} C_{ox,n} (V_{GS1} - V_{th,n})} = \frac{g_m}{\mu_{0,n} C_{ox,n} V_{OV}}.$$

Use:

$$\mu_{0,n} = 301.97 \ \frac{\text{cm}^2}{\text{V} \cdot \text{s}} = 0.030197 \ \frac{\text{m}^2}{\text{V} \cdot \text{s}}, \quad C_{ox,n} = 8.325 \times 10^{-3} \ \frac{\text{F}}{\text{m}^2}.$$

- For $V_{OV} = 0.20$ V:

$$\left(\frac{W}{L}\right)_1 = \frac{3.52113 \times 10^{-3}}{0.030197 \times 8.325 \times 10^{-3} \times 0.20} \approx 70.03.$$

$$\boxed{\left(\frac{W}{L}\right)_1 \approx 70.03 \quad (V_{OV} = 0.20 \text{ V}).}$$

1.2 DC Operating Point

The DC operating point simulation is used to verify device biasing. A gate bias voltage of

$$V_G = 0.4932V$$

was applied to ensure that the NMOS operates in saturation. The operating point results are shown in Fig. 2.

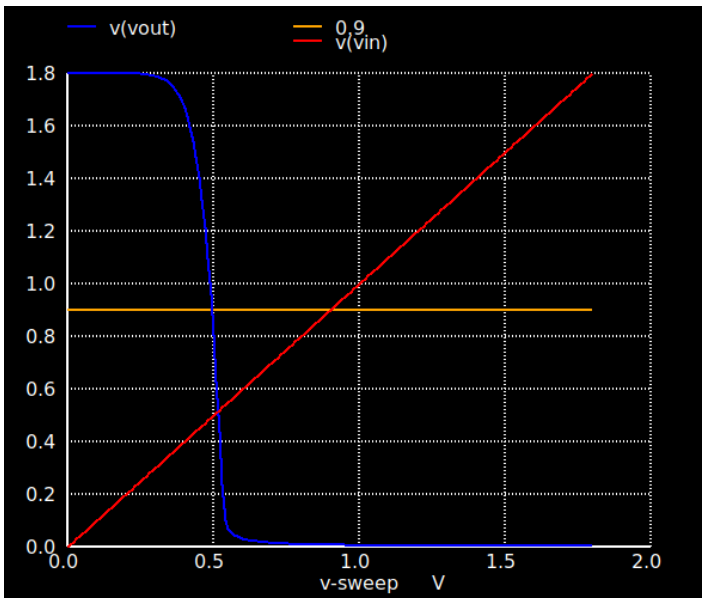

Figure 2: DC operating point analysis of resistive-load NFET amplifier.

1.3 AC Analysis

The small-signal AC analysis was performed with the amplifier biased at $V_G = V_{\text{bias}}$. The resulting gain versus frequency plot is shown in Fig. 3. From this plot, the DC gain A_{DC} and the unity gain frequency f_u were extracted.

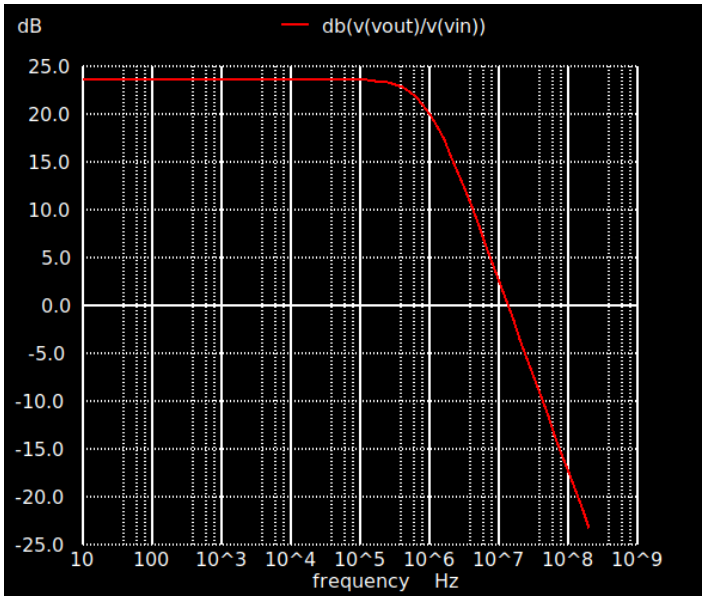

Figure 3: AC analysis and gain plot of resistive-load NFET amplifier.

The Gain-Bandwidth Product (GBW) is calculated as:

$$GBW = A_{DC} \cdot f_u$$

For this design:

$$\boxed{GBW = 13.38MHz}$$

1.4 Transient Analysis

A small-signal transient simulation was carried out using a sinusoidal input:

$$V_{in}(t) = \text{SIN}(V_{\text{bias}},\ 0.01,\ 100k)$$

The time-domain output response is shown in Fig. 4.

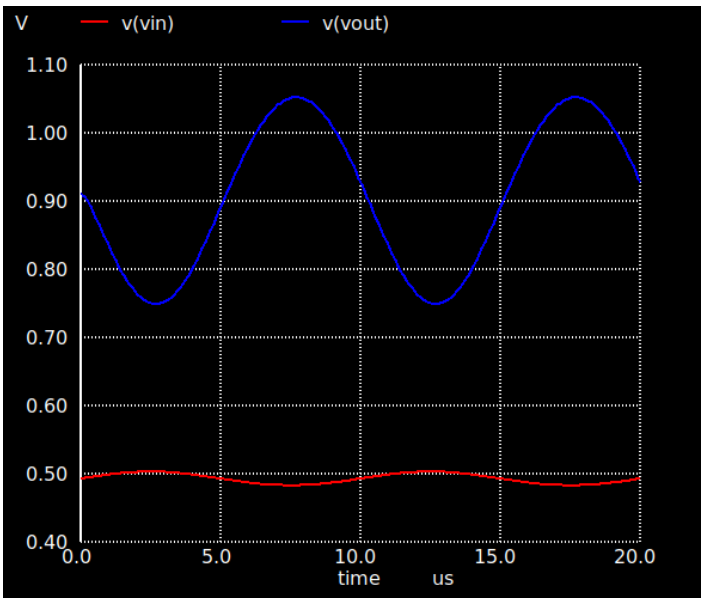

Figure 4: Transient simulation of resistive-load NFET amplifier with sinusoidal input.

2 PMOS Current Source Load

2.1 Schematic

The schematic of the common source amplifier with a PMOS current source load is shown in Fig. 5.

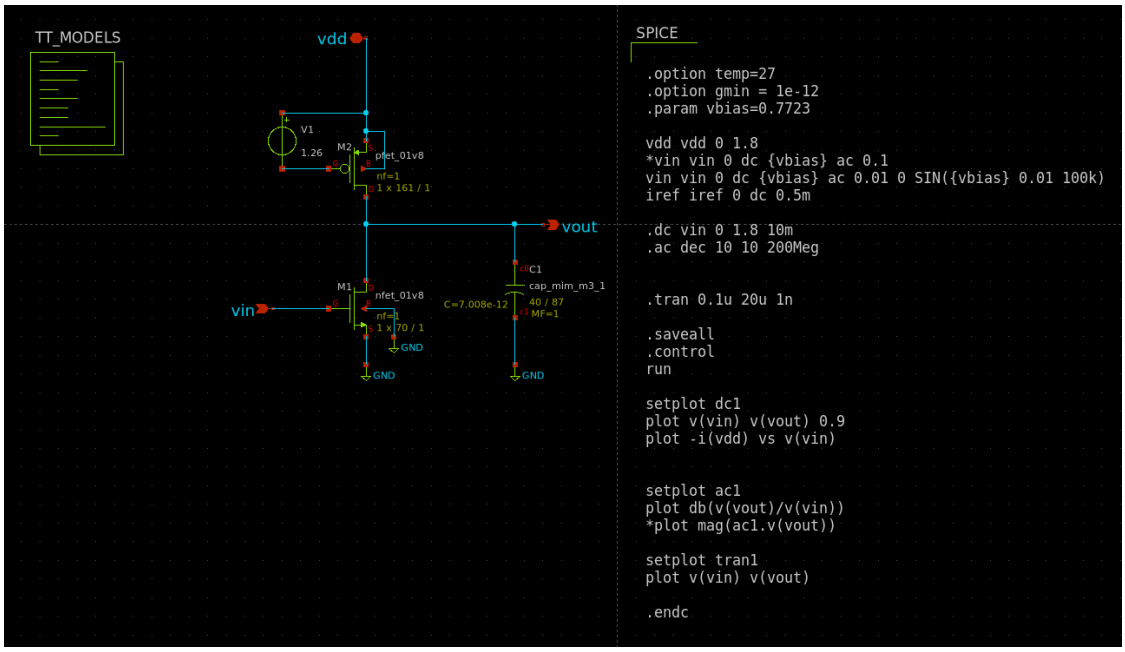

Figure 5: Xschem setup of CS amplifier with PMOS current source load.

Bias current and device sizing

Using the derived output resistance:

$$R_o \approx 2.84 \times 10^4\ \Omega$$

and the channel-length modulation parameters:

$$\lambda_n = 0.0381, \qquad \lambda_p = 0.0696,$$

the required bias current is

$$I_{\text{bias}} = \frac{1}{(\lambda_n + \lambda_p) R_o}.$$

Substituting numbers:

$$\lambda_n + \lambda_p = 0.0381 + 0.0696 = 0.1077$$

$$I_{\text{bias}} = \frac{1}{0.1077 \times 2.84 \times 10^4} = 3.26938 \times 10^{-4} \text{ A}$$

so

$$\boxed{I_{\text{bias}} \approx 3.27 \times 10^{-4} \text{ A} = 327 \ \mu\text{A}.}$$

To satisfy the maximum output voltage constraint the drain-source voltage of M2 must be

$$V_{DS2} = V_{DD} - V_{out,\max} = 1.8 - 1.6 = 0.2 \text{ V}.$$

The aspect ratio for M2 is given by the long-channel square-law approximation:

$$\left(\frac{W}{L}\right)_2 = \frac{2 I_{\text{bias}}}{\mu_{0,p} \, C_{ox,p} \, V_{DS2}^2}.$$

Use the process parameters:

$$\mu_{0,p} = 124.424 \text{ cm}^2/\text{V} \cdot \text{s} = 124.424 \times 10^{-4} \text{ m}^2/\text{V} \cdot \text{s} = 0.0124424 \ \frac{\text{m}^2}{\text{V} \cdot \text{s}},$$

$$C_{ox,p} = 8.163 \times 10^{-3} \ \frac{\text{F}}{\text{m}^2}, \qquad V_{DS2} = 0.2 \text{ V}.$$

Substituting:

$$\left(\frac{W}{L}\right)_2 = \frac{2 \times 3.26938 \times 10^{-4}}{0.0124424 \times 8.163 \times 10^{-3} \times (0.2)^2} \approx 1.6095 \times 10^2.$$

Thus

$$\boxed{\left(\frac{W}{L}\right)_2 \approx 161.}$$

Finally, the aspect ratio of M1 is related to the required transconductance g_m. Using

$$g_m = \frac{A_v'}{R_o},$$

and

$$\left(\frac{W}{L}\right)_1 = \frac{g_m}{\mu_{0,n} \, C_{ox,n} \, (V_{GS1} - V_{th,n})},$$

we proceed as follows. With the design midband gain target $A_v' = 100$,

$$g_m = \frac{100}{2.84 \times 10^4} = 3.52113 \times 10^{-3} \text{ S} = 3.521 \text{ mS}.$$

Process values:

$$\mu_{0,n} = 301.97 \text{ cm}^2/\text{V} \cdot \text{s} = 0.030197 \ \frac{\text{m}^2}{\text{V} \cdot \text{s}}, \qquad C_{ox,n} = 8.325 \times 10^{-3} \ \frac{\text{F}}{\text{m}^2}.$$

We must choose an overdrive $V_{OV} = V_{GS1} - V_{th,n}$.

- For $V_{OV} = 0.20$ V:

$$\left(\frac{W}{L}\right)_1 = \frac{3.52113 \times 10^{-3}}{0.030197 \times 8.325 \times 10^{-3} \times 0.20} \approx 70.0.$$

$$\boxed{\left(\frac{W}{L}\right)_1 \approx 70 \quad \text{for } V_{OV} = 0.20 \text{ V}.}$$

2.2 DC Operating Point Analysis

The DC operating point simulation was carried out to ensure correct device biasing of both NMOS and PMOS transistors. A gate bias voltage of

$$V_G = 0.7723V$$

was applied at the input. The operating point voltages and currents are shown in Fig. 6.

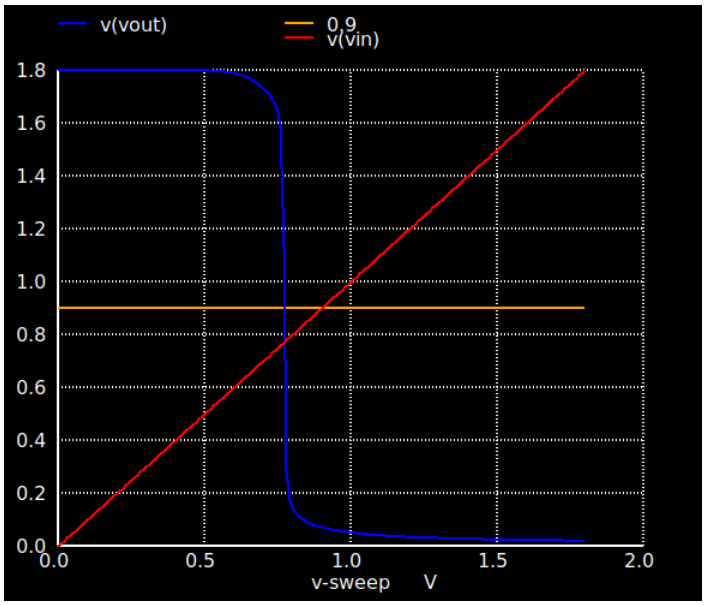

Figure 6: DC operating point analysis of CS amplifier with PMOS current source load.

2.3 AC Analysis

The small-signal AC analysis is used to extract the low-frequency gain A_{DC}, cutoff frequency f_c, and unity gain bandwidth f_u. The gain plot obtained is shown in Fig. 7.

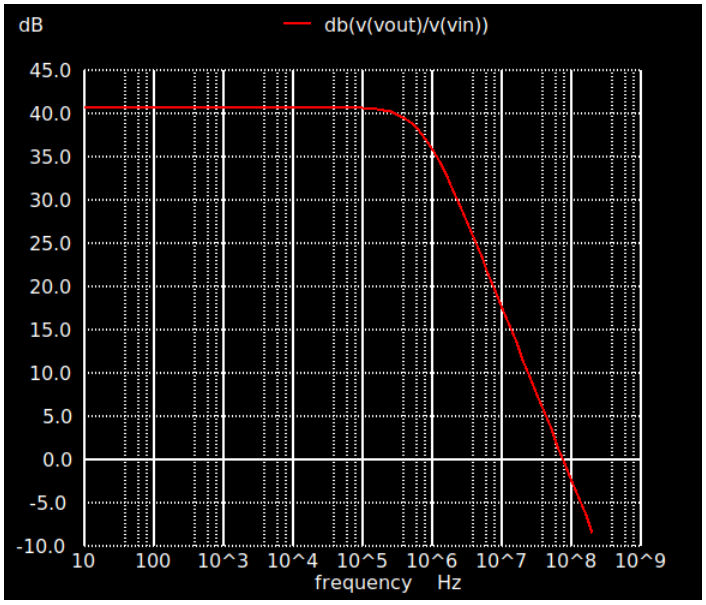

Figure 7: AC analysis and gain plot of CS amplifier with PMOS current source load.

The Gain-Bandwidth Product (GBW) is given by:

$$GBW = A_{DC} \cdot f_u$$

For this configuration:

$$\boxed{GBW = 75.4MHz}$$

2.4 Transient Analysis

A small-signal transient simulation was performed using a sinusoidal input:

$$V_{in}(t) = \text{SIN}(V_{\text{bias}},\ 0.01,\ 100k)$$

The time-domain output waveform is shown in Fig. 8.

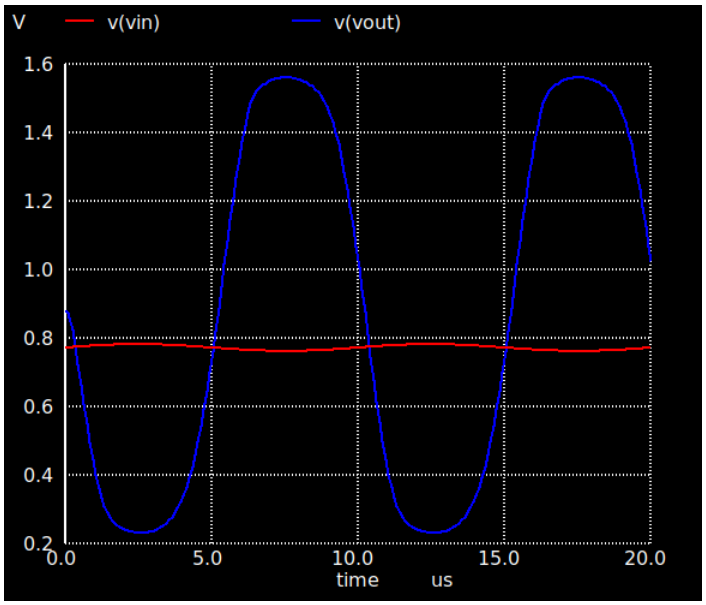

Figure 8: Transient simulation of CS amplifier with PMOS current source load.

3 Active Current Mirror Load

The active current mirror load uses PMOS transistors identical to the PMOS current source configuration. The reference transistor is driven by an external current source of $I_{ref} = 327\,\mu\text{A}$. The output transistor mirrors this current to act as an active load.

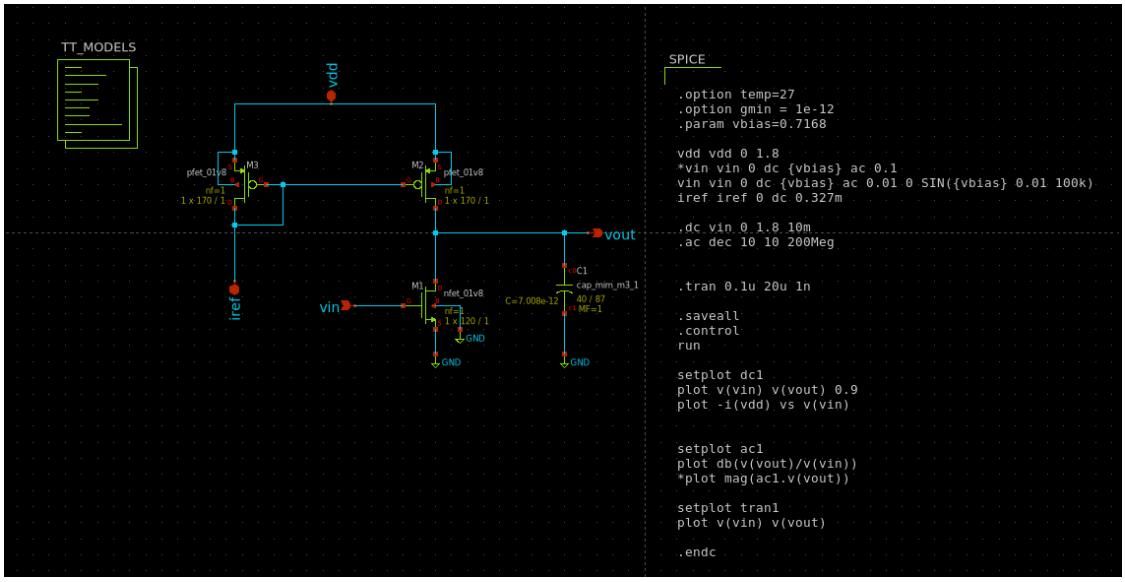

Figure 9: Active PMOS Current Mirror Load Schematic.

3.1 DC Operating Point Analysis

The operating point analysis shows the gate-source voltage required to sustain the reference current and the corresponding drain currents in both transistors.

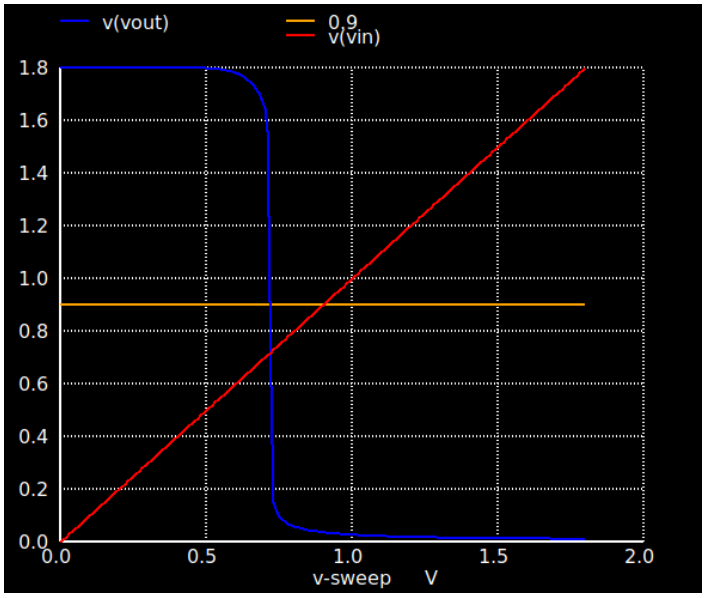

Figure 10: Operating Point (DC) Analysis. Reference Current: 327 μA.

3.2 AC Analysis

AC analysis was performed to observe the small-signal behavior of the active load. The output transistor provides a high output resistance, increasing the voltage gain of the stage.

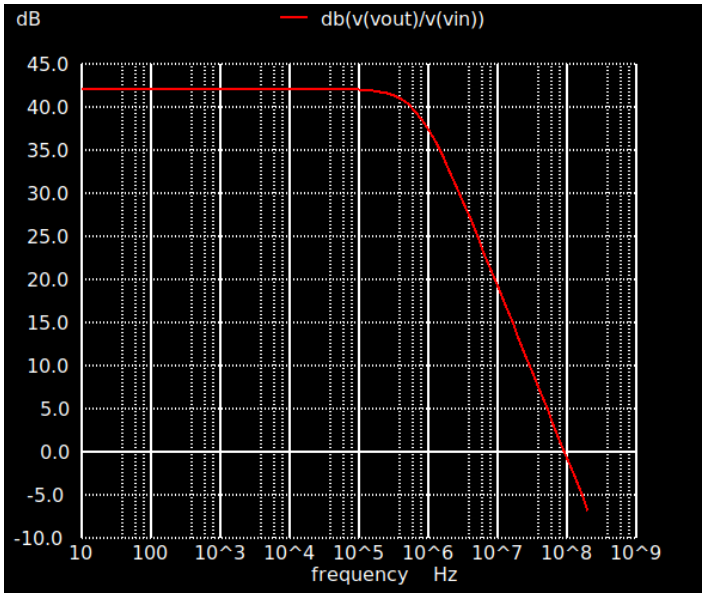

Figure 11: AC Analysis of Active Current Mirror Load.

For this configuration:

$$\boxed{GBW = 90.1MHz}$$

3.3 Transient Analysis

A transient analysis with a small sinusoidal signal on the gate of the reference transistor shows the mirrored response at the output transistor.

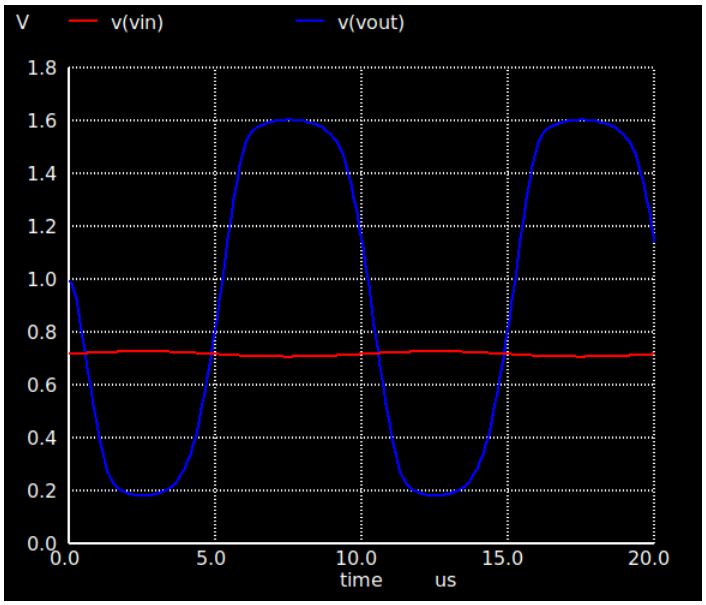

Figure 12: Transient Analysis with $I_{ref} = 327\,\mu$A.

Conclusion

The PMOS active current mirror load successfully mirrors the $327uA$ reference current, providing a high-resistance load suitable for high-gain amplifier stages. The use of identical PMOS transistors ensures minimal mismatch.

Layout

The layout of the designed common-source amplifier was implemented in `KLayout` using the `Sky130A` PDK. The schematic was first drawn in `Xschem` and exported as a SPICE netlist, which was then used as a reference for device placement and routing in KLayout.

Figure 13 shows the resulting layout. While the amplifier layout was completed, a number of **Design Rule Check (DRC)** violations remain unresolved. In particular, some metal spacing and via enclosure rules (e.g., `m1.3ab`, `m2.5`) were not fully satisfied. These violations were identified using KLayout's built-in DRC engine. The layout is still presented here to illustrate the physical implementation.

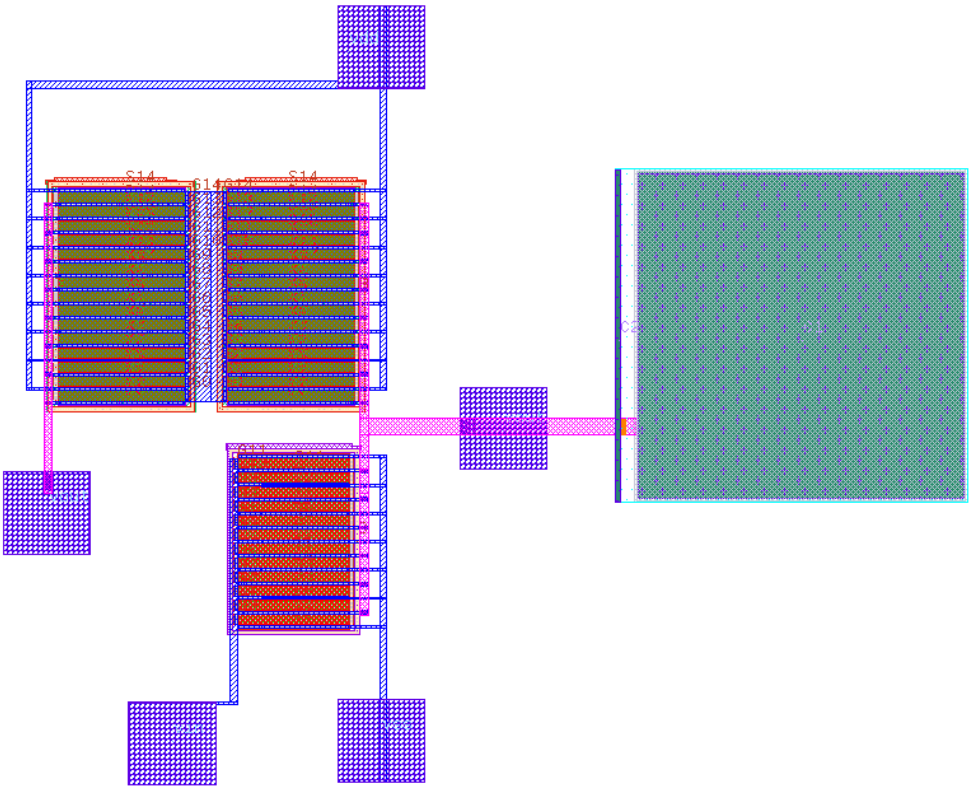

Figure 13: Layout of the common-source amplifier in KLayout (with some DRC violations).