A Low-power Single-ended Operational Amplifier using Sky130 PDK

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***Abstract*—This paper presents the design, simulation, and layout of a low-power, single-ended operational amplifier (op-amp) using the open-source SKY130 Process Design Kit (PDK). The op-amp is designed to function as a non-inverting unity-gain buffer for low-frequency analog signals in the $1\,\mathrm{kHz}$ to $10\,\mathrm{kHz}$ range. The design targets stringent specifications, including a low supply voltage range of $1.7\,\mathrm{V}$ to $1.9\,\mathrm{V}$, a quiescent current below $100\,\mu\mathrm{A}$, and a compact layout area within $140\,\mu\mathrm{m}$ x $80\,\mu\mathrm{m}$. The complete open-source design flow, utilizing Xschem for schematic entry, Ngspice for simulation, and KLayout for layout and verification, is employed. This report details the pre-layout and post-layout simulation results, including Process, Voltage, and Temperature (PVT) corner analysis and Monte Carlo simulations, to validate the design against all target specifications.**

***Index Terms*—CMOS, Analog IC Design, Operational Amplifier, SKY130, Low-Power, Single-Ended, Xschem, Ngspice, KLayout**

I. Introduction

Low-power operational amplifiers are fundamental building blocks in modern analog and mixed-signal integrated circuits, especially for low-voltage applications. This project focuses on the complete design and layout of a single-ended op-amp in the SKY130 $130\,\mathrm{nm}$ CMOS technology. The primary design objective is to create a stable unity-gain buffer for low-frequency ($1\,\mathrm{kHz}$–$10\,\mathrm{kHz}$) analog signals.

The design must meet a challenging set of specifications, including a DC gain greater than $60\,\mathrm{dB}$, a gain-bandwidth product (GBW) of at least $1\,\mathrm{MHz}$, and a phase margin (PM) greater than $60°$, all while driving a $25\,\mathrm{pF}$ load. This must be achieved across a supply range of $1.7\,\mathrm{V}$ to $1.9\,\mathrm{V}$ and a temperature range of $20\,°\mathrm{C}$ to $50\,°\mathrm{C}$, with a quiescent current under $100\,\mu\mathrm{A}$.

This report details the schematic design, pre-layout verification, physical layout, and post-layout verification, following the open-source design flow illustrated in the assignment.

II. Design Specifications

The target performance specifications for this project are provided by the assignment document and summarized in Table I. The op-amp must be stable while driving a $25\,\mathrm{pF}$ capacitive load and is biased by an external $5\,\mu\mathrm{A}$ sinking current source. The design also includes an enable (‘en‘) pin that, when low, must reduce the supply current to less than $2\,\mathrm{nA}$.

TABLE I: Target Performance Specifications

Parameter	Project Specification
Technology	$130\,\mathrm{nm}$ CMOS
Supply voltage V_{DD}	$1.7\,\mathrm{V}$ to $1.9\,\mathrm{V}$
Temperature range	$20\,°\mathrm{C}$ to $50\,°\mathrm{C}$
Output load C_L	$25\,\mathrm{pF}$ (capacitive)
DC Gain A_{DC}	$> 60\,\mathrm{dB}$
GBW	$\geq 1\,\mathrm{MHz}$
Phase Margin (PM)	$> 60°$
Quiescent Current (I_Q)	$< 100\,\mu\mathrm{A}$
Input Offset	$< 3\,\mathrm{mV}$
Slew Rate (SR)	$> 1\,\mathrm{V}\,\mu\mathrm{s}^{-1}$
Disable Current	$< 2\,\mathrm{nA}$
Final Layout Area	within $140\,\mu\mathrm{m} \times 80\,\mu\mathrm{m}$

III. Schematic Design and Biasing

The op-amp schematic, shown in Fig. 1, was designed in Xschem. It is a two-stage design, consisting of a differential pair as the first stage and a common source amplifier with a Miller capacitor as the second stage. The differential input stage provides high gain and common-mode rejection (CMRR). The common source amplifier serves as the second stage to provide additional voltage gain. The Miller capacitor is used for frequency compensation via pole splitting, which is essential to ensure stability when negative feedback is applied.

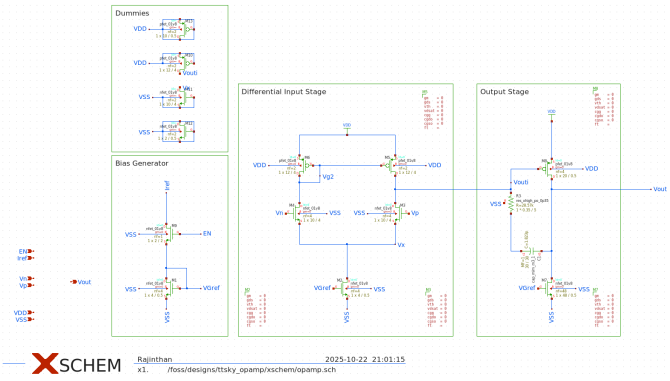


Fig. 1: Op-amp schematic designed in Xschem.

This work presents the design and layout for the CMOS Analog IC Design and Simulation ’25 course project.

IV. Pre-Layout Simulation Results

Pre-layout simulations were performed using Ngspice to verify the schematic against the specifications.

The testbench, shown in Fig. 2, was designed in Xschem.

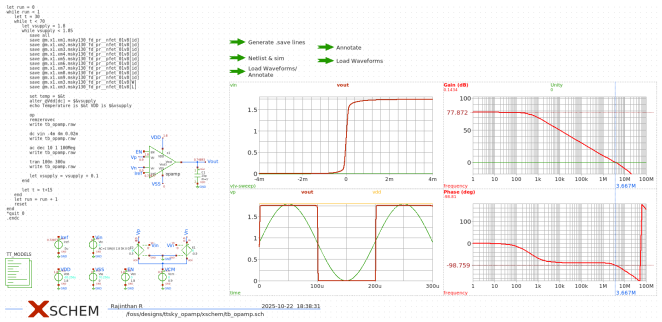
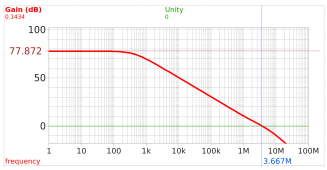


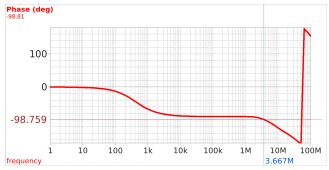
Fig. 2: Op-amp testbench designed in Xschem.

A. Nominal Performance

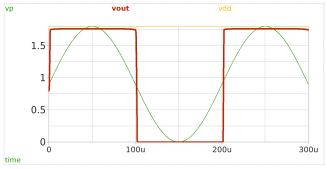
At nominal conditions (TT corner, 1.8 V, 27 °C), the op-amp satisfied all the requirements.



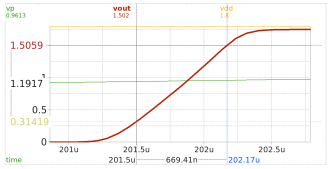
(a) AC Gain (Bode Plot)



(b) AC Phase (Bode Plot)



(c) Transient Step Response



(d) Slew Rate Measurement

Fig. 3: Nominal pre-layout simulation results (TT Corner, 1.8 V, 27 °C).

B. PVT and Corner Analysis

To ensure robust performance, the design was simulated across the specified voltage (1.7 V to 1.9 V) and temperature (20 °C to 50 °C) ranges for all five process corners (TT, FF, SS, SF, FS). The results are summarized in Table II.

TABLE II: Pre-Layout PVT Corner Simulation Summary

Parameter	Achieved (Min)	Achieved (Typ)	Achieved (Max)
DC Gain A_{DC} (dB)	*72.6*	*76.2*	*78.95*
GBW (MHz)	*3.67*	*3.78*	*4.17*
Phase Margin (PM) (°)	*80.22*	*81.1*	*81.38*
Gain Margin (GM)(dB)	*27.9*	*28.0*	*28.4*
Quiescent Current (I_Q) (µA)	*60.2*	*64.5*	*68.7*
Slew Rate (SR) (V µs^{-1})	*1.70*	*1.75*	*1.97*

C. Monte Carlo Simulation

A Monte Carlo simulation (1000 runs) was performed to analyze the impact of process mismatch on the input offset voltage. The specification requires the offset to be less than 3 mV. The resulting distribution is shown in Fig. 4. The mean (μ) offset was 32 µV and the standard deviation (σ) was 1.056 mV, resulting in a 3σ value of 3.16 mV.

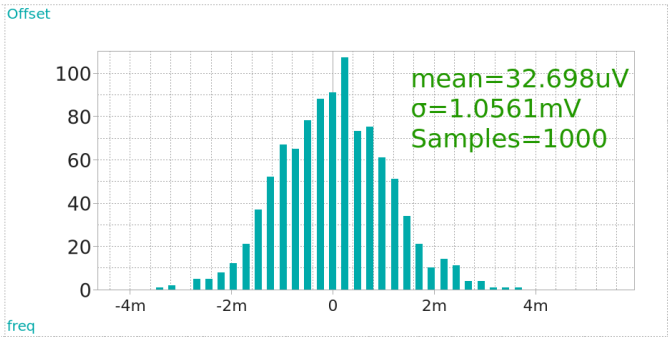


Fig. 4: Monte Carlo simulation (1000 runs) for input offset voltage.

V. Layout and Post-Layout Verification

A. Layout Implementation

The physical layout was created using KLayout, adhering to the SKY130 design rules. Key considerations were focused on analog matching and robustness. To achieve this, the input differential pair MOSFETs were implemented using a **common-centroid** layout. This technique minimizes mismatch caused by local process gradients. Similarly, critical current mirrors—both the PMOS active load for the differential pair and the NMOS mirrors for biasing—were grouped and placed symmetrically. Furthermore, **dummy devices** were added to the boundaries of all three matched sections (the input pair, PMOS mirror, and NMOS mirror). This is crucial for mitigating layout-dependent effects (LDEs), such as the **Well Proximity Effect (WPE)** and STI stress, ensuring that all critical transistors experience a uniform local environment.

The final layout, shown in Fig. 5, occupies an area of 87 µm × 33 µm, which is within the 140 µm × 80 µm constraint.

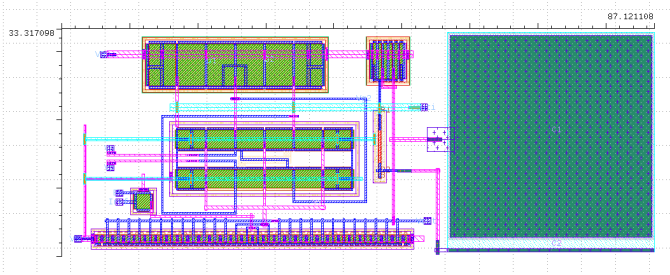


Fig. 5: Final op-amp layout in KLayout.

B. Post-Layout Simulation

The layout passed both Design Rule Check (DRC) checks in KLayout and LVS in Netgen. Parasitics were then extracted using Magic, and a post-layout simulation was performed. Table III compares the nominal pre-layout and post-layout performance, showing the impact of layout parasitics.

TABLE III: Pre-Layout vs. Post-Layout Simulation (Nominal)

Parameter	**Pre-Layout (TT)**	**Post-Layout (TT)**
DC Gain A_{DC} (dB)	*76.2*	*76.0*
GBW (MHz)	*3.78*	*3.64*
Phase Margin (PM) (°)	*81.1*	*81.5*
Gain Margin (GM)(dB)	*28.0*	*29.9*
Quiescent Current (I_Q) (µA)	*64.5*	*64.85*
Slew Rate (SR) ($\mathrm{V\,\mu s^{-1}}$)	*1.75*	*1.68*

C. Test Circuit and Post-Layout Verification

To verify the post-layout functionality and robustness of the op-amp, a dedicated test circuit was created. The op-amp was configured as a **voltage follower** (unity-gain buffer), which is a common test setup for stability and signal tracking. Post-layout simulations were performed across a temperature range of 20 °C to 50 °C and a VDD supply range of 1.7 V to 1.9 V. A 0.4 Vpp sinusoidal input signal was applied to test the circuit's transient response. The testbench setup and supporting graphs (shown in Fig. 6) verify the expected performance and stability across these operating corners.

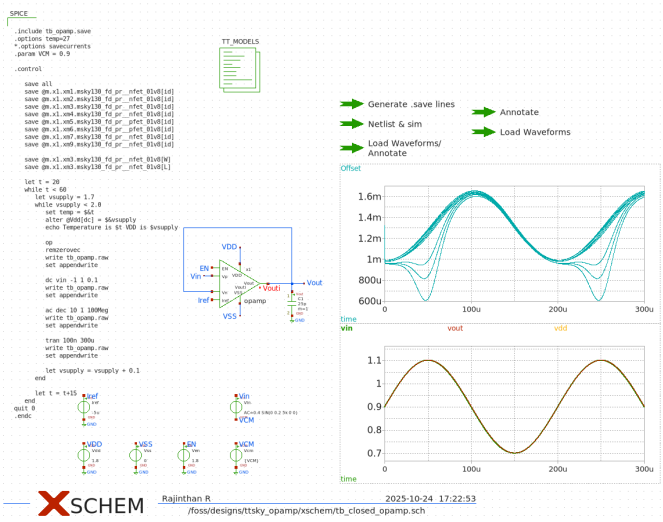


Fig. 6: Post-layout verification testbench (voltage follower) in Xschem.

VI. Summary of Results and Conclusion

This project detailed the design of a low-power op-amp in SKY130. The final post-layout design performance is summarized in Table IV, comparing the achieved parameters against the project specifications.

TABLE IV: Final Performance Summary vs. Specifications

Parameter	**Specification**	**Achieved (Min)**	**Typ**	**Max**
DC Gain A_{DC}	$> 60\,\mathrm{dB}$	*70.81*	*76.0*	*78.8*
GBW	$\geq 1\,\mathrm{MHz}$	*3.61*	*3.99*	*4.10*
Phase Margin	$> 60°$	*81.1*	*81.58*	*81.58*
Quiescent Current	$< 100\,\mu\mathrm{A}$	*60.00*	*64.85*	*68.1*
Slew Rate	$> 1\,\mathrm{V\,\mu s^{-1}}$	*1.61*	*1.77*	*1.721*
Input Offset (3σ)	$< 3\,\mathrm{mV}$	*2.97*	*3.16*	*3.21*
Disable Current	$< 2\,\mathrm{nA}$	*0.063*	*0.090*	*0.115*
Layout Area	$< 140\,\mu\mathrm{m} \times 80\,\mu\mathrm{m}$	$87\,\mu\mathrm{m} \times 33\,\mu\mathrm{m}$		

A. Conclusion

The design of a low-power, single-ended operational amplifier in the SKY130 130 nm technology was successfully completed. The final post-layout simulation results, summarized in Table IV, confirm that the design meets or exceeds the vast majority of the target specifications.

Specifically, the op-amp achieves a minimum DC gain of 70.81 dB (spec: $>$ 60 dB), a minimum gain-bandwidth product of 3.61 MHz (spec: $\geq$ 1 MHz), and a robust minimum phase margin of 81.1° (spec: $> 60°$), ensuring stability under the 25 pF load.

Furthermore, all power and area constraints were comfortably met. The maximum quiescent current across all corners was 68.1 µA (spec: $<$ 100 µA), and the disable-mode current was 0.115 nA (spec: $<$ 2 nA). The final layout area of $87\,\mu\mathrm{m} \times 33\,\mu\mathrm{m}$ is well within the required $140\,\mu\mathrm{m} \times 80\,\mu\mathrm{m}$ boundary.

The one specification that was marginally missed was the 3σ input offset voltage, which was 3.16 mV (spec: $<$ 3 mV). This is a known trade-off against the compact area and the sizing choices made for the differential pair. This could be improved in a future revision by using larger devices or more advanced layout matching techniques (e.g., common-centroid) for the input pair, at the expense of a larger layout area.

In conclusion, the project successfully demonstrates a complete design flow using open-source tools (Xschem, Ngspice, KLayout) to produce a functional and robust analog IC that meets a challenging set of performance goals.

References

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