An 87.25 dB Open-Loop Gain, 2.09 GHz Unity Gain Bandwidth 3-Stage Operational Amplifier Implemented Using 45nm Technology

***Abstract*— An operational amplifier (op amp) is a type of analogue circuit that takes a differential voltage input and outputs a single-ended voltage. Using the Cadence design environment, this paper represents a detailed design and analysis of a three-stage operational amplifier (op-amp). The proposed design has been implemented using 45 nm CMOS technology in cadence virtuoso environment with a power rail of ±0.9 V. The suggested op-amp architecture employs three independent stages namely, differential amplifying stage, OTS stage and gain boosting stage or buffer stage to provide staggering gain, excellent bandwidth, and remarkable stability while consuming little power. The total power dissipation is 21.85 mW for the gain of 87.25 dB. The simulation also showed the phase margin of 60.57 degree with a unity gain Bandwidth of 2.09 GHz which reflects that our op-amp has excellent stability over the frequency spectrum. The layout of the proposed op-amp is 3832.452 µm^2 which has cleaned DRC and LVS. The DC analysis was done maintaining 5.11374 nm current, the slew rate resulted in 0.2079 V/µs in respect to the proposed design. In this paper simulation such as PSRR and CMRR have also been performed with proper validation.**

Keywords—Op-amp, 3-stage op amp, CMOS technology, Cadence, DC analysis, Transient analysis, noise analysis, stability analysis.

I. Introduction

An op-amp is a high-gain amplifier used in electronics to magnify and manipulate analog signals. It has two input terminals for differential input and can be configured in various ways to perform tasks like amplification, filtering, and signal processing. For the design of the 3-stage op-amp CMOS technology was used. Complementary Metal-Oxide-Semiconductor (CMOS) operational amplifiers are key components in the construction of modern analog integrated circuits.

The work focuses on the design of a 3-state op-amp using the Cadence design environment. The architecture of the op-amp is precisely designed to create a balance between gain, bandwidth, and stability, while the complete analysis covers transient, DC, noise, and stability studies to assure optimal performance in a variety of settings. The three-stage op-amp configuration capitalizes on the unique characteristics of each stage to collectively achieve exceptional amplification and response characteristics. The initial stage employs a differential pair with an active load, emphasizing voltage gain and linearity. The second stage utilizes an arrangement to enhance the gain while maintaining stability. Finally, the third stage is responsible for driving the output load while maintaining a low output impedance. These stages are designed to harness the capabilities of advanced CMOS process technology, ensuring efficiency in both layout and integration.

An extensive examination of the operational amplifier design process is provided in this study. The work is organized into several sections, each contributing to a comprehensive study of the constructed operational amplifier. Section II. explores the literature review, offering a conceptual framework for the next phases. Subsequently, section III. portion clarifies the theory behind the design process. Section IV. provides a clear explanation of the operational amplifier's operational concept, specifically focusing on its three-stage structure that is meticulously designed to provide high gain, wide bandwidth, and stability while minimizing power consumption. Section V. concentrates on simulation and outcomes, using the Cadence design environment to examine transient behavior, steady-state circumstances, noise influence, and overall stability as well as a comparative analysis with the existing works. Ultimately, the last section of the article provides a comprehensive overview that emphasizes significant discoveries and advancements in the realm of op-amp design.

II. Literature Review

Modern electronic circuits rely heavily on operational amplifiers for their amplification and signal processing capabilities. A thorough resource for learning about microelectronic design is Rashid, M.H. (2011) Microelectronic circuits: Analysis and design [1]. According to Razavi, B. (2017) "Design Of Analogue Cmos Integrated Circuits," MOS devices in saturation mode may accurately simulate current sources that offer high resistance with negligible voltage loss [2]. Similar issues were encountered with the paper's recommended op-amp. The current mirror is often used in the amplifier stages to generate active loads and bias currents [3]. A current mirror can be employed in the differential pair in place of a current source. Konarkkumar D. Patel and Sophy P. Augusta Sample and Hold Design for Fast Analogue to Digital Conversion According to Beulet (2018), a completely differential folded cascade architecture yields a phase margin of 50°, a gain of over 55 dB, and a unity gain bandwidth of 500 MHz [4]. In their work "Implementation of a CMOS Operational Amplifier using Composite Cascade Stages," K. Sai Kumar and K. Lokesh Krishna constructed an op-amp that uses cascade stage amplifiers to achieve a 420MHz UGB (unity gain bandwidth) at 0.2pF and a DC voltage gain of 68.6dB. According to calculations, the occupied area is 0.032mm2, the slew rate is 72.8V/µs, the power dissipation is 114µW, and the CMRR is around 102.6dB [5]. In the section titled "Design and Implementation of Optimised Parameter Based Operational Amplifier for High-Speed Analogue Signal Processing," the authors state that validation was done using Monte-Carlo and Corner analysis, and that the desired results of 60 dB gain, 58.7 degree phase margin, and 302.55 microwatts of power dissipation were also attained [6]. According to Dipesh Panchal and Amisha Naik, with a gain of 61dB, the total power dissipation is 15.77nW [7]. The op-amp has a unity gain bandwidth of 228MHz at 0.5pF and a DC gain of 66.4dB, according to A. Jeevan Kumar and K. Lokesh Krishna's article [8]. In their article, Kavyashree C L, M. Hemambika said that they used 90nm technology and produced a gain of 84db with a phase margin of 560 and a

power dissipation of 38.02µW [9]. Ashutosh Pranav and Deepak Prasad reported that their slew rate was around 29.9 V/µs and their DC gain was approximately 56.94 dB in their article, "Design of 30 MHz CMOS Operational Amplifier" [10].

III. Theory

The operational amplifier, also known as an op-amp, is a high-gain, direct-coupled amplifier made up of three stages: an output stage that produces a low output resistance, a middle stage that produces a high voltage gain, and an input stage that produces a high input resistance with a specific amount of voltage gain. The amplifier functions by means of a differential voltage between its two input terminals and is a prefabricated, integrated circuit [1].

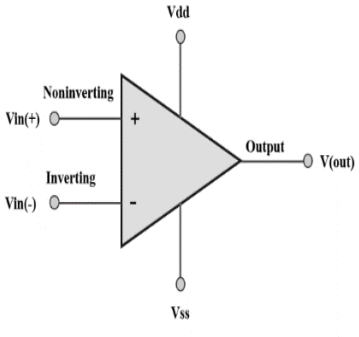


Fig. 1. Operational Amplifier.

In Figure 1. The inverting op-amp is a device that applies a signal to its inverting input while connecting its non-inverting input to ground. The inverting op-amp's voltage gain is -

$$\text{Voltage Gain (Av)} = \frac{\text{Vout}}{\text{Vin}} = -\frac{R2}{R1}$$

Conversely, the resultant circuit is referred to as a Non-Inverting Op-Amp when the signal is supplied at the non-inverting input. For a non-inverting op-amp, the voltage gain is –

$$\text{Voltage Gain (Av)} = \frac{\text{Vout}}{\text{Vin}} = 1 + \frac{R2}{R1}$$

The proposed op-amp is designed using CMOS technology. The low cost of fabrication and the ability to combine analog and digital circuitry on the same chip to improve overall performance and/or minimize packing costs make CMOS technology appealing [2].

A. Differential Pair

The most common building component in analogue integrated circuit design is the differential pair; a differential amplifier is what an op-amp's input stage is [11]. Two transistors make up the differential pair; they are usually one n-type and one p-type metal-oxide-semiconductor (NMOS and PMOS, respectively).

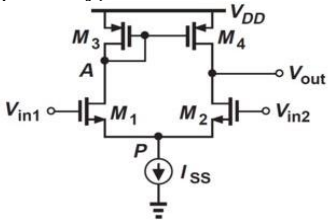


Fig. 2. Basic differential pair.

These transistors are wired in a parallel fashion, with the two input signals—typically denoted as Vin+ and Vin−—driving the transistors' gates. Gain is applied to the difference between two input signals via differential amplifiers.

B. Current Mirror

A current mirror is a circuit block that replicates the current in an output terminal to create a duplicate of the current flowing into or out of an input terminal. Because of its comparatively high output resistance, the current mirror helps maintain a consistent output current under all load conditions. Two NMOS linked to the gate and a reference resistor—where another NMOS can be utilized since NMOS has resistive qualities—make up the current mirror.

C. Miller Capacitor

The Miller capacitor is a capacitance that, although being created by the amplifier's gain and the intrinsic capacitance between the input and output nodes, seems to be linked across the amplifier's input and output terminals. The feedback loop of the amplifier experiences a frequency-dependent phase shift due to the Miller capacitor, which affects the amplifier's stability and bandwidth.

D. Operational Transconductance Amplifying Stage

The OTA stage receives input from the differential input stage's output. We employ a compensating. capacitor between the two stages—that is, from the output of the first stage to the output of the second stage to achieve this. We maintain a resistor in series with the capacitor to overcome this [12]. The OTA stage helps with the current flow.

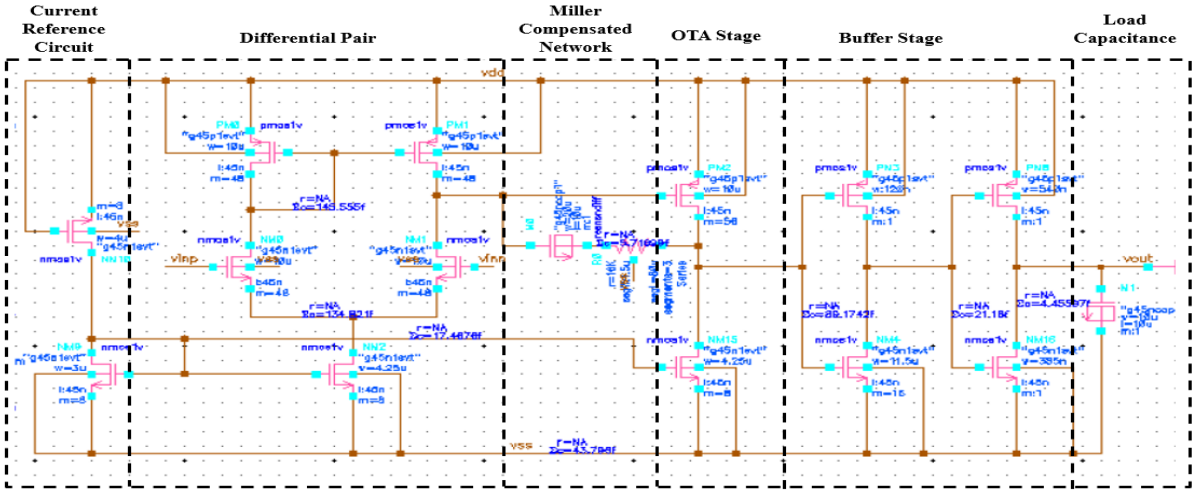


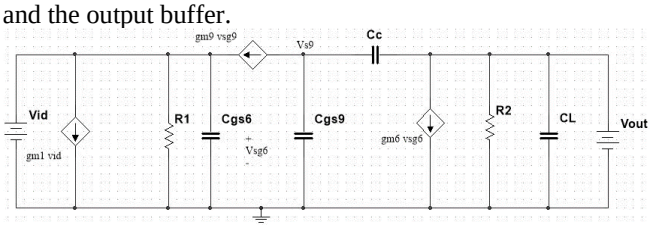
Fig. 3. Proposed 3-Stage Op-amp.

E. *Buffer Stage*

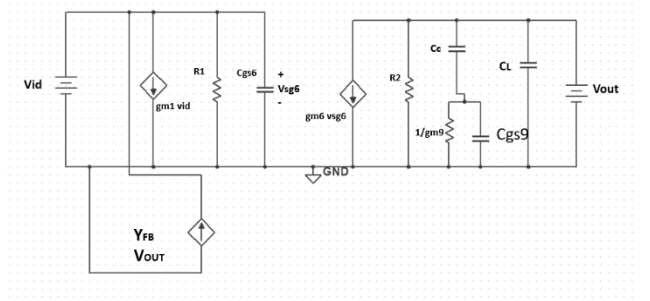
The last stage, often known as the output buffer, oversees driving the output load while keeping the output impedance low. buffer is formed by cascading two CMOS inverters back-to-back. The operation of one CMOS inverter is to invert the input signal to the opposite logic level. Thus, a cascaded combination of two such circuits will bring back the input signal to the original level.

IV. Methodology

The small-signal model of a three-stage op-amp represents the amplifier's behavior for small input variations. It encompasses input differential pairs, intermediate gain stages, and the output buffer.



(a)



(b)

Fig. 4. (a) Small-signal equivalent circuit of the op-amp in (b) equivalent circuit of (a) in a classical shunt-shunt feedback configuration.

The transfer function from Fig. 4(b) may be examined using feedback theory in the manner shown below. Using ZOL(s) as the open loop trans-impedance function and YFB (s) as the transfer feedback factor, as shown in Fig. 4(b), we obtain:

$$A(s) = g_{m1}\frac{Z_{OL}(s)}{1+Z_{OL}(s).Y_{FB}(s)} = \frac{g_{m1}}{Y_{OL}(s)+Y_{FB}(s)} \quad (1)$$

Where under normal condition, $C_{gs8} \ll C_L$ *and* $R_2 \gg {}^{1}/_{g_{m8}}$

$$Y_{OL}(s) = \frac{(1+sR_1C_{gs6})\{s^2R_2C_L(C_c+C_{gs9})+s[R_2g_{m9}(C_L+C_c)]+g_{m9}\}}{g_{m6}R_1R_2\{g_{m9}+s(C_c+C_{gs9})\}} \quad (2)$$

$$Y_{FB}(s) = \frac{sC_C\,g_{m9}}{g_{m8}+s(C_C+C_{gs9})} \quad (3)$$

According to (1), we found that the dc gain of the op-amp is given by,

$$A_O = g_{m1}g_{m6}R_1R_2 \quad (4)$$

The frequency of the op-amp dominating pole may be determined by,

$$\omega_{p1} \cong \frac{1}{g_{m6}R_1R_2\,C_C} \quad (5)$$

By combining [(1)-(5)],

$$A(s) \cong \frac{\omega_u}{s} \times \frac{1+s\frac{C_C+C_{gs9}}{g_{m9}}}{s^2\left(\frac{C_L.C_{gs6}}{C_Cg_{m6}}\times\frac{C_C+C_{gs9}}{g_{m9}}\right)+s\left(\frac{C_L.C_{gs6}}{C_Cg_{m6}}\times\frac{C_C+C_{gs6}}{g_{m6}}\right)+1} \quad (6)$$

Where,

$$\omega_u \cong A_O.\,\omega_{p1} = \frac{g_{m1}}{C_C} \quad (7)$$

Another term for this number is the gain-bandwidth product, or the unity-gain frequency of the op-amp.

Upon reviewing (6), we discovered that,

$$\frac{g_{m9}}{C_C+C_{gs9}} = \frac{g_{m6}}{C_{gm6}} \quad (8)$$

$$B(s) = s^2\left(\frac{C_LC_{gs6}}{C_C\,g_{m6}} \times \frac{C_C+C_{gs9}}{C_C\,g_{m6}}\right)+s\left(\frac{C_LC_{gs6}}{C_C\,g_{m6}} + \frac{C_{gs9}}{g_{m6}}\right)+1 \quad (9)$$

The non dominant poles of A(s), i.e., the roots of the polynomial are given by.

$$P_2 = -\frac{g_{m6}\,C_C}{C_{gm6}\,C_L} \quad (10)$$

$$P_3 = -\frac{g_{m9}}{C_{gS6}} \quad (11)$$

It can be observed that P_3 cancels the finite zero of the transfer function.

$$Z = -\frac{g_{m9}}{C_C+C_{gs9}} \quad (12)$$

Exactly and A(s) can therefore be reduced to.

$$A(s) \cong \frac{\omega_u}{s} \times \frac{1}{1-\frac{s}{p_2}} \quad (13)$$

As per equation (13), the op-amp's phase margin, when evaluated at 100% feedback, is observable. ΦM=180 - −A(jωu).

$$\phi_M = tan^{-1}\frac{|p_2|}{\omega_u} = tan^{-1}\frac{\omega T_6 C_C}{\omega_u C_L} \quad (14)$$

It might be applied in the trade-off between the compensating circuit's area and power usage.

V. Simulation and Results

To verify the proposed op-amp several analyses were conducted to do further comparative analysis.

A. *DC Analysis*

By simulating the op-amp circuit under DC conditions, for about 5 mA the whole system was optimized through DC operating point to ensure that every MOSFET is in saturation condition.

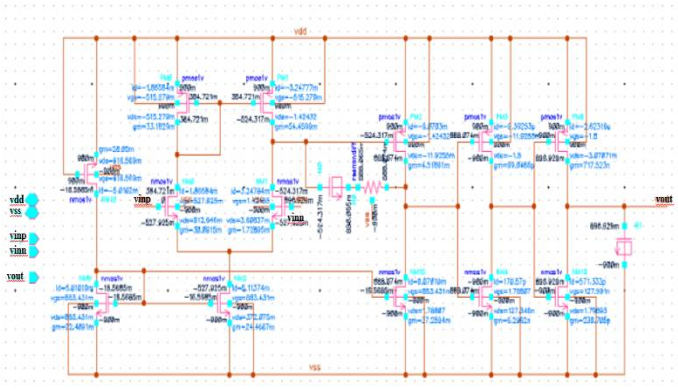


Fig. 5. DC operating Points.

B. *AC Analysis*

From the AC analysis in Fig. 6, the AC phase and gain plot were obtained. From the plot it is visible that the 0 dB crossing point is before the -180° crossing point resulting in a positive phase margin. Which means that the circuit is stable. For op-amp the phase margin should be 40-65°.

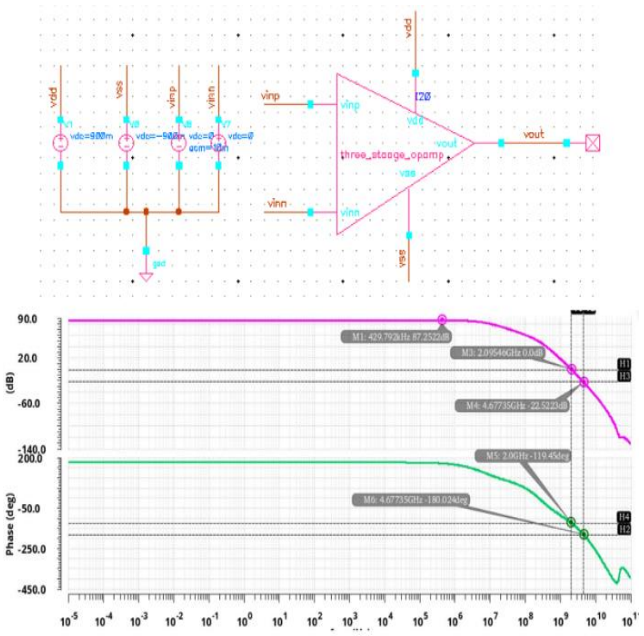


Fig. 6. AC gain and phase

The system's phase margin is computed as 60.574 °, suggesting high stability. It is discovered that the gain margin is 22.5223 dB, and the op-amp has a suitable gain of up to 87.2522 dB. Furthermore, up to 2.09 GHz, the system responds steadily; beyond that, it becomes unstable. The system appears to have a good phase margin, gain margin, and frequency responsiveness overall, according to the research, however outside of the stated range, 2.09 GHz should be used with caution because of possible instability.

C. *Transient Analysis*

The transient analysis of a three-stage op amp with Vin+ and Vin- varying from -0.9 V to 0.9 V during a 20 ns period and 10ns period, respectively, exhibits dynamic behavior. The output of the op amp in Fig. 7. fluctuates in response to changes in the input, showing amplification and phase shifts.

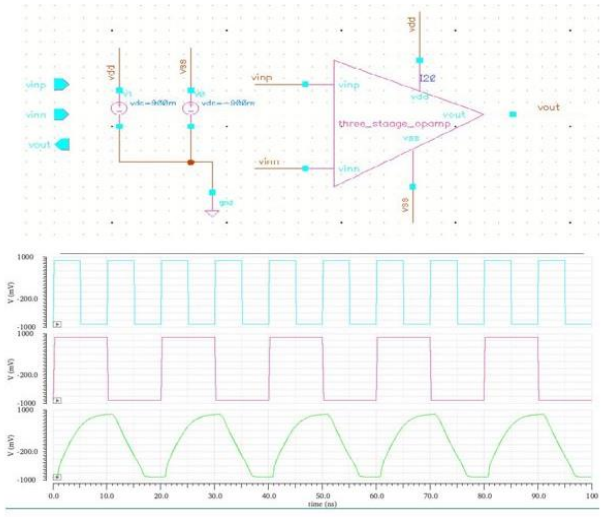


Fig. 7. Transient analysis.

D. *Slew Rate*

The operational amplifier's or a circuit of a similar type's slew rate indicates how fast the output voltage may alter in reaction to a sudden change in the input signal.

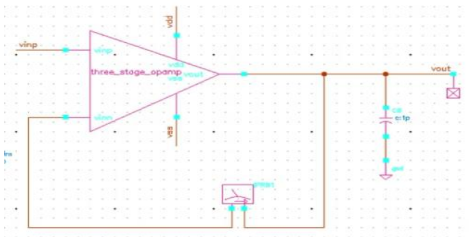


Fig. 8. Slew rate

The suggested op-amp's slew rate was ascertained using the testbench shown in Figure 8. The slew rate for the vout signal was calculated using the values that were chosen from the Cadence Virtuoso calculator tool. The resultant slew rate was 0.2079 V/µs.

E. *Noise Analysis*

Noise analysis assesses the undesired electrical disruptions that occur in electronic circuits and have the potential to compromise signal integrity and overall system performance.

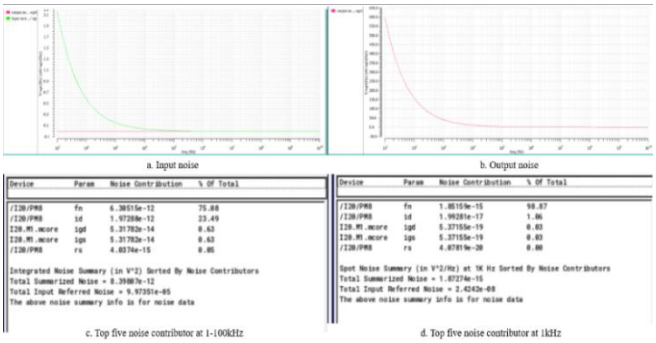


Fig. 9. Noise analysis.

After following the steps for noise analysis, the input and output plot from Fig. 9. was obtained. From the figure it is visible that the top noise contributor for both 1kHz and 1-100kHz frequency is the PM8 PMOS. From the spot noise and integrated noise summary it is also visible that the PM8 or the PMOS8 is responsible for most of the noise contribution.

F. *S-parameter Analysis*

High-frequency RF and microwave circuit design may be effectively accomplished with the use of S-parameter analysis. Both low-frequency and high-frequency networks can benefit from the use of S-parameter analysis. On the other hand, additional characteristics like admittance or impedance may be used to depict low-frequency networks with ease [13].

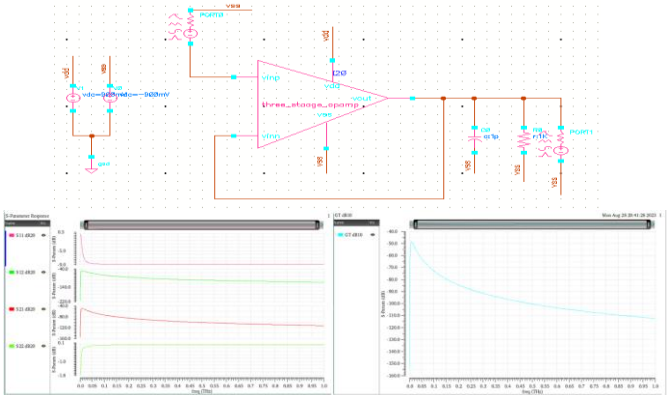


Fig. 10. S-parameter analysis.

The s-parameter analysis for the proposed circuit was done using the circuit provided in Fig. 10. Where the graphical representation is also visible.

G. PSRR (Power Supply Rejection Ratio)

The ratio of the input offset voltage change to the power supply voltage change is known as the PSRR. DC Variation is the standard that is applied in the datasheet. Power Supply Variation (PSRR) = 20 log (Input Offset Voltage Variation) [dB]. In general, PSRR is frequency dependent, declining with increasing frequency [14].

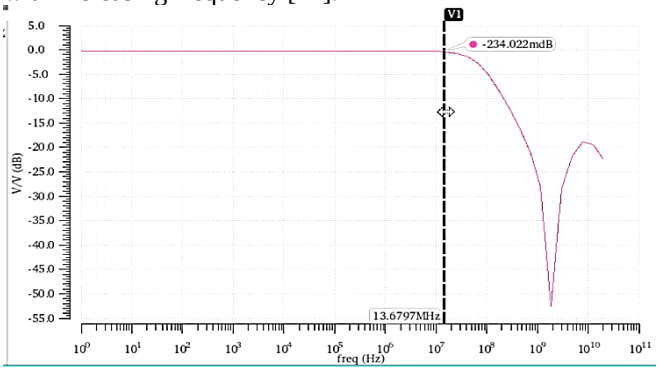


Fig. 11. PSRR analysis.

The PSRR analysis was conducted for the proposed circuit and the power supply rejection ratio was determined, which can be observed in Fig. 11.

H. CMRR (Common-Mode Rejection Ratio)

CMRR is a measure of an electronic circuit's ability to reject common-mode signals, which are disturbances that appear simultaneously on both input terminals of the circuit. It quantifies how well the circuit responds to differential signals compared to common-mode signals. The value of the CMRR frequently depends on the signal frequency and the function should be specified [15].

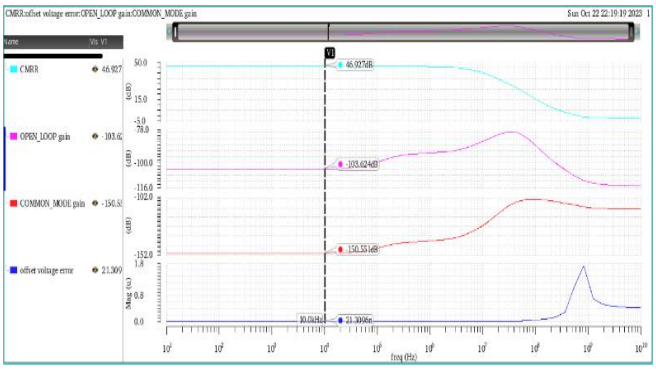


Fig. 12. Common-mode rejection ratio.

From Fig. 12. It is clearly visible how the proposed circuit responds to open loop gain, common mode gain, and offset voltage error.

I. Stability Analysis

Stability analysis evaluates the reliability of an electronic circuit's behavior across different conditions, ensuring it remains predictable and consistent. This analysis is essential for designing circuits with consistent performance, particularly in critical applications like control systems or communication circuits.

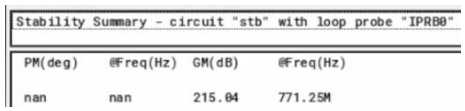


Fig. 13. Stability analysis.

The stability analysis was done using ADE L using the same test bench from Fig. 8. After doing the stability analysis of the proposed circuit the stability summary was obtained which is shown in Fig. 13.

J. Power Consumption

Power consumption assesses the energy usage of electronic circuits, crucial for optimizing efficiency in battery-powered devices. The power consumption was measured of the proposed op-amp using the test bench in Fig. 8. The power consumption resulted in 21.854mW.

K. Layout

The physical layout of 3-stage op-amp can be observed in Fig. 14. From where we can determine that the total area of the 3-stage op-amp is 3832.452 μm^2. The height of the op-amp is 36.845 µm and the width is 104.015 µm. The LVS, ERC, DRC of the proposed design were also cleaned.

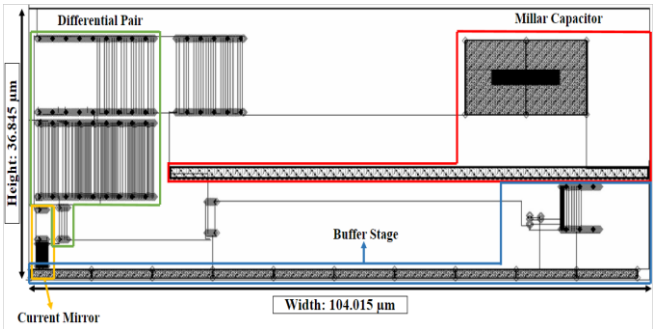


Fig. 14. Layout of the proposed design.

VI. Result Analysis

Compared to previous studies [4–10], our study offers a detailed examination across a variety of factors, indicating a deeper comprehension of the system's functionality. In particular, our analysis covers a broad spectrum of technology, from 180nm to 45nm, and includes both mature and cutting-edge nodes. In contrast to several other studies that did not include supply voltage information [4], we carefully examine the effects of different supply voltages, ranging from 1.5V to ±0.9V. We find that our analysis of gain indicates a significant improvement, coming in at 87.25 dB, above the values published in [4, 5, 6, 7, 8, 9]. In addition, our Unity Gain Bandwidth is 2.09 GHz, which is notable for spanning a wider spectrum and shows better frequency responsiveness than [4, 5, 6, 8]. The breadth of our analysis is further enhanced by slew rate and settling time assessments, which cover a variety of technologies and are lacking in certain referred papers [4, 5, 6, 7]. Furthermore, power consumption is carefully considered in our research as well; values range from 0.038 mW to 21.854 mW, providing a more comprehensive understanding of efficiency than in [4, 5, 6]. Finally, our thorough examination of output voltage swing, encompassing a range of ±0.306 mV, sets our study apart. To sum up, our study is distinct since it offers a more thorough and comprehensive examination of several aspects, which makes it a more substantial addition to the area.

TABLE I. PERFORMANCE PARAMETERS COMPARISON BETWEEN PROPOSED 3- STAGE OPAMP WITH OTHER WORKS

Parameters	[4]	[5]	[6]	[7]	[8]	[9]	[10]	This Work
Technology (nm)	180	130	180	180	90	90	45	45
Supply voltage (V)	-	1.5	1.8	0.3	1.5	1	2	±0.9
Gain (dB)	57.87	68.6	60	61	66.4	84	56.94	87.25
Unity Gain Bandwidth (GHz)	0.63	0.42	0.03	-	0.228	0.005	0.03	2.09
Slew rate (V/µsec)	299.3	72.8	20	58.7	248.2	5	29.9	0.2079
Phase Margin (deg)	60	-	58.7	51.8	277.4	56	65.64	60.574
Settling time (ns)	0.75	-	-	-	-	-	-	7.69
Power Consumption (mW)	-	0.114	0.302	0.000015	74	0.038	1.667	21.854
Output Voltage Swing (mV)	-	-	-	-	-	-	-	±0.306

VII. CONCLUSION

A general investigation has been taken upon the characteristics and performance of 3-stage operational amplifiers through different analyses including DC analysis, AC analysis, Noise analysis, Power consumption, S-Parameter analysis, determining the slew rate, CMRR, PSRR, stability analysis, power consumption and lastly creating a physical layout. Each analysis provided crucial insights for the proposed op-amp. Different specifications like phase margin, gain margin and response frequency for op-amp were discussed. It can be observed that the system will respond up to 2.09GHz. And after that the system will be unstable. The S-parameter study offered information on its interaction with surrounding components, the noise analysis emphasized the value of noise management, the AC analysis highlighted its dynamic behavior, and the plotted graph were used for power consumption from that the power consumption was obtained 21.854mW. The DC analysis clarified its stable operating point. The analyzing techniques helps to understand the operational amplifiers functionality. The comparative analysis reflects the results obtained from the proposed design. It also gives an idea of how this design is better from the rest and what area we should focus on to improve the design further.

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