Group# 08	
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CO2: Integrate different tools such as, LVS, DRS, and synthesized tools for the prediction and modeling of complex VLSI circuits for any specific needs
P.e.2.p4 (P1, P4, & P5): Project Report [20]

Category	Proficient [4-5]	Good [3-2]	Unacceptable [1-0]	Secured Marks
Knowledge of Technology (K6)	The students have acquired extensive knowledge of the commercial tools and concept to solve real-life problems in the domain.	The students have acquired moderate knowledge of the commercial tools and concept to solve real-life problems in the domain.	The students have acquired insufficient knowledge of the commercial tools and concept to solve real-life problems in the domain.	
Depth of Knowledge required (P1)	Use of tools for predicting and modeling the problems are based on advance circuit design knowledge and advance knowledge of commercial tools.	Use of tools for predicting and modeling the problems are based on moderate circuit design knowledge and moderate knowledge of commercial tools.	Use of tools for predicting and modeling the problems are based on limited/no circuit design knowledge and limited knowledge of commercial tools.	
Familiarity of Issues (P4)	Many unfamiliar issues on engineering tools and design parameters are addressed successfully.	Some unfamiliar issues on engineering tools and design parameters are addressed successfully.	No/one unfamiliar issue on engineering tools and design parameters is addressed successfully.	
Extent of Applicable Codes (P5)	The documentation has incorporated the problem solution with the standards and codes of practice for professional engineering.	Some standards and codes of practice for professional engineering has been identified and linked with the problem solution.	Inadequate or no standards and codes of practice for professional engineering has been identified and linked with the problem stated.	
Total Marks (Out of 20)				

Part-02:

Title: Designing the physical layout of 2-to-1 MUX and verifying the layout using DRC, ERC and LVS.

Introduction: A Multiplexer (MUX) is a fundamental digital circuit that selects one input from multiple sources and directs it to an output based on control signals. It's like a digital data switch, used in various applications to efficiently manage data routing and reduce circuit complexity. This report involves designing the physical layout of the 2-to-1 MUX that was developed in part-01. The layout will be verified using DRC, ERC and LVS.

Simulation and Results: Cadence environment was used to design the physical layout of the MUX. The MUX was designed in part-01. To design the layout the cell library was used, and the instances of the 2-to-1 MUX cells were placed in the layout. Metal interconnects were created to connect the cells according to the schematic, adhering to metal layer design rules. The metal routing was implemented with proper consideration for signal integrity and parasitic effects. Symmetry, alignment, and adequate spacing between components was ensured.

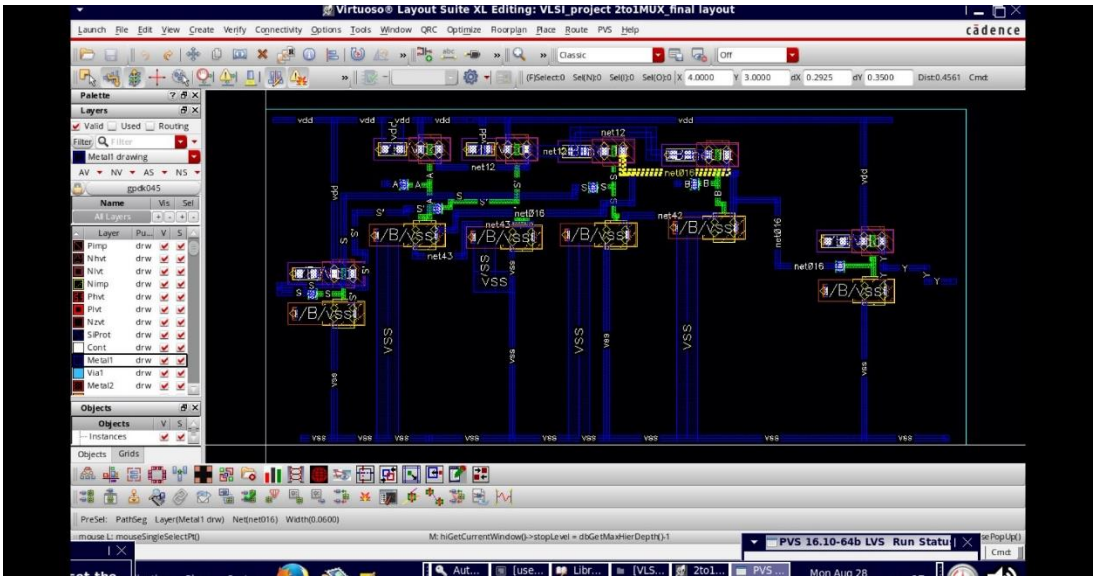

Fig.01: Physical layout of 2-to-1 MUX

The DRC process detects and flags any violations of the design rules, helping to identify and fix potential fabrication issues that could affect the performance and yield of the fabricated 2 to 1 MUX. After completion of the physical layout the Design Rule Checking (DRC) using layout verification tools was performed. DRC identifies violations such as incorrect spacing, width violations, overlap, and other geometric errors.

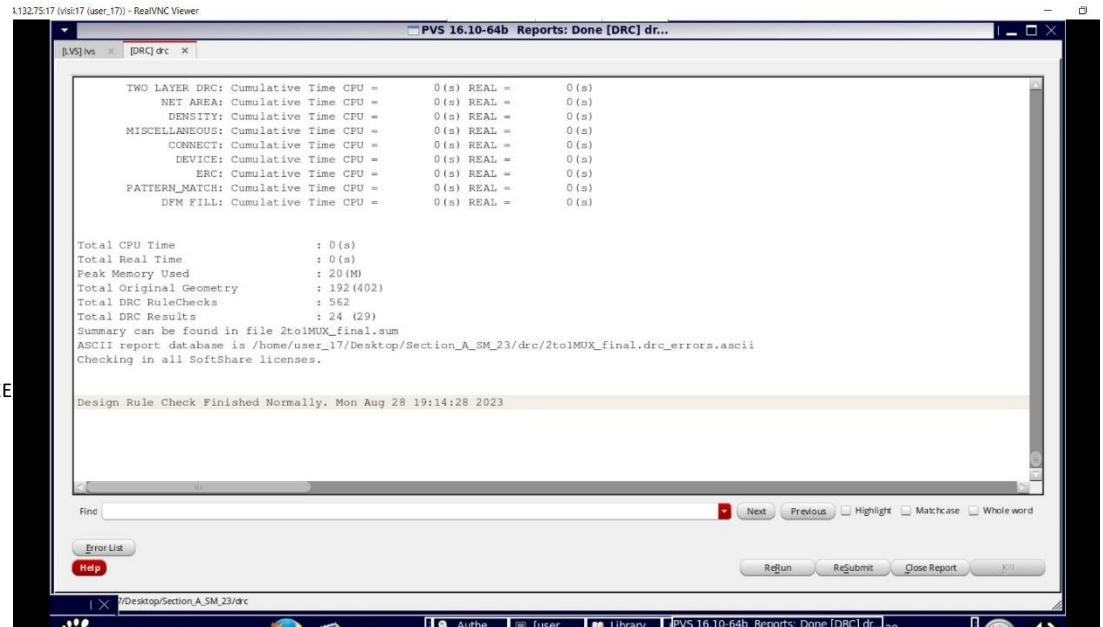

Fig.02: DRC of 2-to-1 MUX

ERC (Electrical Rule Check) is a process in Cadence that checks for violations of electrical design rules in a schematic or layout. Electrical Rule Checking (ERC) was executed then to verify that the layout adheres to electrical rules and guidelines. ERC checks for signal connectivity, proper isolation, and compliance with design specifications.

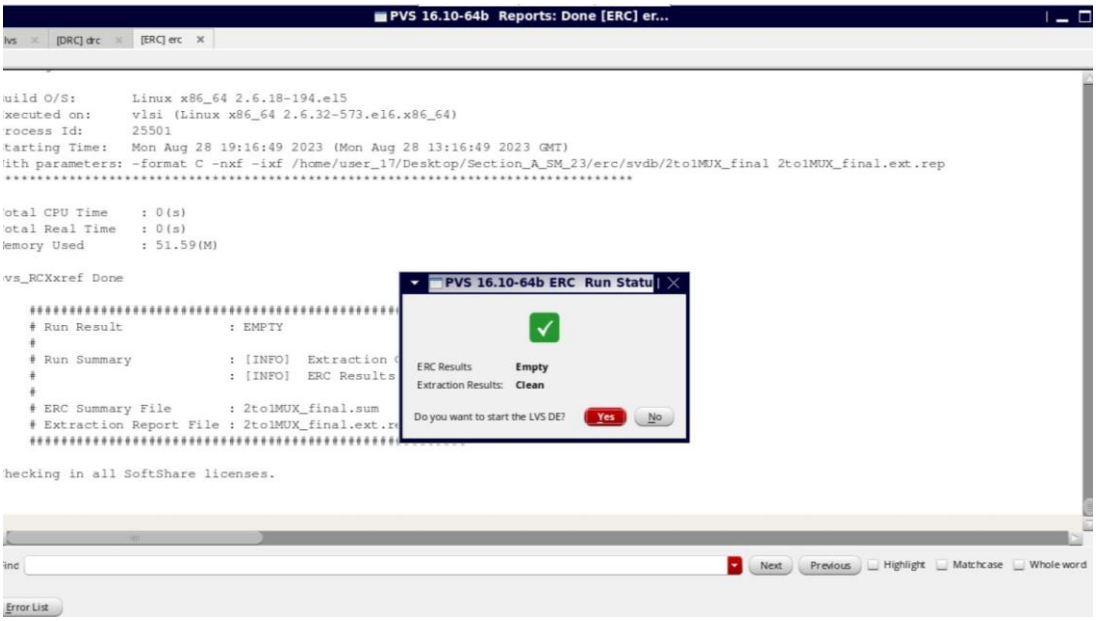

Fig.03: ERC of 2-to-1 MUX

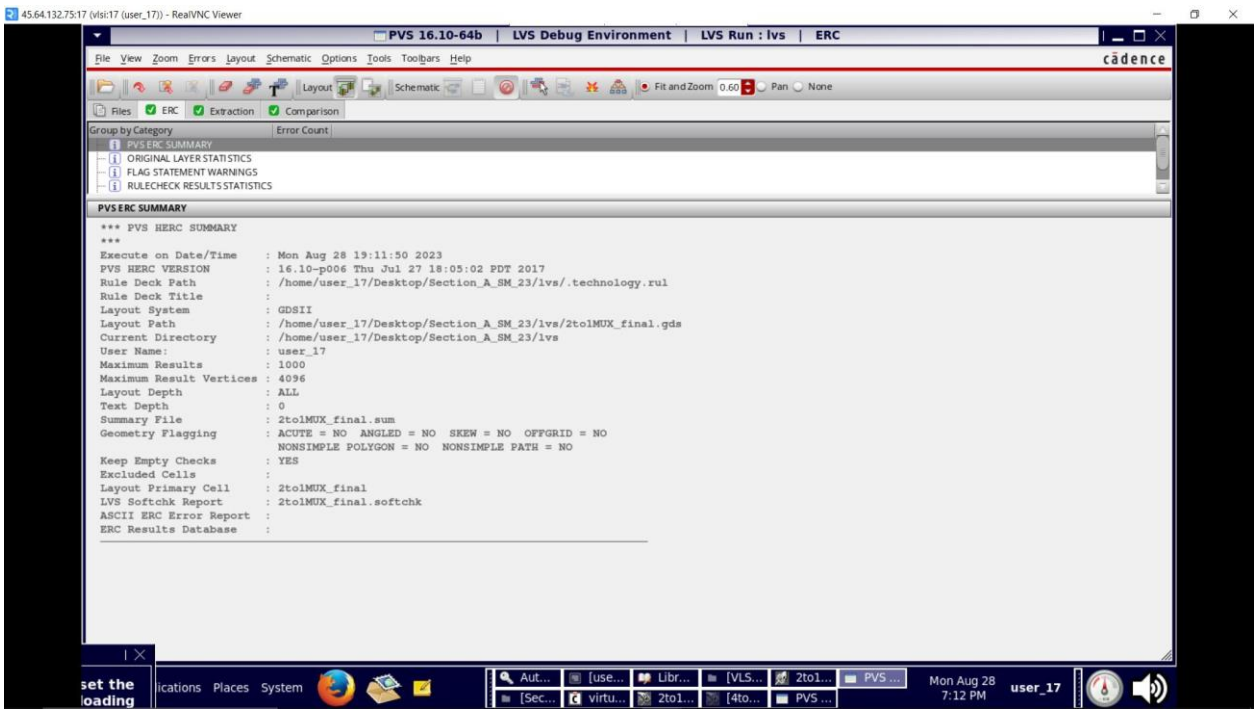

Fig.04: ERC summary of 2-to-1 MUX

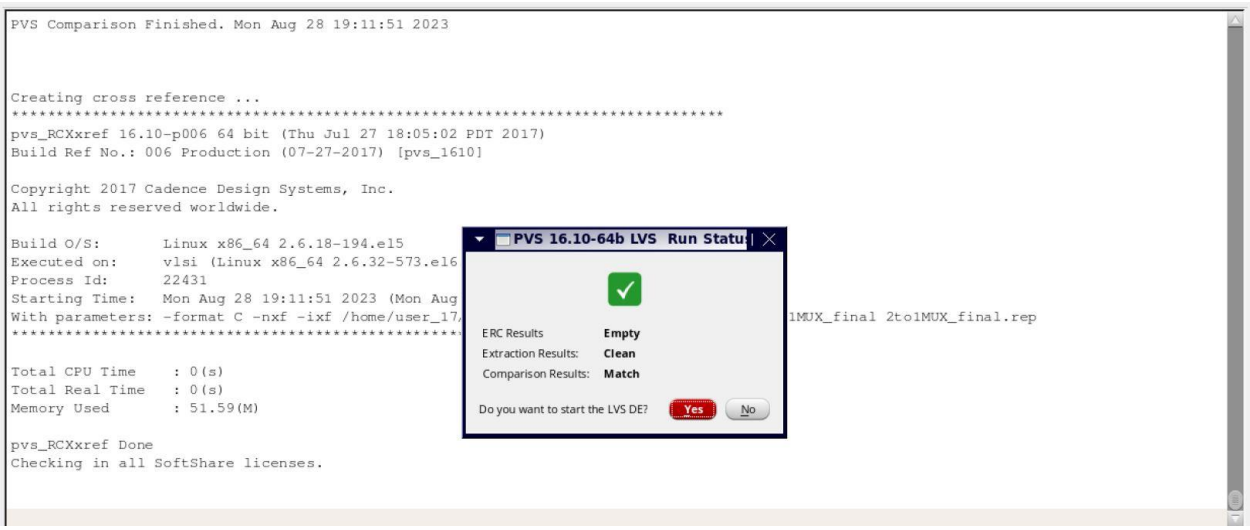

Fig.05: LVS of 2-to-1 MUX

Lastly, Layout vs. Schematic (LVS) comparison was performed to verify that the physical layout matches the intended schematic design. LVS compares netlists extracted from the layout with the original schematic netlist.

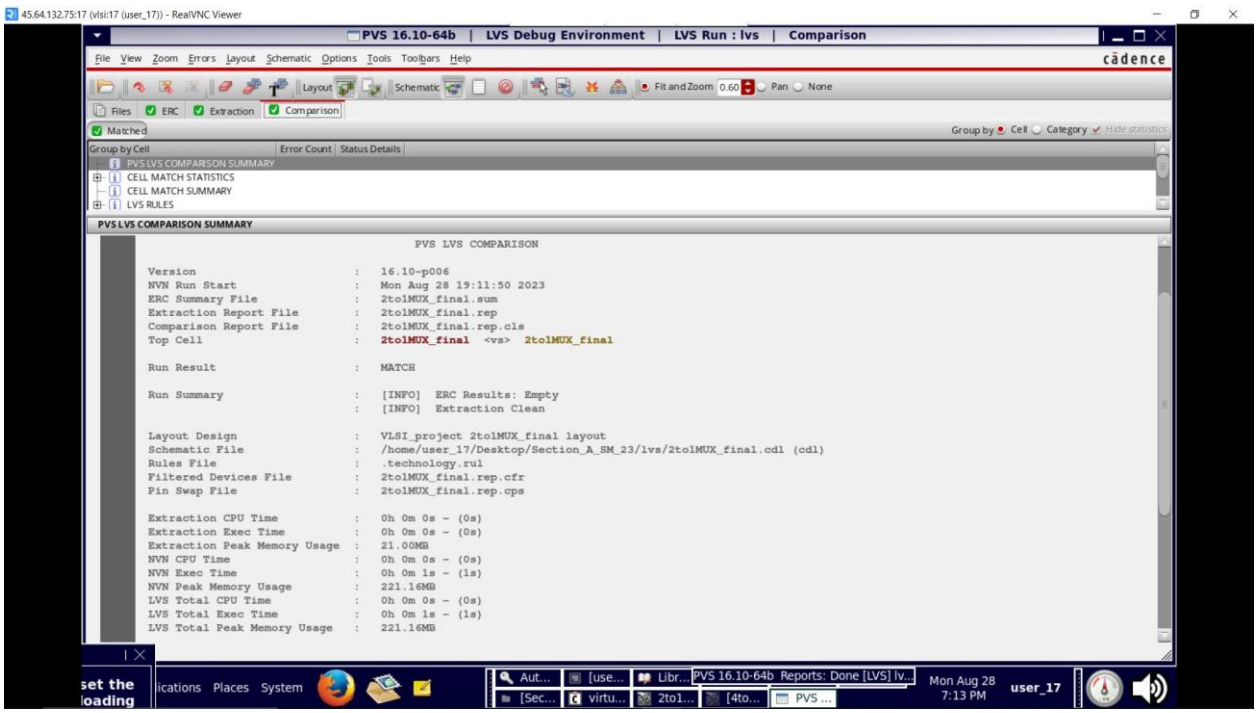

Fig.06: LVS summary of 2-to-1 MUX

Discussion and Conclusion: The process of designing the physical layout of a 2-to-1 multiplexer (MUX) and rigorously verifying its accuracy through Design Rule Checking (DRC), Electrical Rule Checking (ERC), and Layout vs. Schematic (LVS) comparison is a crucial foundation of semiconductor design. The application of DRC, ERC, and LVS verification steps significantly reduces the likelihood of errors, thereby increasing the chances of successful manufacturing and functionality. We successfully checked DRC, ERC and LVS for 2 to 1 MUX. ERC and LVS result successfully matches. So, we can say that the experiment was completed with moderate results.

Reference:

[1] Teja, R. (2023, March 13). *Multiplexer (MUX) and Multiplexing*. ElectronicsHub. https://www.electronicshub.org/multiplexerandmultiplexing/

[2] *Digital Circuits - Multiplexers*. (n.d.). Tutorialspoint. https://www.tutorialspoint.com/digital_circuits/digital_circuits_multiplexers.htm