Group# 08	
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CO2: Integrate different tools such as, LVS, DRS, and synthesized tools for the prediction and modeling of complex VLSI circuits for any specific needs
P.e.2.p4 (P1, P4, & P5): Project Report [20]

Category	Proficient [4-5]	Good [3-2]	Unacceptable [1-0]	Secured Marks
Knowledge of Technology (K6)	The students have acquired extensive knowledge of the commercial tools and concept to solve real-life problems in the domain.	The students have acquired moderate knowledge of the commercial tools and concept to solve real-life problems in the domain.	The students have acquired insufficient knowledge of the commercial tools and concept to solve real-life problems in the domain.	
Depth of Knowledge required (P1)	Use of tools for predicting and modeling the problems are based on advance circuit design knowledge and advance knowledge of commercial tools.	Use of tools for predicting and modeling the problems are based on moderate circuit design knowledge and moderate knowledge of commercial tools.	Use of tools for predicting and modeling the problems are based on limited/no circuit design knowledge and limited knowledge of commercial tools.	
Familiarity of Issues (P4)	Many unfamiliar issues on engineering tools and design parameters are addressed successfully.	Some unfamiliar issues on engineering tools and design parameters are addressed successfully.	No/one unfamiliar issue on engineering tools and design parameters is addressed successfully.	
Extent of Applicable Codes (P5)	The documentation has incorporated the problem solution with the standards and codes of practice for professional engineering.	Some standards and codes of practice for professional engineering has been identified and linked with the problem solution.	Inadequate or no standards and codes of practice for professional engineering has been identified and linked with the problem stated.	
Total Marks (Out of 20)				

Part-01:

Title: Designing a 1-bit 4-to-1 multiplexer from multiple 1-bit, 2-to-1 multiplexers.

Abstract: A Multiplexer (MUX) is a fundamental digital circuit that selects one input from multiple sources and directs it to an output based on control signals. It's like a digital data switch, used in various applications to efficiently manage data routing and reduce circuit complexity. This project involves the design of a 4-to-1 MUX. The design of 4-to-1 MUX is created from the simpler circuits 2-to-1 MUX using the cadence schematic tool then the results were validated by simulating the circuit for prediction and modeling of the circuit transient analysis, DRC and LVS in an industry-standard EDA tool such as Cadence Virtuoso was used.

Introduction: The pursuit of efficient and optimized solutions has encouraged the investigation of creative approaches in the field of digital circuit design. Multiplexers, which are fundamental components in digital systems, allow data to be routed selectively from several inputs to a single output based on control signals. This study delves into a novel method for building a 1-bit 4-to-1 multiplexer by cleverly linking numerous 1-bit 2-to-1 multiplexers. This project provides an approach for creating higher-order multiplexing functionality by using the inherent capabilities of these fundamental building pieces. This method not only demonstrates the versatility of employing simpler units to accomplish complicated processes, but it also reveals insights into optimizing digital circuitry for improved performance and resource efficiency. Several design stages are included in the project, including circuit optimization, simulation, layout design, and schematic design. The MUX's performance has been evaluated using several criteria transient analysis, DRC and LVS. The simulation results show that the created MUX meets the needed standards and is suitable for real-world applications.

Theory and Methodology: A 4-to-1 multiplexer (mux) is a digital logic circuit that allows the selection of one out of four input lines to be routed to a single output line. It is composed of four data inputs (A, B, C, and D), two control inputs (S0 and S1), and one output (Y). The control inputs S0 and S1 determine which input data line is propagated to the output. The combination of these control inputs defines the selection logic.

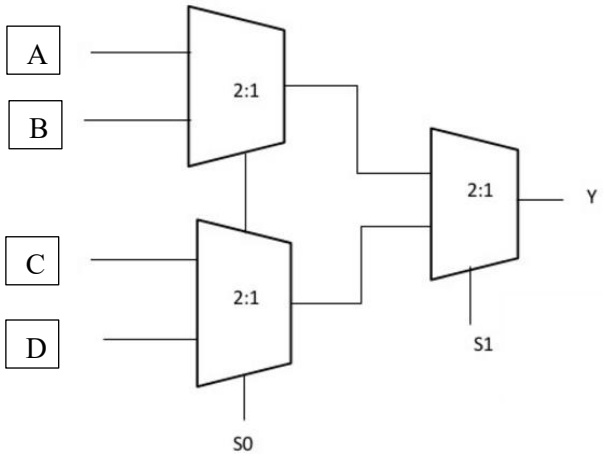

Fig.01: 4-to-1 MUX symbol

Down below is the truth table for the 4-to-1 MUX.

S_1	S_0	A	B	C	D	Y
0	0	0	x	x	x	0
0	0	1	x	x	x	1
0	1	x	0	x	x	0
0	1	x	1	x	x	1
1	0	x	x	0	x	0
1	0	x	x	1	x	1
1	1	x	x	X	0	0
1	1	x	x	x	1	1

The control inputs S0 and S1 determine which input data line is propagated to the output. The combination of these control inputs defines the selection logic. The general selection equation for a 4-to-1 multiplexer can be expressed as:

Y = S1' S0' A + S1' S0 B + S1 S0' C + S1 S0 D

Here:

Y represents the output.
S0 and S1 are the control inputs that select the desired input line.
A, B, C, and D are the data inputs that correspond to the four possible choices.
The logic equations demonstrate that each data input is associated with a specific combination of control inputs. Depending on the values of S1 and S0, one of the data inputs is selected and passed to the output. The other data inputs are effectively disconnected from the output.

For designing the 4-to-1 MUX at first the 2-to-1 MUX was built. For the circuit gpdk45 technology was used. To build the 2-to-1 MUX combinations of PMOS and NMOS was used. So, the CMOS technology was used to complete the designs. Down below is the schematic block for the 2-to-1 MUX implemented in cadence virtuoso environment.

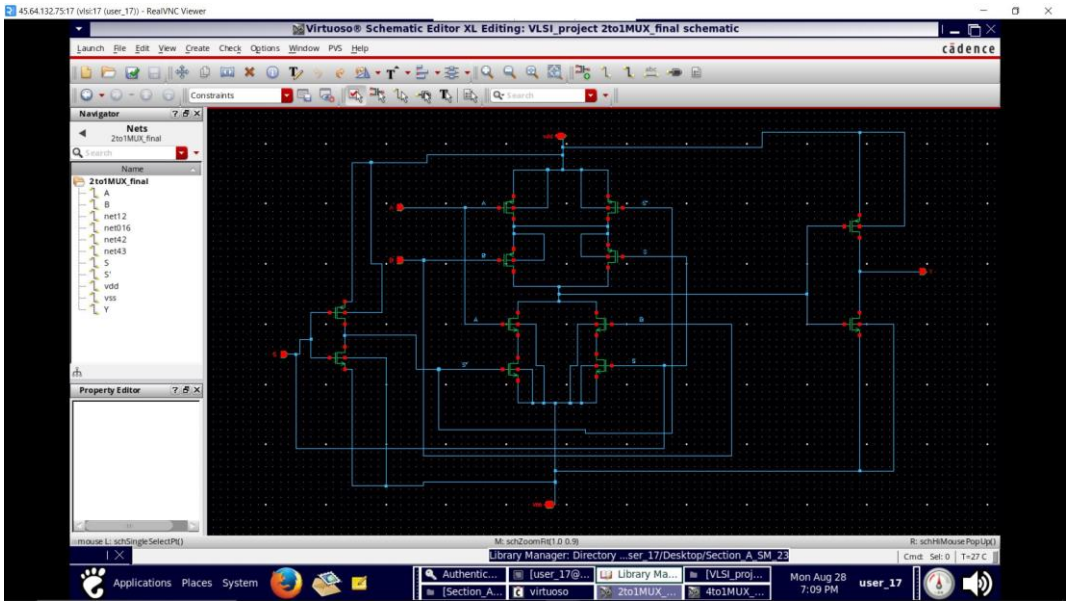

Fig.02: 2-to-1 MUX block

A 2-to-1 multiplexer (MUX) in CMOS design is a digital circuit that selects one of two input signals based on a control signal. It consists of two data inputs (A & B), one control input (S), and one output (Y). When C is low (0), D0 is selected, and its value appears at the output Y. Y=A.S'+B.S

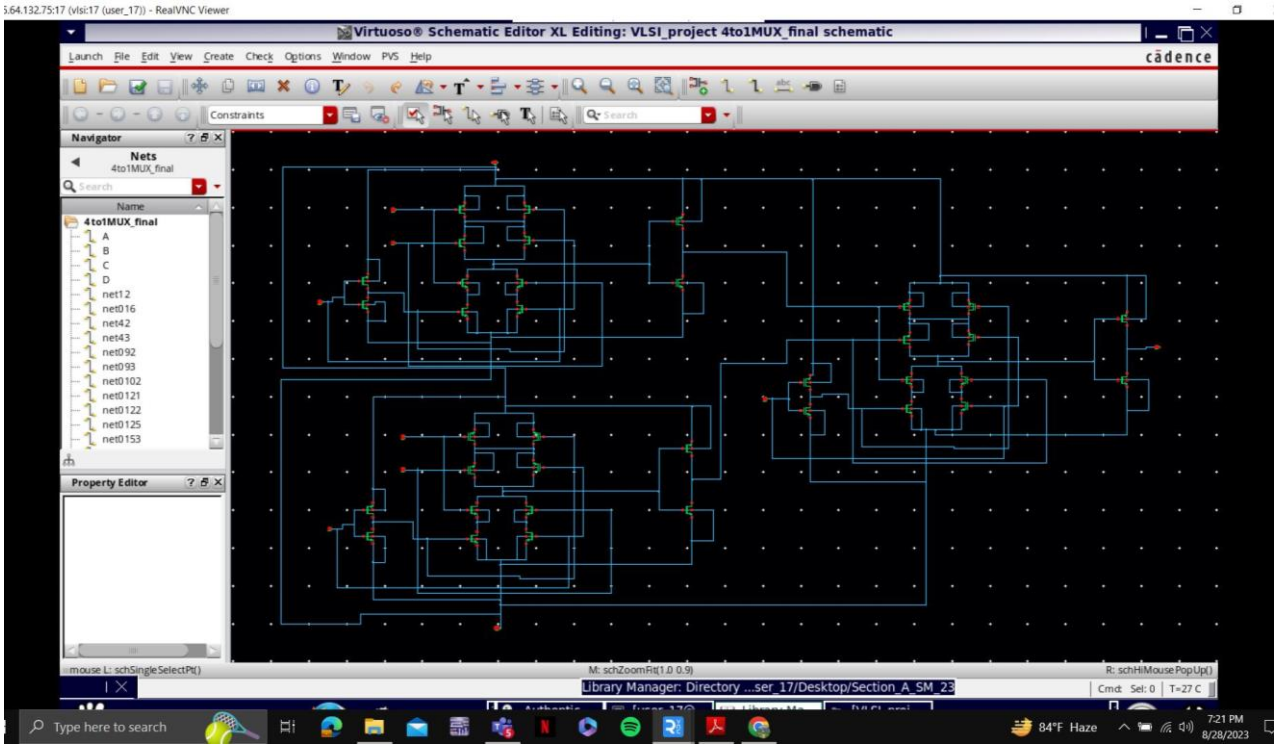

Fig.03: 4-to-1 MUX schematic

Simulation and Results: To verify the circuit for the 4-to-1 MUX transient analysis was completed and the results were compared with the truth table of 4-to-1 MUX.

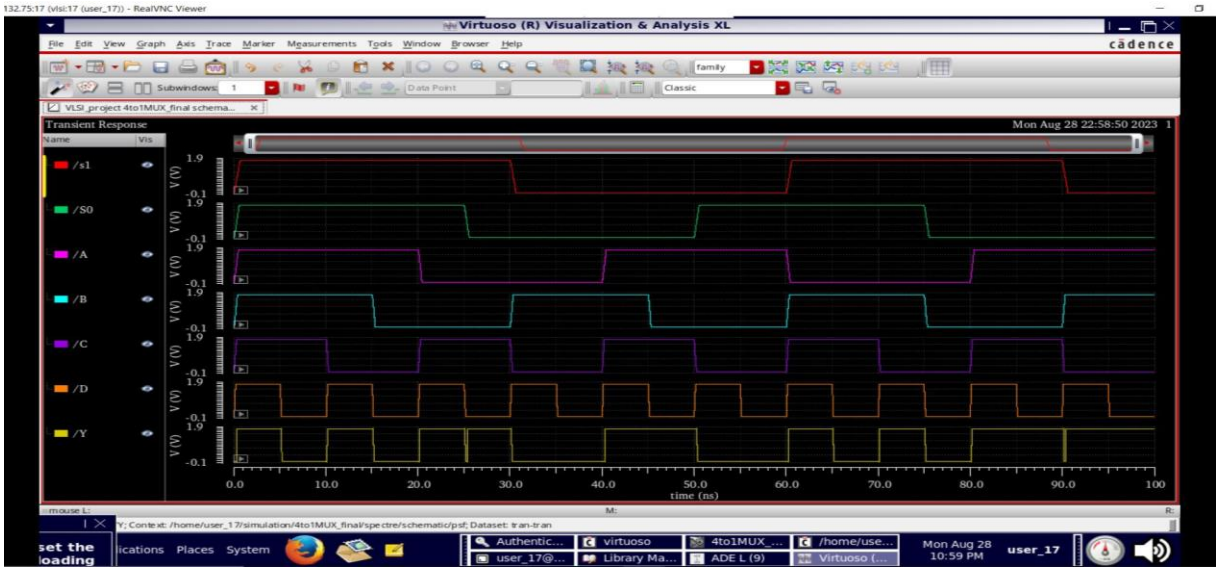

Fig.04: Transient analysis of 4-to-1 MUX

To do the simulation ADE L was chosen from the launch option. Then the transient analysis was chosen, and the stop time was set 100ns. Then the parameter was set for all the input and output pins. After running the simulation, the result below was determined. Then the result was compared to the truth table, and it was determined that the circuit was working fine.

Discussion and Conclusion: The 4:1 MUX design was effectively developed using the Cadence Design Environment, and the simulation results show that the designed MUX matches the intended parameters. The project report's discussion part will focus on design considerations, issues encountered, and recommended areas for further improvement. Several obstacles arose throughout the design process, including signal integrity issues and transistor size. Transistor sizing is an important part of the design process, and proper sizing can result in optimal circuit performance. Overall, the project gave hands-on experience with the Cadence Design Environment and developing a complicated digital circuit with CMOS technology. In conclusion, the design and implementation of a 4-to-1 multiplexer (MUX) using 2-to-1 multiplexers using CMOS has proven to be a versatile and efficient approach. By cascading two levels of 2-to-1 MUXes, we were able to effectively combine multiple data inputs into a single output based on the control signals. This method allowed us to minimize the complexity of the overall circuit while maximizing its functionality.

Reference:

[1] Teja, R. (2023, March 13). *Multiplexer (MUX) and Multiplexing*. ElectronicsHub. https://www.electronicshub.org/multiplexerandmultiplexing/

[2] *Digital Circuits - Multiplexers*. (n.d.). Tutorialspoint. https://www.tutorialspoint.com/digital_circuits/digital_circuits_multiplexers.htm