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Performance Study of 4:1 Multiplexer CMOS Logic Structures

M. Sumathi[1], Shakthimurugan K. H.[2] and K. Sumathi[3]

ABSTRACT

Now days, low power and low energy have become an important issue in consumer electronics and it is necessary to do research in combinational circuits. One of the important elements in digital circuits is a multiplexer or data selector for processing multiple inputs with a single output. Presently, multiplexers have become a universal logic element used to design any digital combinational logic circuits /systems in IC's, so it is needed to design or revise a multiplexer topology for low power consumption and high speed. In this paper, the different designs of multiplexer using complementary metal oxide semiconductor (CMOS) logic are analyzed in performance point of view. The multiplexer structures are realized using Positive Feedback Adiabatic Logic (PFAL), Cascode Voltage Switch Logic (CVSL) and Transmission Gate Based logic styles. The power consumption, delay, supply voltage and number of transistors present in the designs are tabulated and compared. The performance study is carried out using 0.18-µm CMOS technology. These different logic styles are differentiated by performing detailed transistor level simulations using CAD tools of DSCH3 and Micro wind 3.1.

Keywords: Multiplexers, CMOS, Transmission gate, Power Consumption, Delay, Area.

INTRODUCTION

A multiplexer (or mux) is a device that selects one of many analog or digital inputs signals and transfers the selected input information into a single output line. A multiplexer on 2n inputs has n select lines, which are used to select the input line for transferring the binary information to the output. These multiplexers are mainly used to increase the amount of data that can be sent over the network with in a certain amount of time and bandwidth. A multiplexer is also named as a data selector. A data selector makes it possible for several signals to share one device or resource, for example one analog to digital converter or one communication line instead of having one device per input signal. Multiplexer is essential component in digital design. It is extensively used within data path-intensive designs [1][2]. Data selector can be considered as a multiple-input and single-output switch, whereas a de-multiplexer is used as a single-input and multiple-output switch. The logic symbol for a multiplexer is an isosceles trapezoid with the longer parallel side containing the input pins and the short parallel side containing the output pin. The block diagram on the below shows in Figure 1 a many data lines to single multiplexer. The control/select lines wire connects the desired input to the output. In CMOS logic design half of the power is dissipated in PMOS network and stored energy is dissipated during discharging process of output load capacitor during the switching events. The energy taken from the power supply is not used fully and half of the energy is dissipated. In order to increase the energy efficiency of logic circuits, an efficient technique is required that can reuse the energy stored on load capacitor.

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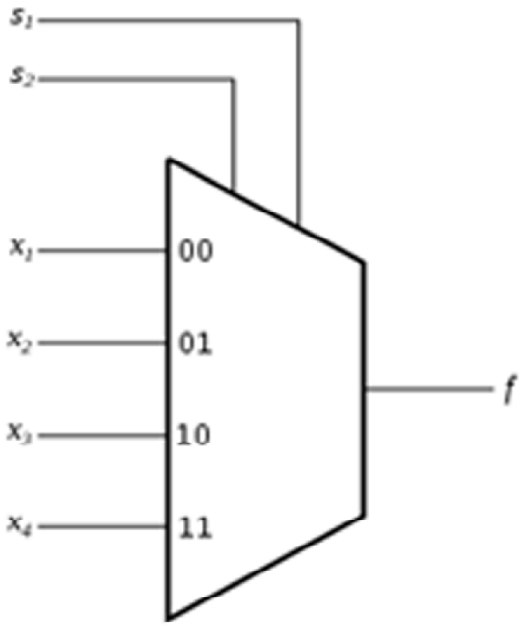


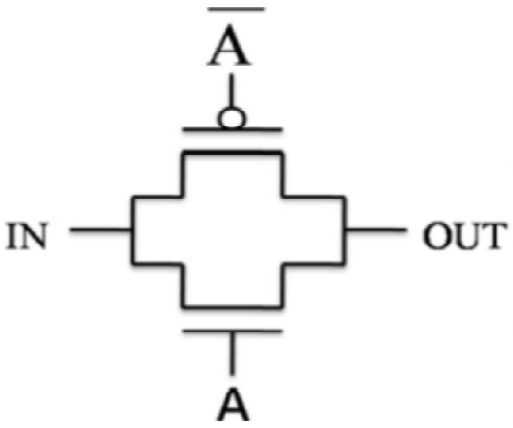
Figure 1: Block diagram of 4:1 multiplexer

It has been found that there is a fundamental relation between computation and power dissipation. The logic for computation could be implemented without any loss of information, and then the energy required for their operation can be potentially reduced to zero. It can be done by performing all computation in reversible manner. The energy dissipation depends upon average voltage drop traversed by charge that flows on to the load capacitance. By using smaller voltage steps or increments, the power dissipation can be reduced in digital designs [5]-[7]. The minimum power consumption needed during the charge transfer phase is termed as adiabatic switching. The adiabatic logic is also called as energy recovery CMOS, where charging is done by constant current source instead of constant voltage source as in conventional CMOS logic. It makes use of trapezoidal or sinusoidal waveforms as a power supply. The power dissipation can be controlled by reducing the supply voltage, switching activity and node capacitance value. By reducing the values of these parameters or by revising the topologies, an improvement in performance study is highlighted in many digital circuits.

BASIC LOGIC ELEMENTS

In CMOS logic style, multiplexer can be constructed by NMOS, PMOS pass transistors and transmission gates. Signal degradation takes place in NMOS and PMOS transistors due to the threshold effect so that good logic 1 / logic 0 levels could not be transmitted from input to output. Transmission gates are the best logic elements for transferring the binary information without any signal degradation. It is constructed by the two transistors PMOS and NMOS that are connected in parallel. The gate terminals are acting as normal and complementary control terminals. The graphical symbol, truth table of transmission gate is shown in fig. 2. (a), (b) respectively and also basic topology of logic styles are referred from reference papers that quoted in brackets.

The increasing requirement for low-power very large scale (VLSI) can assigned at different design levels, such as the architectural, circuit, layout, and the process technology level. In the circuit design level, the major part of potential for power stake exists by means of proper choice of a logic style for implementing combinational circuits. Exploration of low power logic styles reported in the research till now have mainly concentrated on particular logic cell, namely data selectors or mux, used in arithmetic circuits. At higher frequency to the frequency above, the CMOS logic can be used for continuing with low power consumption.



A	IN	OUT
H	H	H
H	L	L
L	X (don't care)	Z(high impedance)

Figure 2: (a) Graphical symbol [4] (b) Truth table

In the past decade, current mode logic structure based MUX circuits is highlighted in most international papers for high-speed systems in CMOS process. In this paper, 4:1 MUX is realized in different logic styles at 0.18-µm CMOS process. The paper is organized as follows: Section I and II highlights the introduction and basic logic elements and Section III describes the proposed 4:1 MUX designs. Simulation results and their comparisons are included in Section IV and finally Section V concluded the paper.

PROPOSED DESIGNS

CMOS gate configuration is the nucleus of all digital circuits and logic functions. It is constructed by NMOS pull down network and PMOS pull up network. Logic style is the method of representing the logic function with a set of transistors. It characterizes the speed, size, power dissipation and wiring of a circuit. All these factors may vary from one logic style to another and thus make the proper choice of logic style is essential for circuit performance.

(A) CMOS Transmission Gate Logic Based 4:1 Mux

The purpose and basic operation of a transmission gate can be used to isolate multiple signals with a minimal investment in board area and with a slight degradation in the characteristics of those critical signals. Transmission gate is used to block or pass a signal level from the input to the output. The solid-state-switch is comprised of parallel connection of a PMOS transistor and NMOS transistor. The control gates are biased in a complementary manner so that both transistors are either on or off. When the voltage on node A is a Logic 1, the complementary Logic 0 is applied to node active-low A, allowing both transistors to conduct and pass the signal at IN to OUT. When the voltage on node active-low A is when applied Logic 0, then the complementary Logic 1 is applied to node A, turning both transistors off and forcing a high-impedance condition on both the IN and OUT nodes. By using many transistors, the required functionality will consume much power with abundant area. At the same time technology is also scaled down, so that the circuit should be carefully designed to perform with minimum operating voltage and power consumption. As a result, the design is not considered more advantageous for lower technology. So, this paper concentrated on transmission gate based 4:1 multiplexer design. This comprised of 12 transistors only so power consumption is reduced with minimum area in proposed design. The general transistor level representation of a 4:1 multiplexer is shown in fig.3 Timing diagram of proposed transmission gate 4:1 multiplexer is shown in fig 4. It is logically verified the different states the circuit.

(B) Positive Feedback Adiabatic Logic (PFAL) Based 4 :1 Mux

PFAL logic is partial adiabatic method with dual railing. The basic circuit is given below in Fig.5. Adiabatic amplification is necessary for PFAL. PFAL latch consist of cross-coupled inverter pair. It also use power

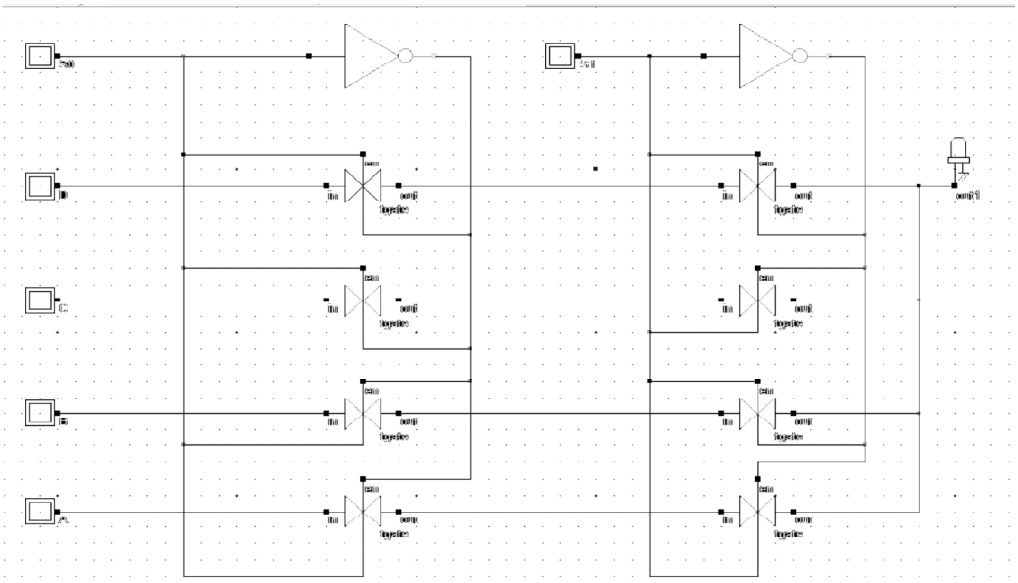


Figure 3: Schematic diagram of transmission gate based 4:1 multiplexer

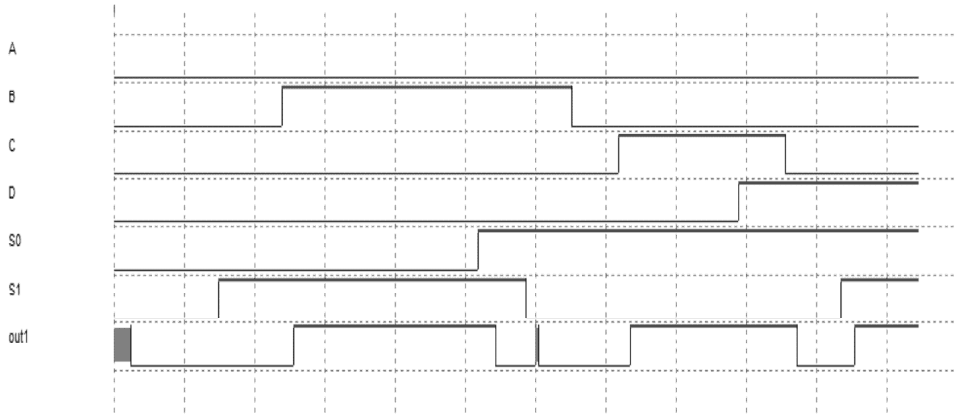


Figure 4: Timing diagram of transmission gate logic 4:1 multiplexer

clock instead of normal one that is used for energizing the logic networks. There is no extra dc power required and a time varying signal is used to activate the circuit elements alongwith the clocking control. One of the logic blocks connects the concerned input to the power clock with a low resistance path. The other logic network provides a very high resistance path in between the power clock and the other concerned output. One of the two outputs is pulled up to the power clock and other down to the ground. PFAL

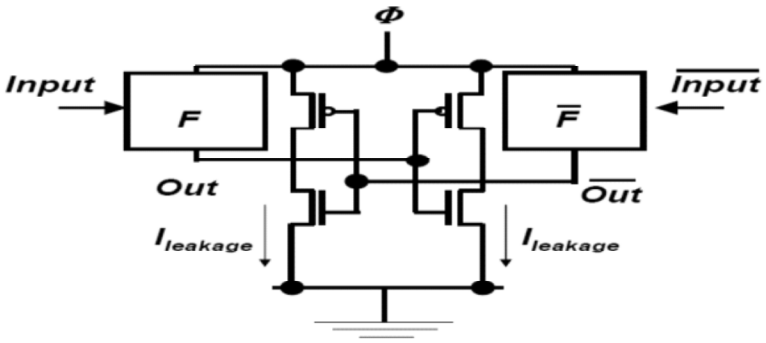


Figure 5: PFAL logic circuit [3]

minimize the signal deterioration on the outputs. It gives full swing like transmission gate technology and the logic blocks F and F' tree are in parallel with PMOS. F and F' functions handles the logic inputs. The resistance offered is lesser as compare to other adiabatic circuits.

The schematic diagram of the PFAL inverter gate is shown. PFAL uses four phase clocking rule to efficiently recover the charge delivered by power clock. The Fig 6 shows the schematic diagram of PFAL 4:1 multiplexer. Timing diagram of proposed 4:1 Mux is shown in fig 7. It logically verify the different states the circuit. Timing simulation is performed at schematic design.

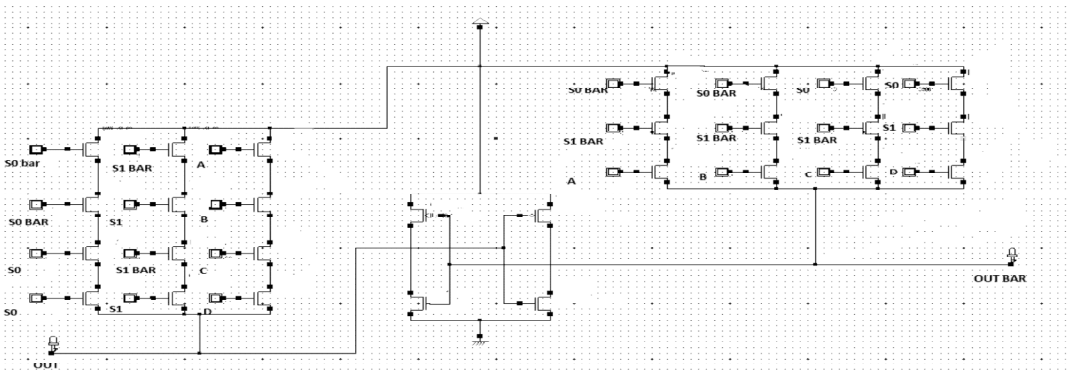


Figure 6: Schematic diagram of 4:1 positive feedback adiabatic logic

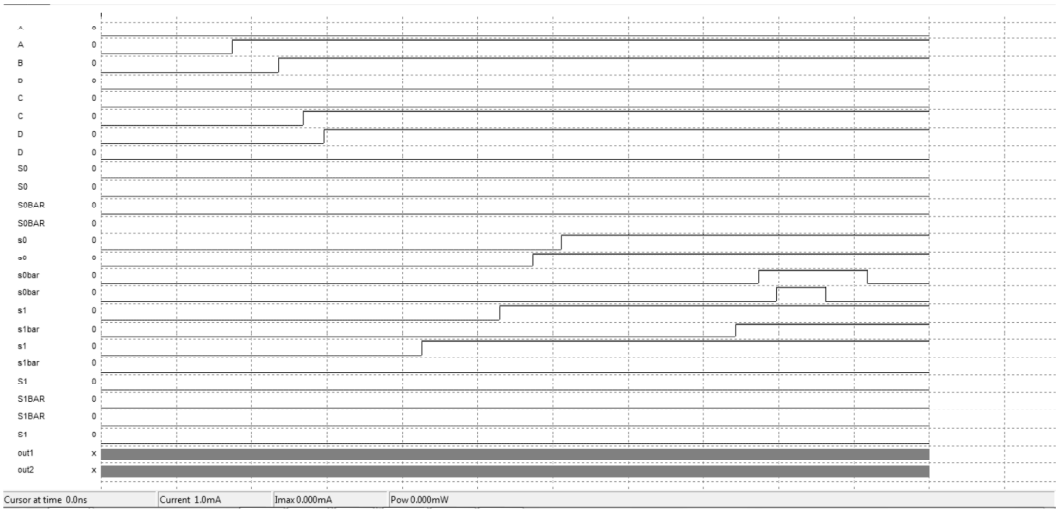


Figure 7: Timing diagram of positive feedback adiabatic logic 4:1 multiplexer

(C) Cascode Voltage Switch Logic Based 4:1 Mux

Cascode Voltage Switch Logic (CVSL) refers to a CMOS-type logic family which is designed for consuming low power. It mainly designed by using NMOS transistors to implement the logic using true and complementary input signals, and also used two P-channel transistors at the top to pull one of the outputs high. This logic family can also be called as Differential Cascode Voltage Switch Logic (DCVS or DCVSL). The fig 8 shows the logic circuit of CVSL.

The schematic diagram of cascade voltage switch logic based 4:1 multiplexer shown in fig. 9 is drawn using DSCH.

Timing diagram of proposed 4:1 Mux is shown in fig. 10. It logically verify the different states the circuit. Timing simulation is performed at schematic design.

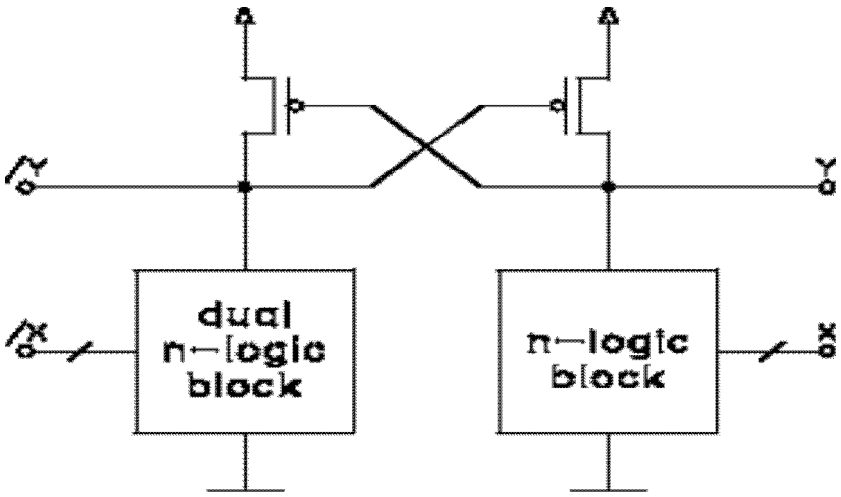


Figure 8: CVSL logic circuit [8]

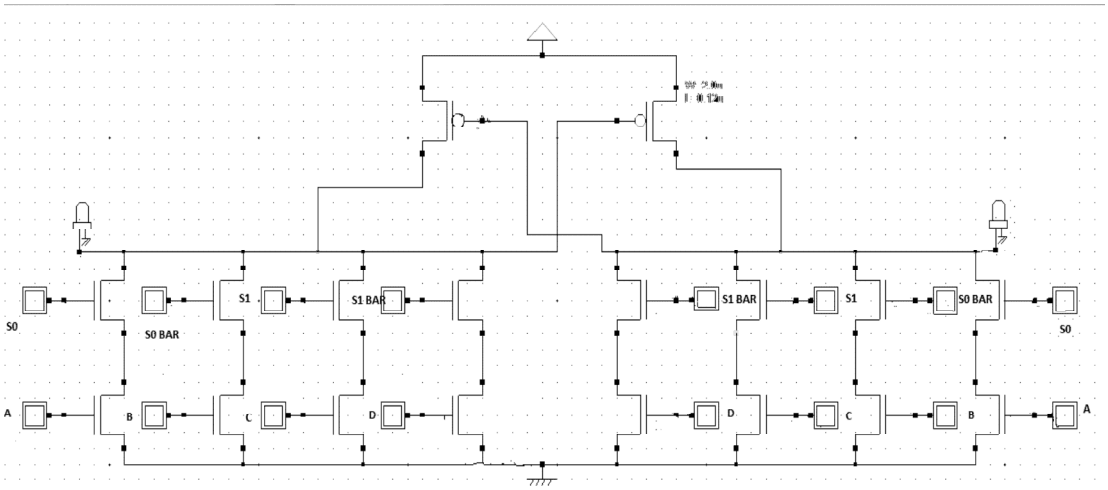


Figure 9: Schematic diagram of cascade voltage switch logic 4:1 multiplexer

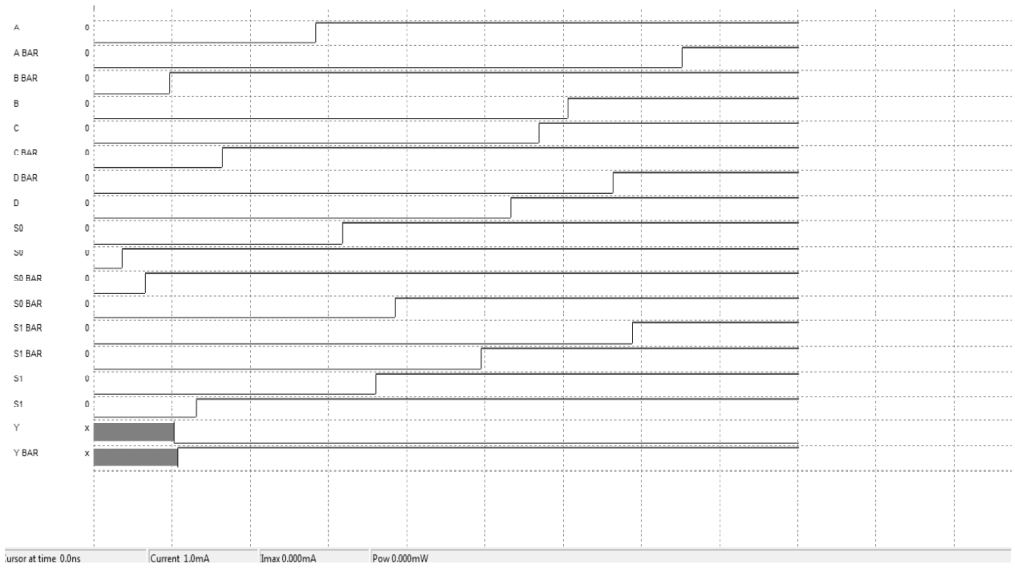


Figure 10: Timing diagram of cascade voltage switch logic 4:1 multiplexer

SIMULATION RESULTS

All simulations are done at Microwind 2.7 CAD tool. All schematic are drawn at 0.18 µm CMOS technology with 2.0 V supply voltage. Layout diagrams of different CMOS logic styles are shown in fig 11, fig 12, fig 13. IC layout design is the representation of an integrated circuit in terms of geometric shapes of semiconductor, metal and oxide layers that make up the components of the integrated circuit. Layout diagram is also the design procedure in which circuit specification is converted into physical implementation of the circuit.

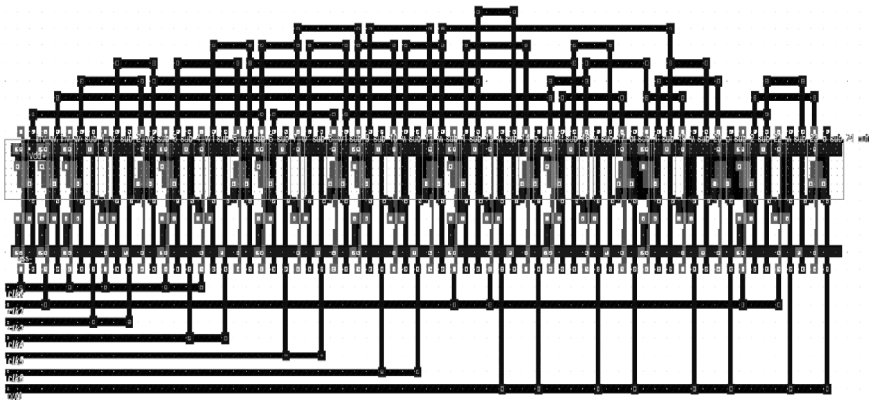


Figure 11: Layout diagram of transmission gate 4:1 multiplexer

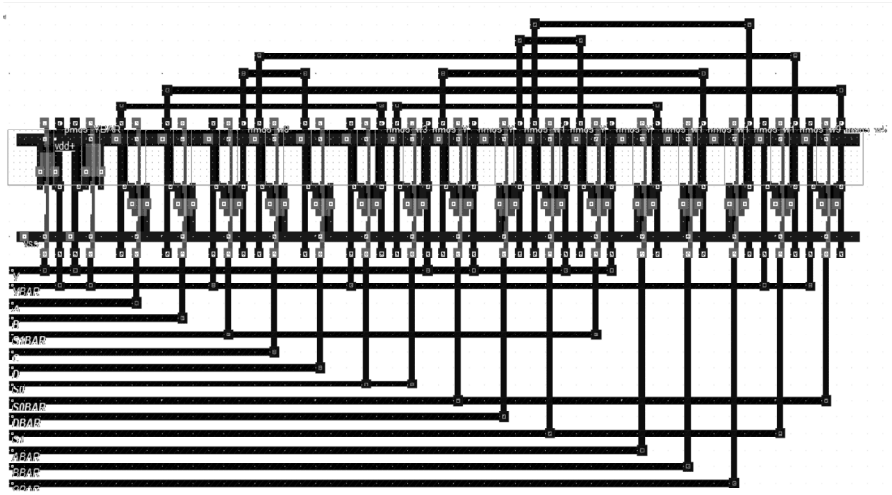


Figure 12: Layout diagram of positive feedback adiabatic logic (PFAL) 4:1 multiplexer

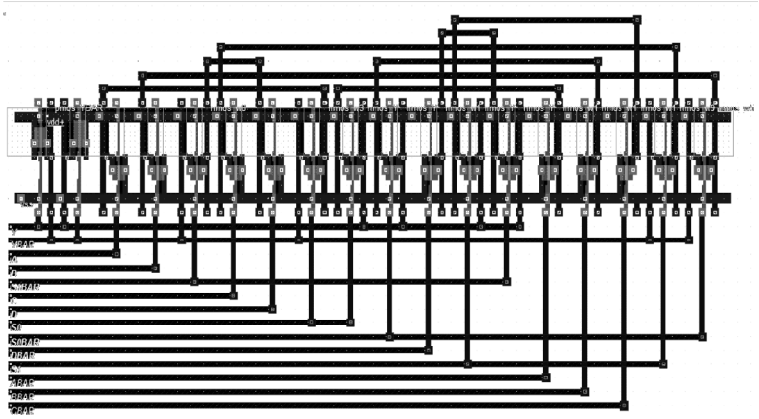


Figure 13: Layout diagram of Cascode voltage switch logic (CVSL) 4:1 multiplexer

Simulation is performed on the Microwind software. The fig 4, fig 7, fig 10 just shows the time domain simulation of multiplexer. The layout simulations are done at 0.18 µm technology. The fig 14, fig 15, fig 16 shows the layout simulations of the proposed 4:1 multiplexers.

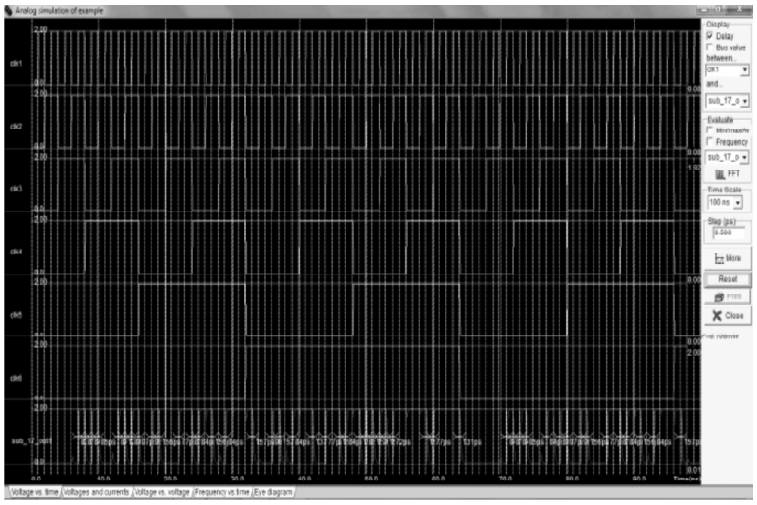


Figure 14: Layout simulation of transmission gate logic 4:1 multiplexer

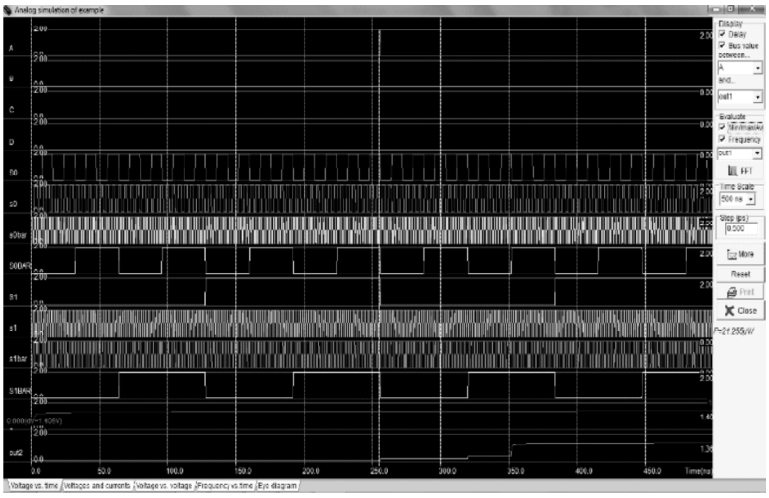


Figure 15: Layout simulation of positive feedback adiabatic logic 4:1 multiplexer

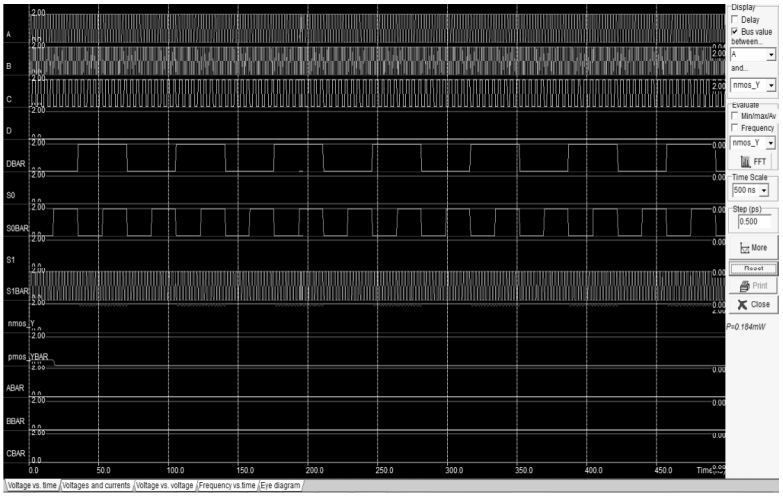


Figure 16: Layout simulations of cascode voltage switch logic (CVSL) 4:1 multiplexer.

In order to appraise logic diagram, it is developed using DSCH 2 and simulated in MICROWIND 2.7 on a platform. The aim is to compare the different logic styles in 4:1 multiplexer with the parameters like power dissipation, delay, and number of transistors. The simulated results for logic styles in 4:1 multiplexers are listed below for comparison. The comparison table and graphs are mentioned in Table- 1.

Table 1
Simulation Environment

Performance factor	*Transmission Gate*	*Positive feedback adiabatic logic*	*Cascode Voltage Switch Logic*
Power Dissipation	0.106 mW	21.255 µW	0.184 mW
Delay	83 ps	117 ps	95ps
Number of Transistors	36	28	46
Supply Voltage	2 v	2 v	2v
Temperature	27° c	27° c	27° c

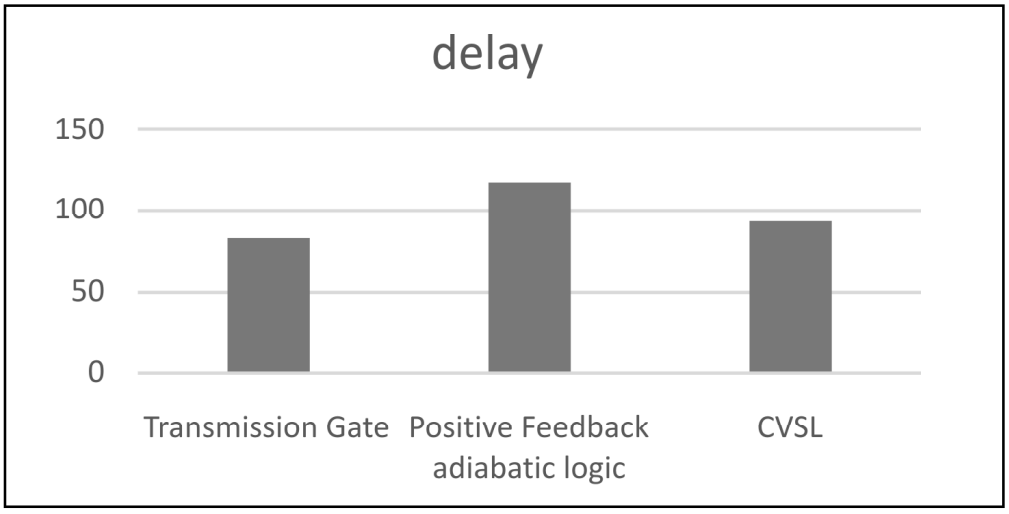


Figure 17: Comparison of Delay

CONCLUSION

In this paper, different logic style multiplexers have been designed, simulated, analyzed and compared. The post layout simulations of new improved 4:1 CMOS MUX designs are also highlighted. We observed that transmission gate design based 4:1 multiplexers are faster than when compared with positive feedback adiabatic logic and cascade voltage switch logic (CVSL). The delay in transmission gate logic is 83ps whereas it is 117ps and 95ps in positive feedback adiabatic logic and cascade voltage switch logic respectively. In transmission gate based logic 4:1 multiplexers has less power consumption and delay in 0.18 µm technology. The number of transistors used is high in transmission gate based 4:1 multiplexers. The net effect is that proposed 4:1 multiplexer shows better performance than the other logic styles.

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