POWER MANAGEMENT INTEGRATED CIRCUITS

PROJECT - 1

Linear Dropout Voltage Regulator

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- Circuit Diagram

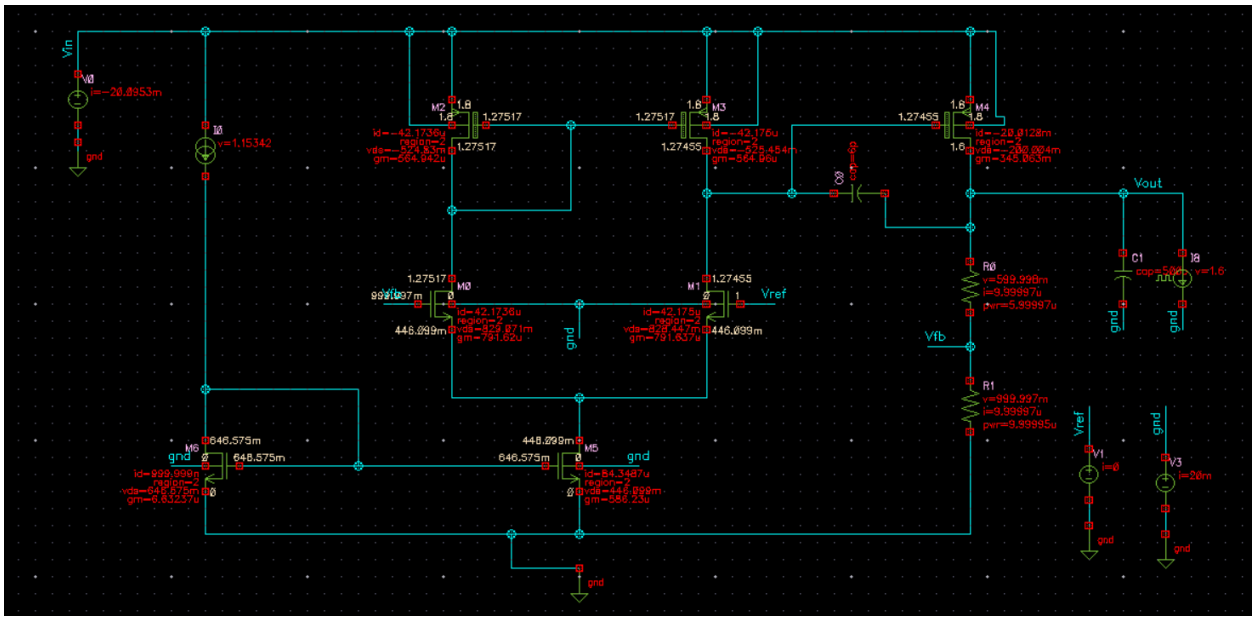

Fig 1: Schematic layout

Parameters	Values
Vin	1.8 V
Miller Capacitance(C_c)	6p F
Load Capacitance	500p F
Vref	1 V
R_1	60k Ω
R_2	100k Ω
Load Current	100m A

Table 1: Basic Parameters

- Transistor Ratios

Transistor	Width (W)	Length (L)	Multiplier (m)	W/L Ratio	Vov(V)
M0(Nmos Differntial Pair)	7 µm	1 µm	8	56/1	37m
M1(Nmos Differntial Pair)	7 µm	1 µm	8	56/1	36m
M2(Pmos Current Mirror)	10 µm	1 µm	10	100/1	112m
M3(Pmos Current Mirror)	10 µm	1 µm	10	100/1	112m
M4(Pass Transistor)	100 µm	0.18 µm	200	20000/0.18	66m
M5(Tail Transistor)	7 µm	5 µm	6	42/5	269m
M6(Tail current Mirror)	0.525 µm	0.18 µm	1	0.525/0.18	284m

Table 2: Transistor ratios

- Size of Transistors

* Size of Transistors

1) for PMOS Transistor

$$I_D = 1/2\, K_P \frac{W}{L} (V_{GS} - V_{th})^2$$

$$I_D = 1/2\, K_P \frac{W}{L} (V_{GS} - V_{th} \approx V_{OV})^2$$

From Design of diode connected PMOS we got,

$K_P \approx 50 \mu A/V^2$, Given :- $V_{OV} = 0.2V$

$I_D = 100mA$

$$100mA = 1/2 \times 50 \times 10^{-6} \times \frac{W}{L} \times 0.04$$

$\frac{W}{L} = 100,000$, taking L to be Minium

$L = 0.18 \mu m$, $W = 18,000 \mu m$

→ Given, Settling time $\leq 1\mu s$

5τ = (S_time $\approx 1\mu s$)

$\Rightarrow \tau = 0.2\mu s = \frac{1}{BW}$ *

$$BW = \frac{1}{0.2\mu s} \Rightarrow 5MHz$$

$$\omega_{ugb} = \frac{g_{m_1}}{C_c + C_{gg}}$$

C_{gg} → Cap of Pass gate transistor

$C_{gg} \simeq 26\,pF$ from Design,
$C_c = 6\,pF$

$5MHz \simeq \omega_{ugb} = \frac{g_{m_1}}{(6+26)\times 10^{-12}}$

$\Rightarrow 2\pi \times 5\times 10^6 \times 32\times 10^{-12} = g_{m_1}$

$\Rightarrow 160\times 2\pi = g_m$

$1004.8 \simeq g_{m_1}$ (Gain of differential pair)

Now

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times I_{out}}{V_{in} \times (I_{out} + I_q)}$$

$I_q \hookrightarrow 122\mu A$

$\eta = 88.78\%$

~~*~~ Size of NMOS differential pair

$$g_{m_1} = \frac{2I_D}{V_{OV}}$$

taking $2_D = 50\mu A$

$1004.8 = \frac{2\times 50\times 10^{-6}}{V_{OV}}$

$V_{OV} \simeq 0.10\,V$

$k_n = 270 \mu A/V^2$

$$I_D = 1/2\, k_n (W/L)(V_{OV})^2$$

$$50 \times 10^{-6} = \frac{1}{2} \times 270 \times 10^{-6} \times W/L \times 0.01$$

$$\Rightarrow \frac{100}{2.7} = W/L$$

$$W/L \approx 37$$

* Now pmos current Mirror

$$I_D = 1/2\, k_p (W/L)(V_{OV})^2$$

$\Rightarrow$ taking $I_D = 50 \mu A$, $V_{OV} = 0.2$

$$W/L = 50$$

* for Tail Transistor

$$I_D = 1/2\, k_n (W/L)(V_{OV})^2$$

taking $V_{OV} = 2.7V$, $I_D = 50 \mu A$

$$\Rightarrow W/L = 8.4$$

and $(W/L)_{tail} = (W/L)_{its\ current\ Mirror} \times \frac{1}{50/100}$

$\Rightarrow (W/L) = 0.105$ 0.084

- Stability Summary

Load(mA)	Phase Margin	Gain Margin	BandWidth	Loop Gain
20m	61.75 °	16.441 dB	5.92 MHz	71.95 dB
50m	66.75 °	19.97 dB	5.72 MHz	69.67 dB
100m	70.186 °	22.96 dB	5.22 MHz	69.362 dB

Table 3: stability summary

- Block wise power consumption

Blocks	Light Load	Nominal Load	Full Load
Feedback	17µ W	17µ W	17µ W
OTA	152.468µ W	152.47µ W	152.471µ W
Pass transistor	4m W	10m W	20m W

Table 4: Power Consumption

- Loop Gain
    1. At Light Load(20mA)

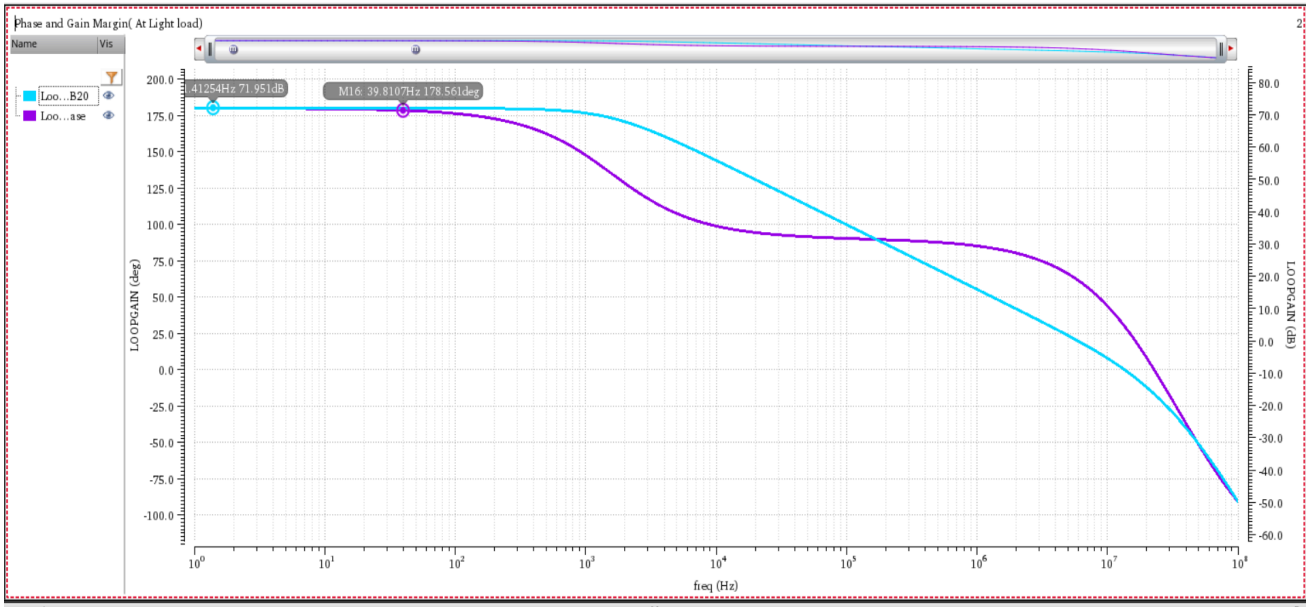

Fig 2: Loop Gain at Light load

2. At Nominal load(50mA)

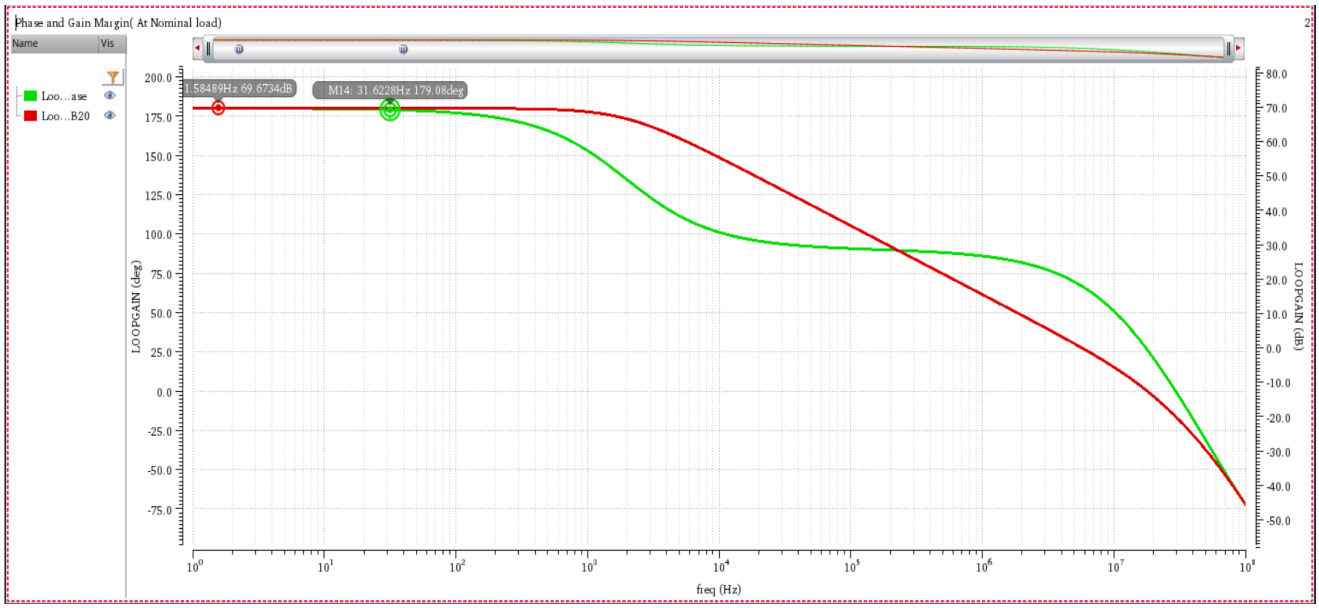

Fig 3: Loop Gain at Nominal load

3. At Full Load(100mA)

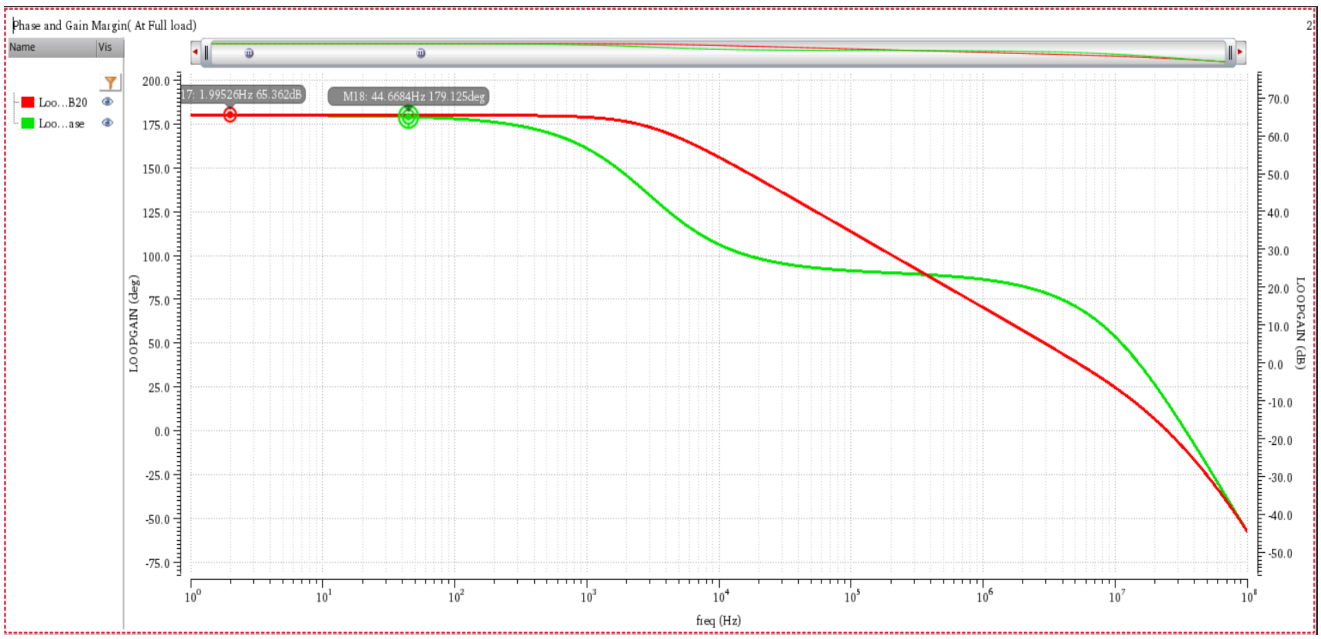

Fig 4: Loop Gain at Full load

- PSRR(Power Supply Rejection Ratio)

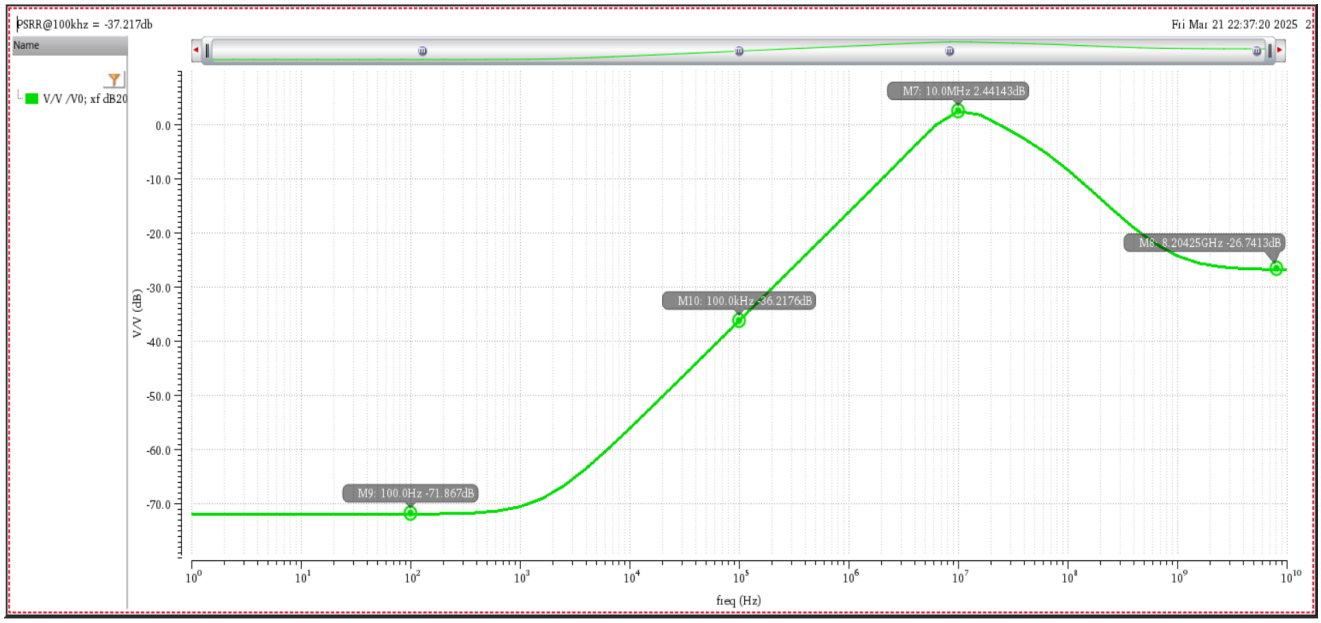

Fig 5: PSRR at light load

- Efficiency

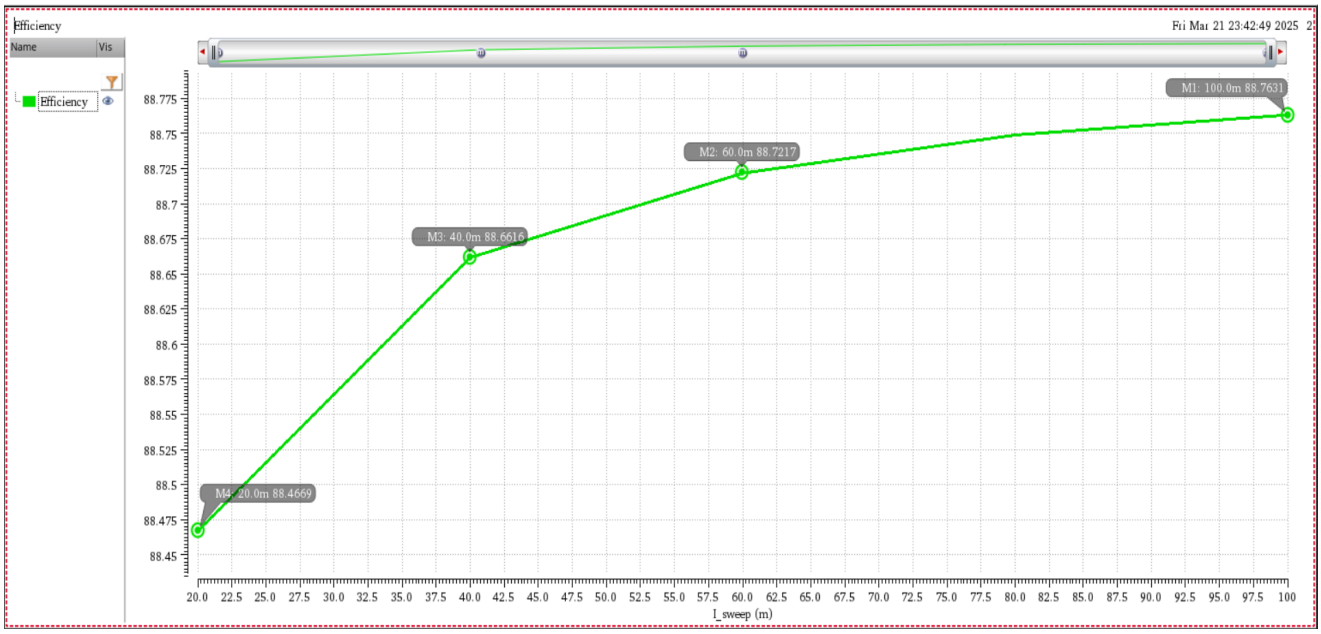

Fig 6: Efficiency across load range(Light to Nominal)

- Line Regulation

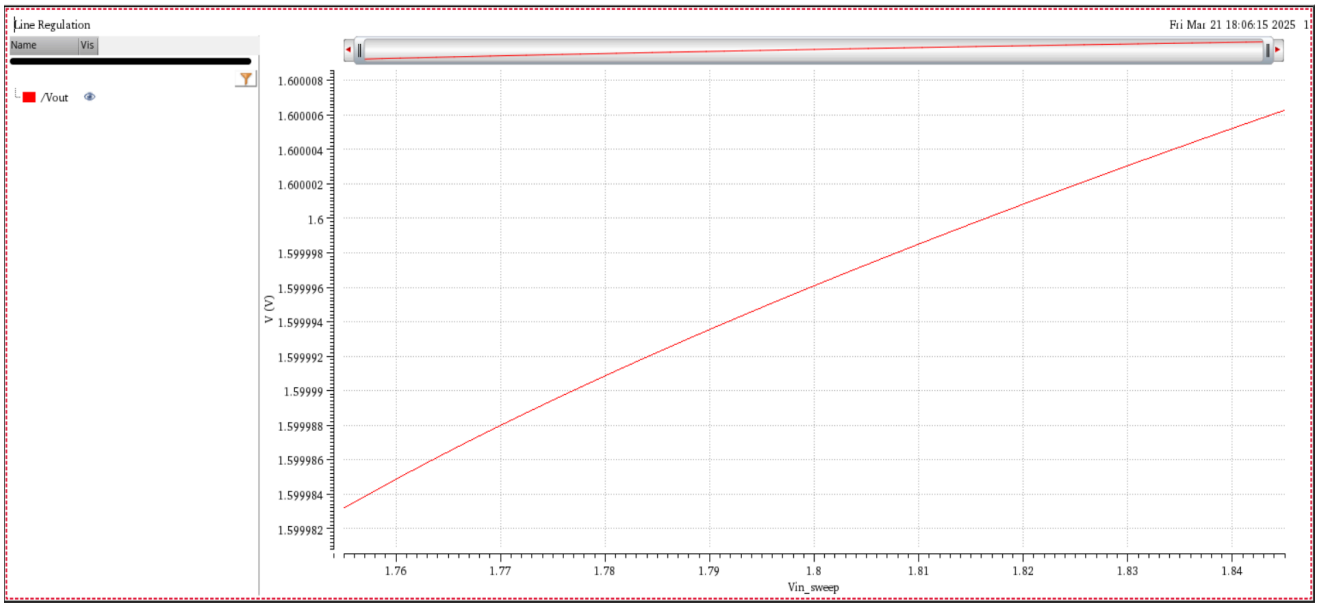

Fig 7: Line Regulation

- Load Regulation

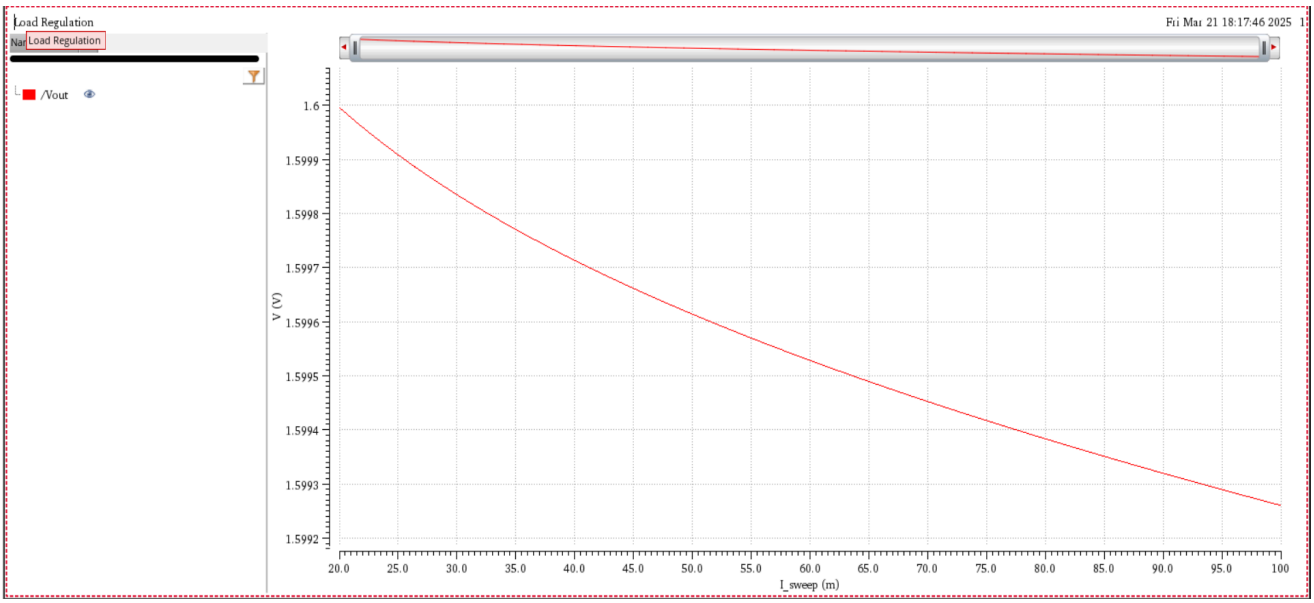

Fig 8: Line Regulation

- Transient Response(At Light Load - Nominal Load)

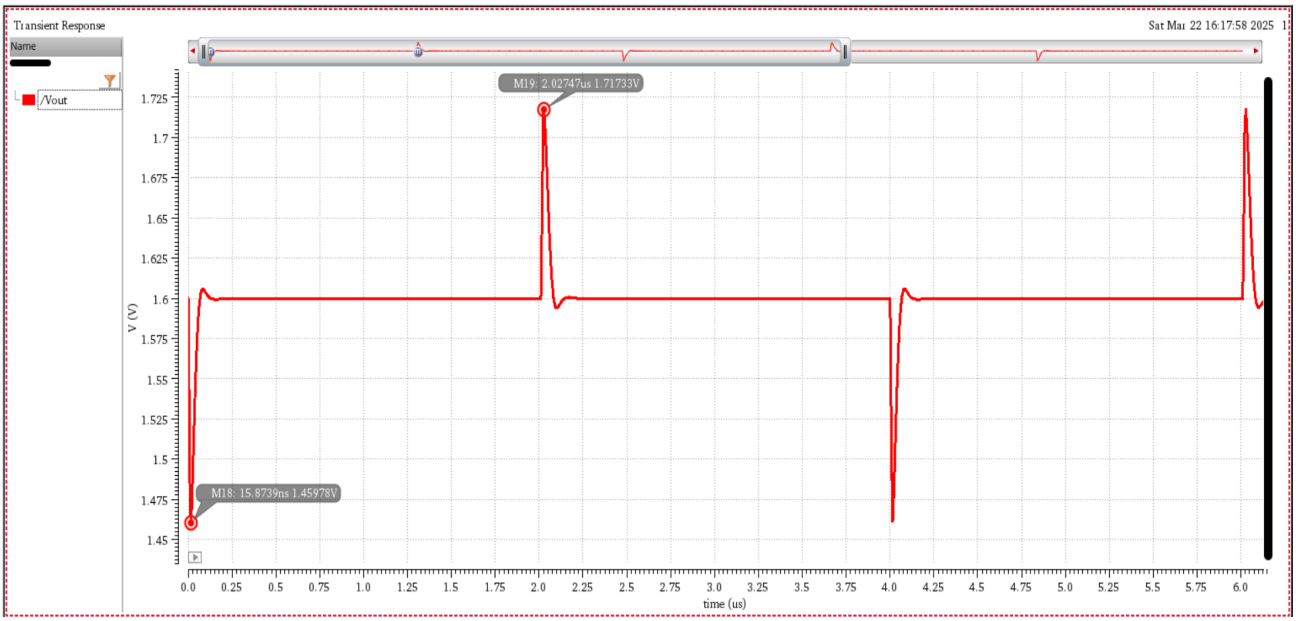

Fig 9: Transient response

- Settling time(Transient response)

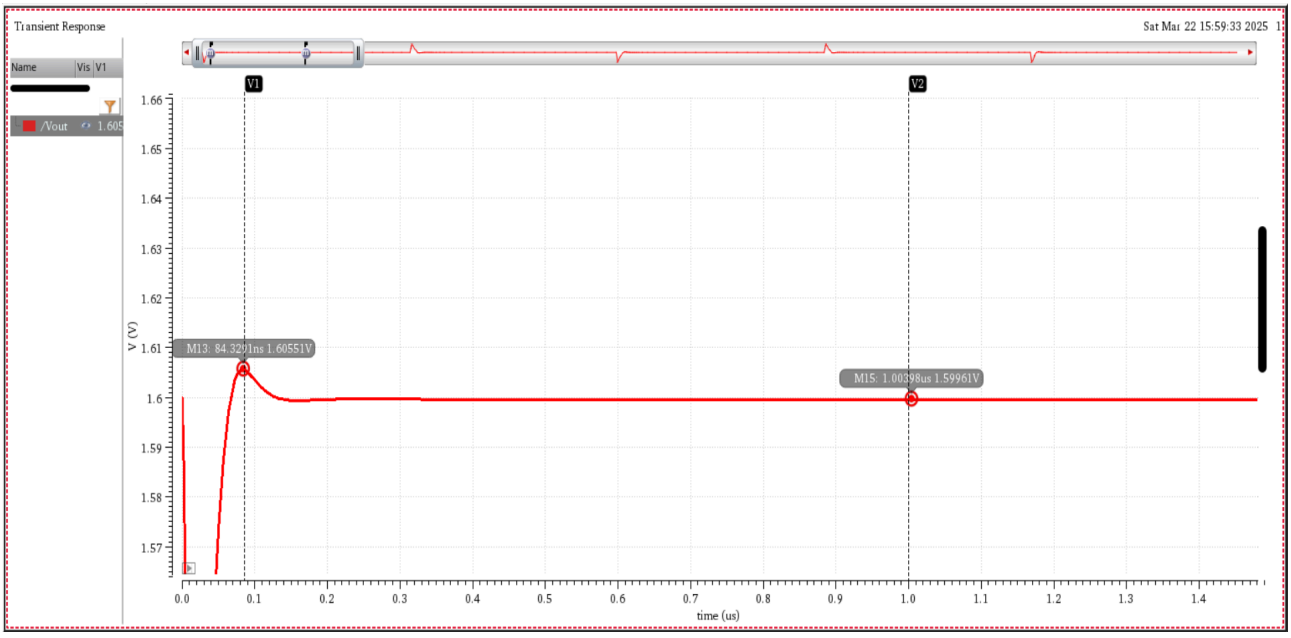

Fig 10: Settling time(< 200n s)

Load Range	Overshoot	Undershoot	Settling Time
20m A → 50m A	-	140m V	200n s
50m A → 20m A	117 mV	-	200n s

Table 5: Transient response

- Final Results

Parameters	***Behaviour***
PSRR	-36.21 dB at 100KHz
Load Regulation	≤ 0.05% Across Load Range
Line Regulation	≤ 0.00125 for ± 2.5% of Input voltage
Phase Margin	≥ 61.75% across Load Range
Efficiency	≥ 88.46% across Load Range
Transient response	Settling time(< 200n s)
	Overshoot/Undershoot ≤ 140m V

Table 6: Final summary