

Moosa Qaisar

+92 3125480489 | moosaqaisar@outlook.com | [linkedin.com/in/moosa-qaisar/](https://www.linkedin.com/in/moosa-qaisar/) | github.com/rajput-musa

SUMMARY

Aspiring Computer Engineer with strong foundations in hardware design, software development, and network. Skilled in leveraging Linux environments, cloud technologies, and programming to build practical solutions. Eager to apply strong problem-solving skills and a collaborative approach in a challenging role, driven by a passion for continuous learning and technological innovation.

EDUCATION

University of Engineering and Technology, Taxila

Bachelor of Science in Computer Engineering

Expected 2025 GPA: 3.36

Punjab Group of Colleges

FSc Pre Engineering

Marks: 961/1100 (87%)

TECHNICAL SKILLS

Languages: Python, C/C++, JavaScript, HTML/CSS, MATLAB, Verilog, SQL

Developer Tools: Git, Linux, Opti System, Google Cloud Platform, VS Code, Visual Studio, PyCharm, IntelliJ, Android Studio

Libraries: TensorFlow, Keras, scikit-learn, OpenAI, Pandas, NumPy, Matplotlib

Hardware: Microcontrollers, Arduino, FPGA

EXPERIENCE

NeuronTech

June 2023 – Aug 2023

Research Intern

- Conducted research and development on Apache Sparkx for large-scale data processing
- Developed prototypes and simulations for data applications
- Designed and developed simulation environments to model real-time big data ingestion and processing pipelines across clustered nodes.
- Performed throughput analysis, evaluated fault-tolerance mechanisms, and documented optimization strategies.

Levrify

Sep. 2024 – Oct. 2024

Data Science Intern – Remote

- Worked extensively with Excel, SQL databases, and Power BI to collect, clean, and organize large datasets for business analytics projects.
- Designed and developed interactive dashboards and visual reports to communicate key performance metrics and business insights to stakeholders.
- Completed a capstone project and qualified for AWS Cloud Practitioner training.

PROJECTS

FYP on AES Core Hardware Accelerator on FPGA (Artix-7) | Verilog, Vivado, Xilinx ISE, Digilent Adept

- Designed and implemented a pipelined AES encryption and decryption core optimized for secure, high-speed communication systems.
- Researched and explored optimized S-box designs, countermeasures against side-channel attacks (such as Differential Power Analysis).
- Developed simulation test benches using Xilinx ISE, Vivado, and iSim tools to validate functionality.
- Analyzed resource utilization (LUTs, flip-flops) and achieved high throughput across FPGA prototypes.

VOIP Server Deployment using Asterisk | CentOS

- Installed, configured, and deployed an Asterisk VOIP server on CentOS Linux.
- Manually set up configuration for user management and call routing.
- Established and tested softphone connectivity using MicroSIP, verified successful signaling and voice communication between endpoints.
- Demonstrated internal calling functionality across a simulated network environment between users.

Active Directory Domain Services (ADDS) Corporate Setup | Windows Server 2024

- Architected a full-fledged ADDS setup including domain controllers, user and group creation, policy management, and firewall configurations.
- Configured DNS and DHCP servers to manage network addressing and name resolution.
- Deployed Group Policy Objects (GPOs) for centralized administration of users and systems across a dummy corporate network of users.

Free Space Wireless Communication System | OptiSystem, MATLAB

- Designed and optimized a long-distance wireless communication link to maximize data rates.

- Analyzed Q-factors and signal integrity using domain and frequency analyzers.

Macro Keyboard | *Arduino*

- Designed and developed a custom macro keyboard to automate tasks.

OTHER

Clubs/Societies: Ex-Graphic designer at NYA, UET Taxila

Interesting Fact: My Macro Keyboard project won best performance in MCSD project exhibition.