The Era of High Bandwidth Memory

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Who am I?

- Kevin Tran
- Senior Manager Technical Marketing
- HBM Product and Ecosystem Champion
- DRAM Memory Solutions for Automotive, Infrastructure and Networking.
- Emerging Memory Technologies

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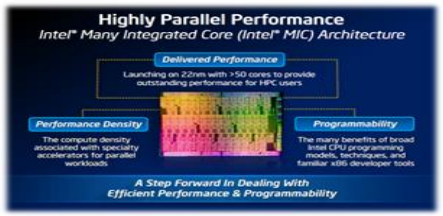
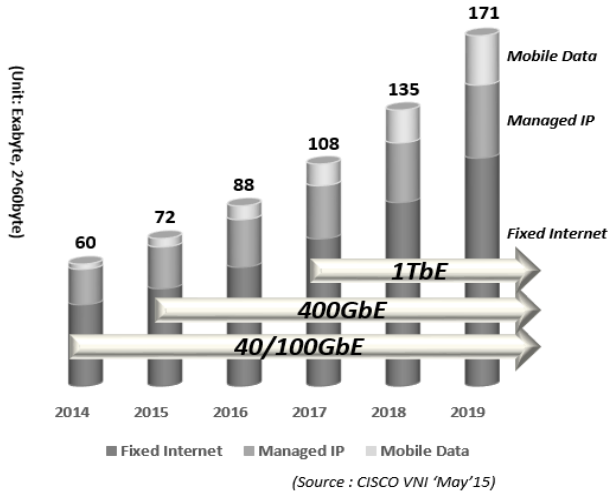
Major Trends Driving Higher Memory Performance

Scaling of DRAM memory density, bandwidth and form factor are critical for next generation processing architectures

HPC: Continuous Increasing of Cores



Infrastructure: Unprecedented Growth of Data



(Source : CISCO VNI 'May'15)

Graphics: Increasing High Performance Graphics Card Max. *Fillrate*

**Number of pixels a graphics card can provide and write to video memory (per sec);*
No. of raster operations (ROPs) X GPU clock frequency

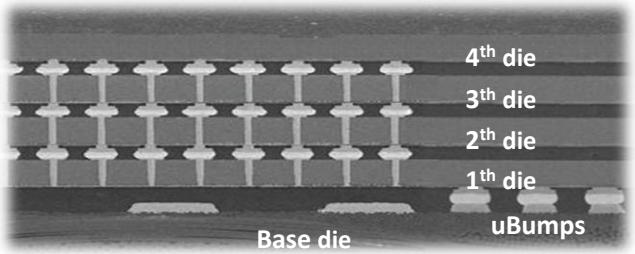
Network: Ethernet Speed Demands Scaling of Memory Bandwidth

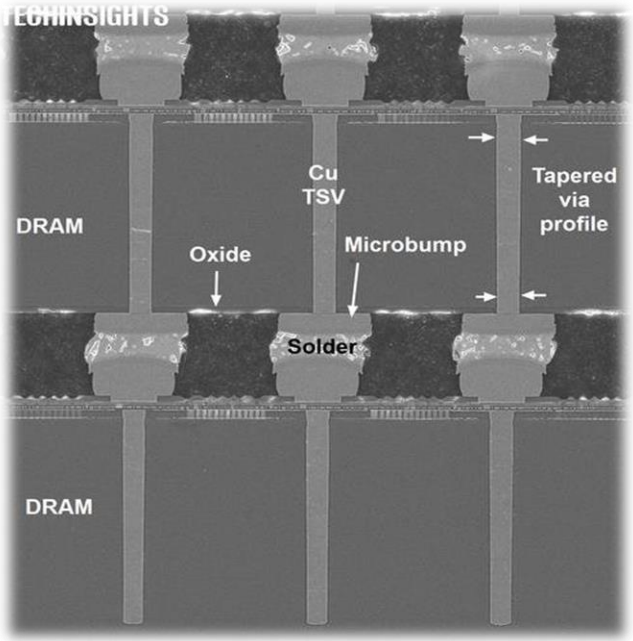
	Ethernet Interface					
	10GbE	25GbE	40GbE	100GbE	400GbE	1TbE
Speed*	30Gbps	75Gbps	120Gbps	300Gbps	1.2Tbps	3Tbps

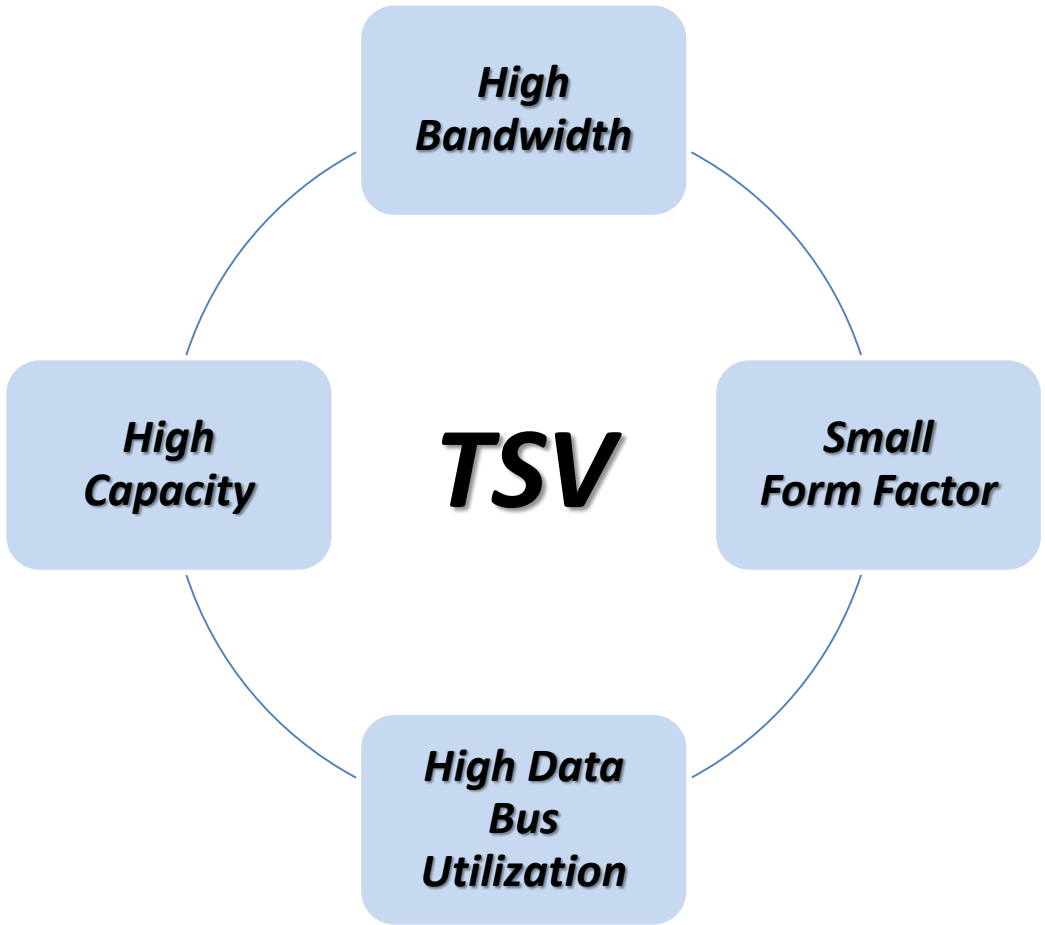
**Speed = Read/Write x Overhead 150% x Ethernet Interface*

High Bandwidth Memory & TSV

Through Silicon Via (TSV) technology enable DRAM memory to overcome existing performance challenges





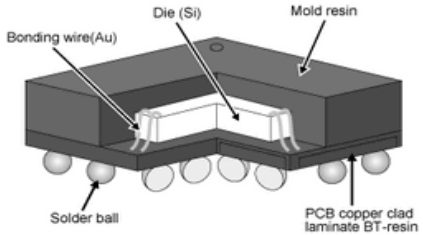


2. High Bandwidth Memory Overview

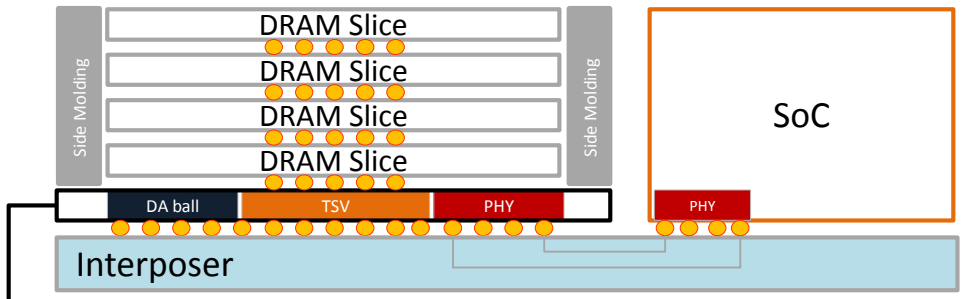
HBM, What Exactly Is It?

Known Good Stacked Die(KGSD) DRAM Memory for 2.5D System in Package integration

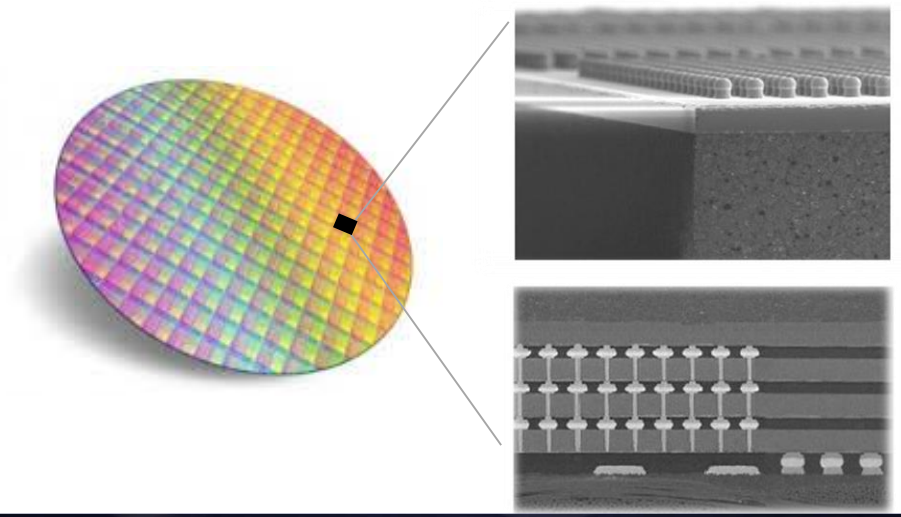
Fine Ball Grid Array (FBGA)

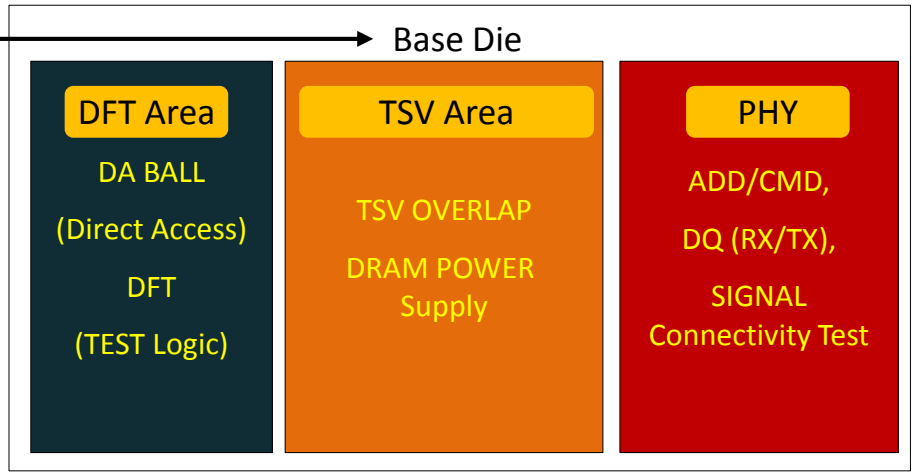


HBM in SiP



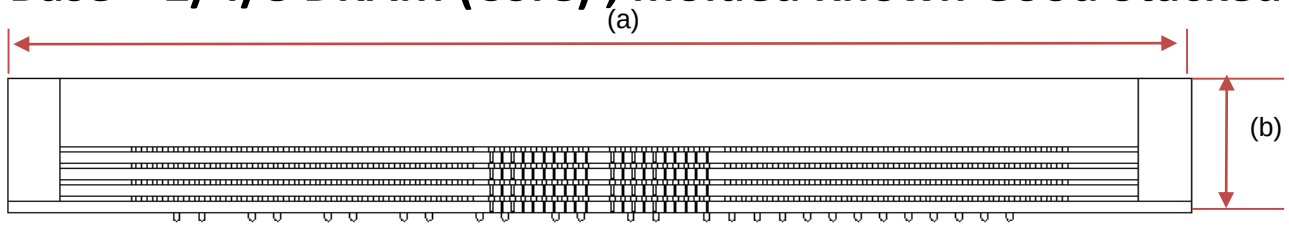
Known Good Stacked Die (KGSD)



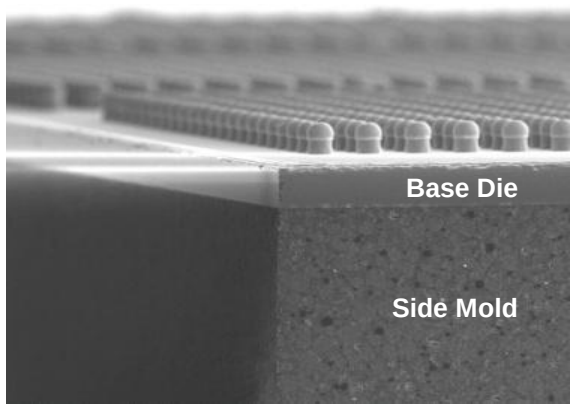


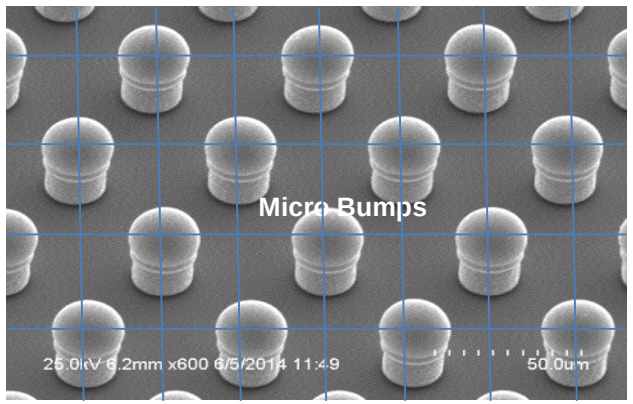
Mechanical Outline : molded KGSD

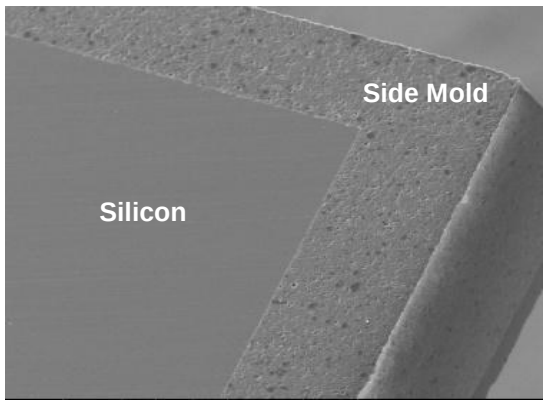
- **mKGSD (1 Base + 2/4/8 DRAM (Core) ; molded Known Good Stacked Die)**



	Item	Value	Bump		Remark
			CD	Pitch	
(a)	Gen1 - Package Dimension (X, Y)	5.48 mm x 7.29mm	25um (As Reflow)	55um	Face Centered Rectangular (FCR) pattern ubump
	Gen2 - Package Dimension (X, Y)	7.75 mm x 11.87mm			FCR
(b)	Gen1 - Package Body Height (Z)	0.49 mm			
	Gen2 - Package Body Height (Z)	0.72 mm			
	Micro Bump Array (MPGA)	JEDEC	-	-	JC11-2.883, JC11-4.884

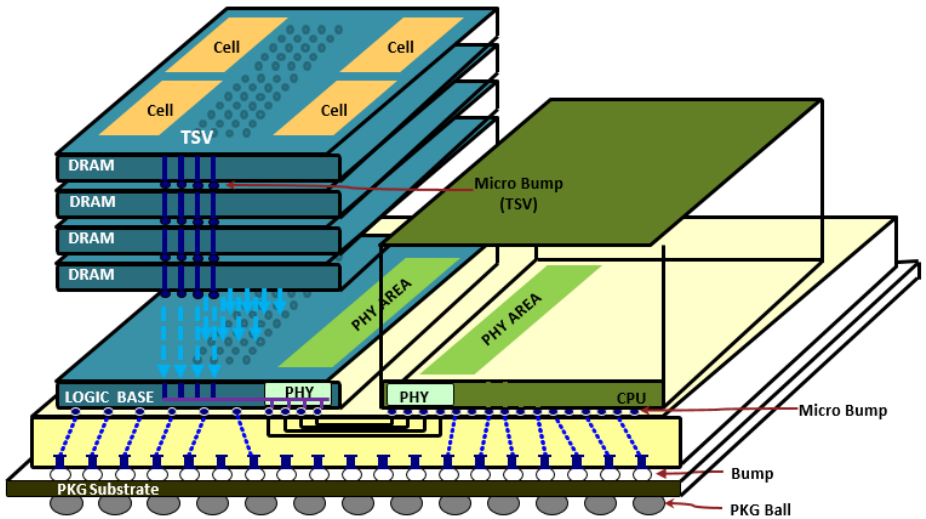






HBM Functional Overview

HBM 1024 IO from base die PHY region connect to host PHY through the interposer

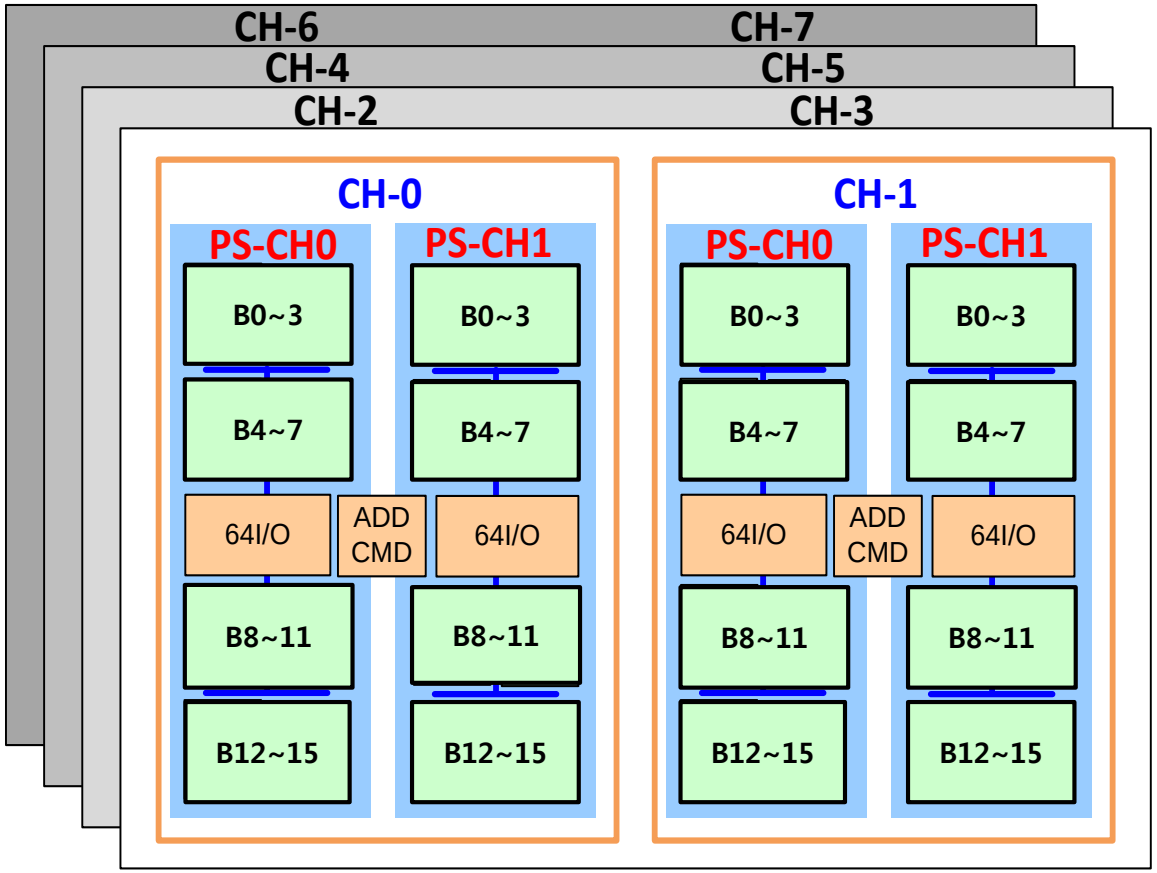


Features	Spec
Burst Length	2, 4
# of Die per Stack	2/4/8 DRAM (+1 Base Die)
Density per Stack	2GB 4GB 8GB avail
Channels / Stack	8
Channel / DRAM Slice	Up to 8 (2/4)
Banks / Channel	8/16
IO / Channel	128
Prefetch / Channel	32B (128x2bit)
Total Data IO Width	1024
Logic Buffer Data IO / Rate	1024 DQ's @ 1GT (500MHz)
Peak Read BW / Stack	Up to 256GB/s
Page Size	2KB
DRAM Core voltage	1.2V
Logic Buffer IO voltage	1.2V

HBM Architecture

Each DRAM core die consists of a number of Channels

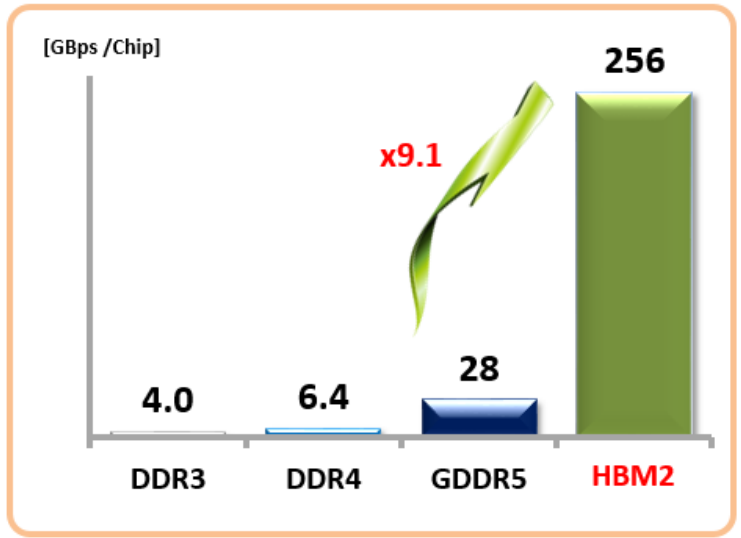
Pseudo Channel Mode - separate IO but independent ADD/CMD for each pseudo-channel



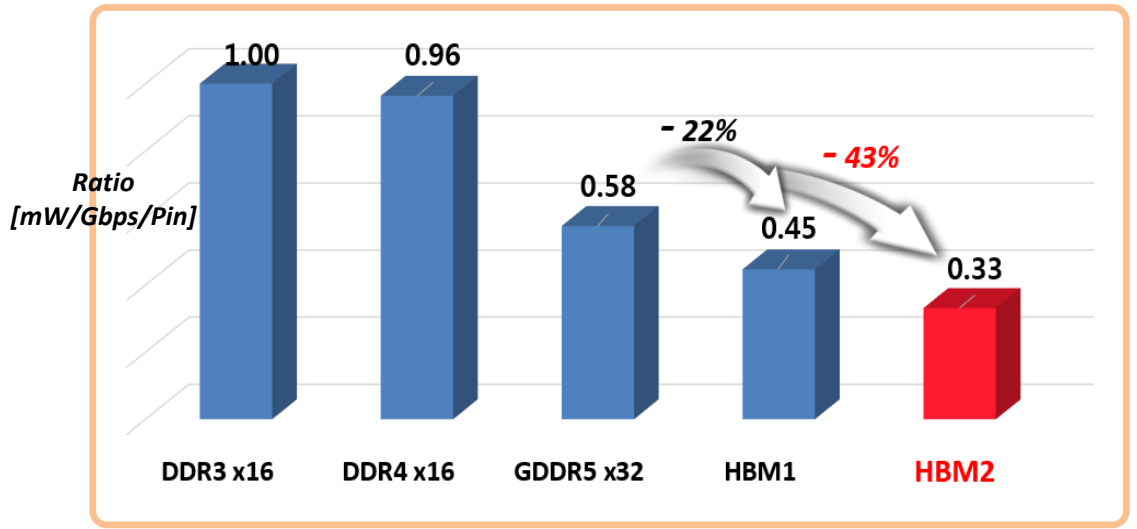
Note: this is an illustration of a design with 2 Channels per DRAM slice

HBM Advantages

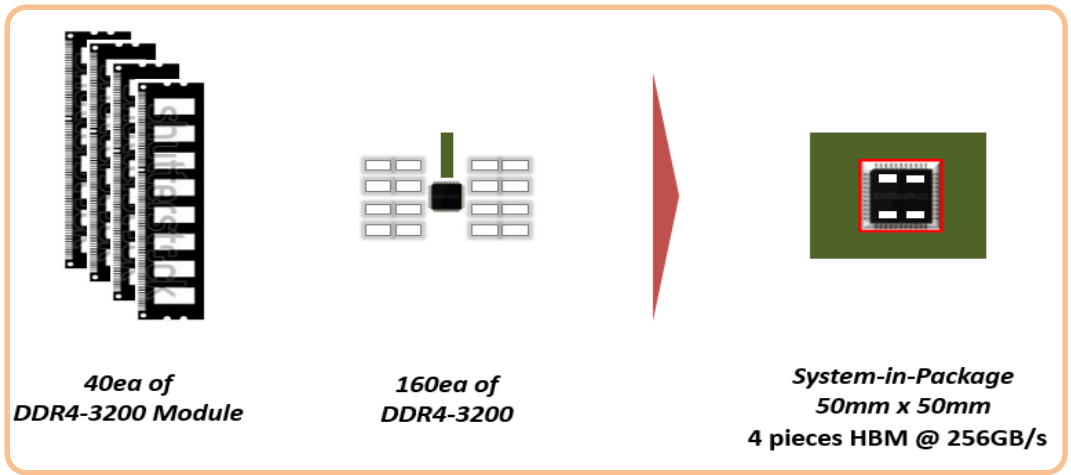
Bandwidth Per Chip



Power Efficiency @ IDD4R

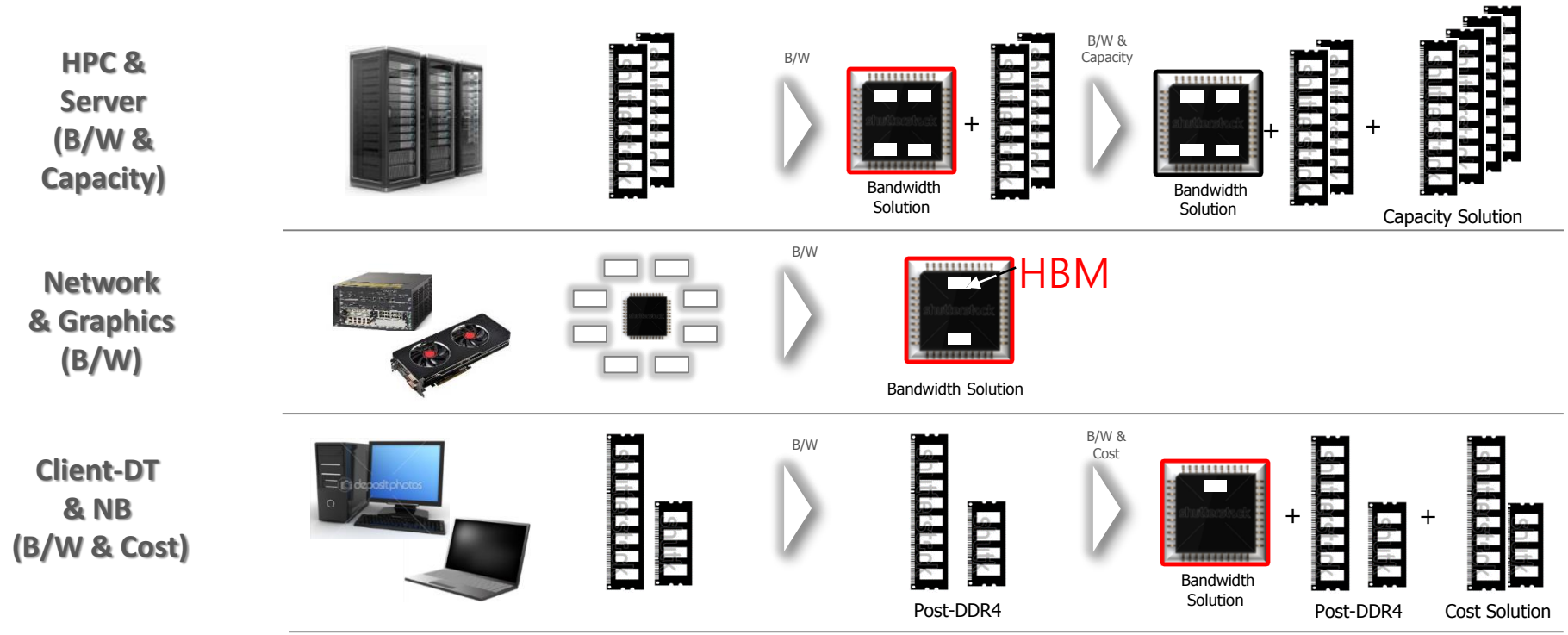


To Achieve 1TB Bandwidth .....



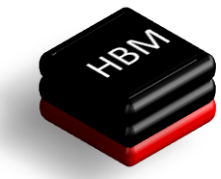
System & Memory Architecture

HBM is designed to address multiple needs of next generation systems



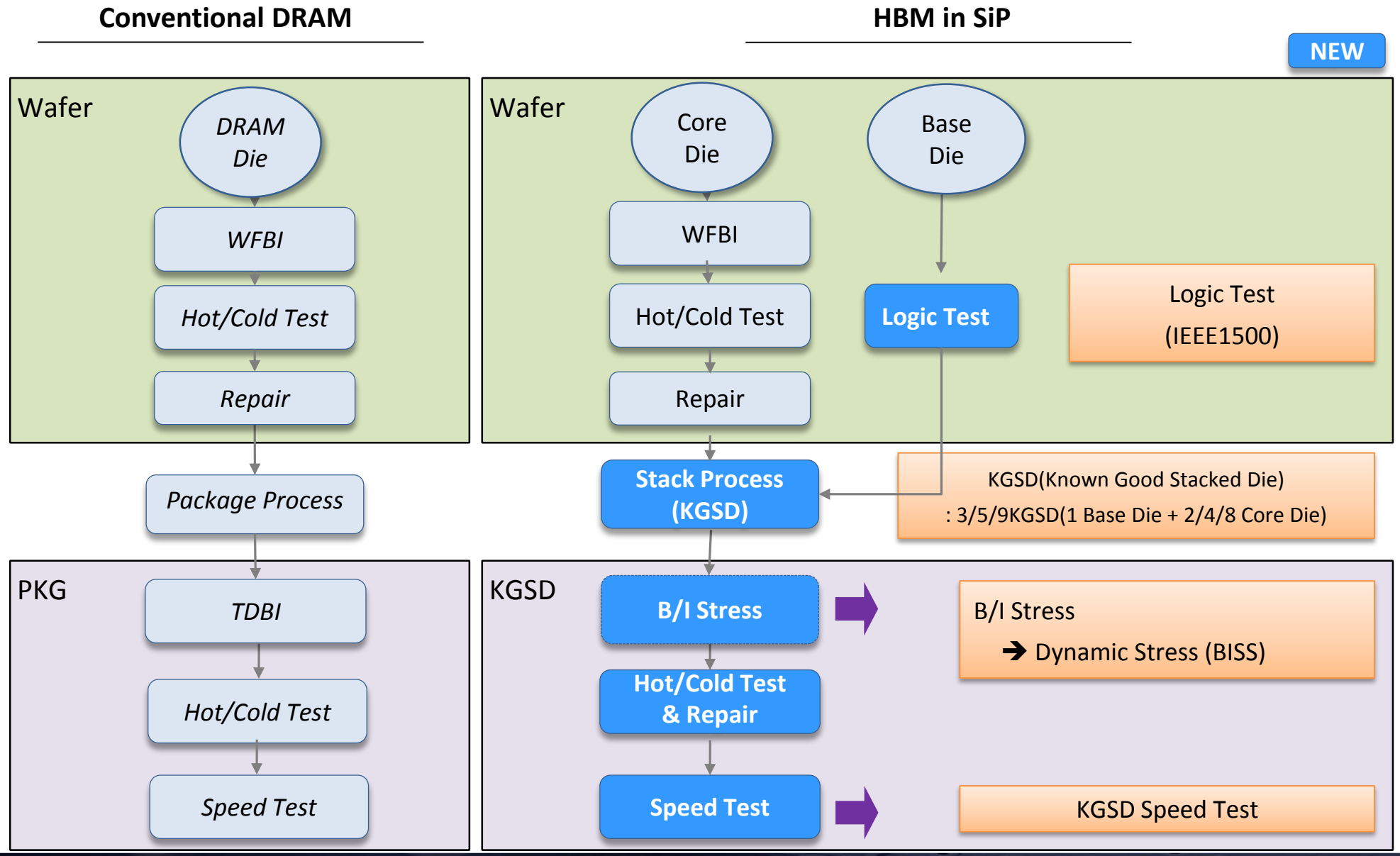
HBM Product Available

Different HBM2 line-ups available for different needs of various market segments

8Gb/4Gb based	9mKGSD(8 Hi)			5mKGSD(4 Hi)			3mKGSD(2 Hi)		
Density/Cube(GB)	8			4			2		
IO(DQ)	1024			1024			1024		
Speed/Pin(Gb/s)	1.0	1.6	2.0	1.0	1.6	2.0	1.0	1.6	2.0
Bandwidth(GB/s)	***128***	***204***	***256***	***128***	***204***	***256***	***128***	***204***	***256***
Usage	HPC, Server, Network			HPC, Server, Graphics, Network			Graphics, Cache		
Configuration									

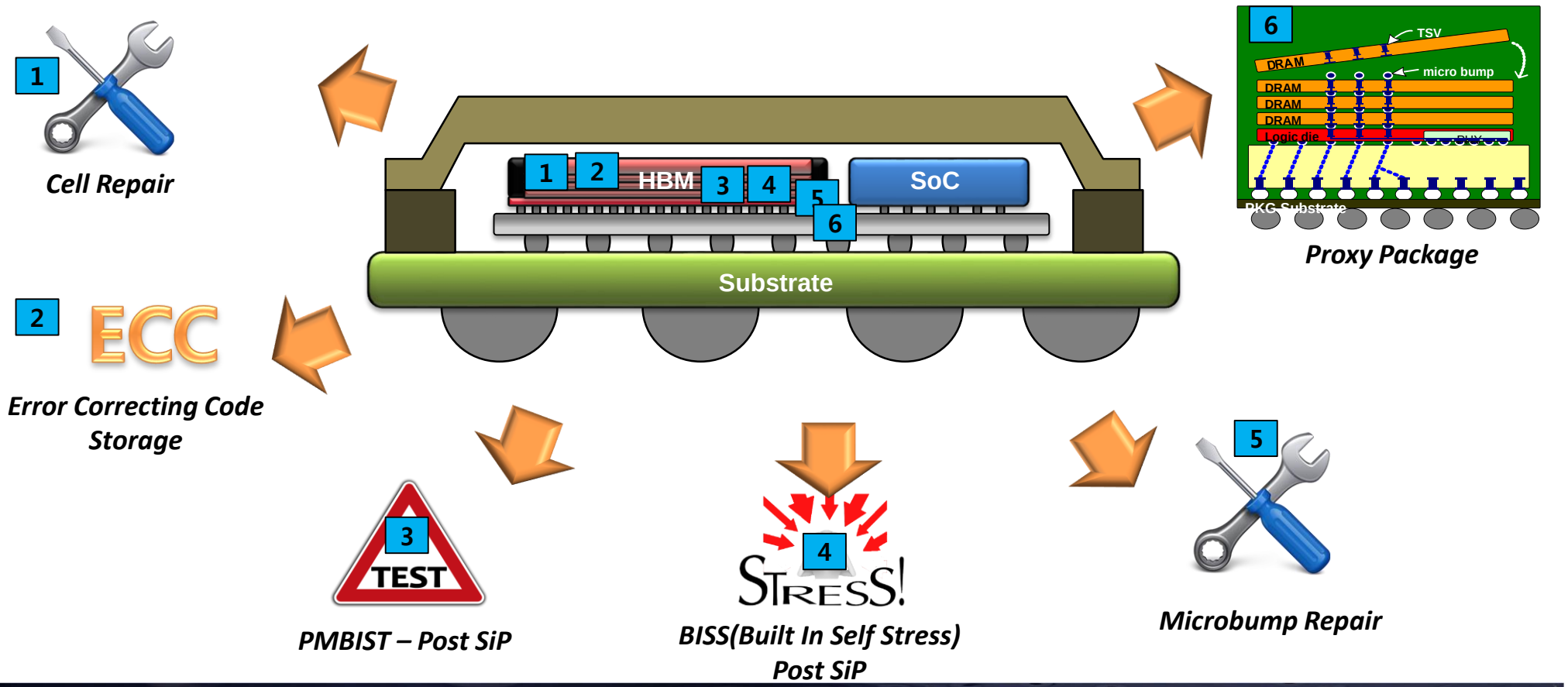
3. High Bandwidth Memory – Test/Quality/Reliability

HBM Test Flow



Quality and Reliability Features

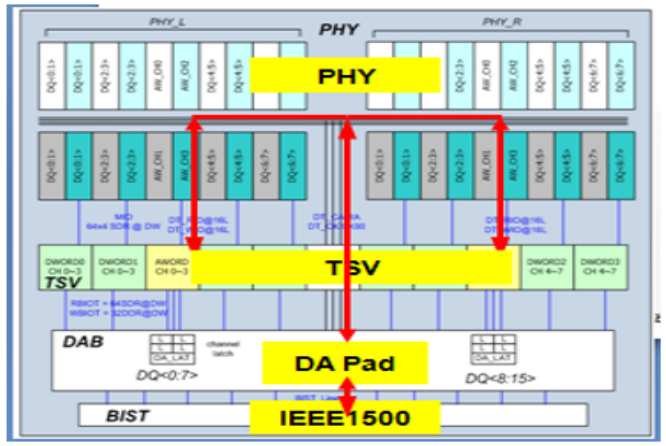
HBM features enable high quality and reliability at post 2.5D assembly



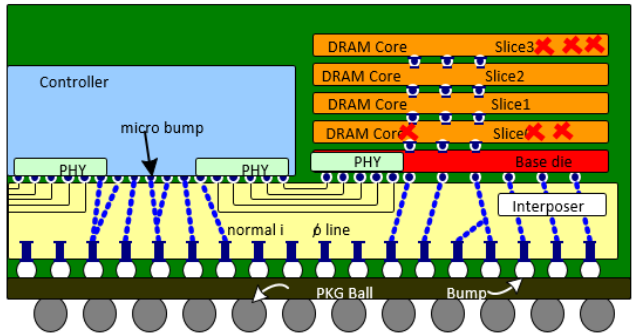
Post Package Repair – DRAM Cells & TSV/ubumps

HBM includes test/repair features for Post SiP assembly through IEEE1500 standards
HBM provides Soft & Hard Post Package Repair (PPR) functions

KGSD (Base/Core)

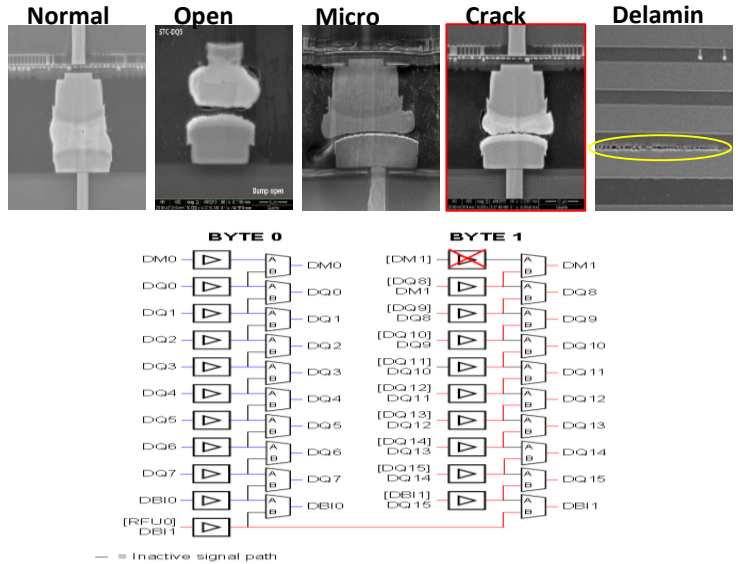


Test Area	Function	Detail item	Coverage
PHY	Function Test	RD/WT,CL,BL	100%
	Margin Test	Speed, VDD, Setup/Hold Timing	100%
TSV	Function Test	RD/WT,CL,BL,TSV interface	100%
	OS Check	TSV Open/Short Check	100%
Logic	Function Test	IEEE1500, Function, BIST, Repair	100%
	Margin Test	VDD, Speed, Setup/Hold	100%
Core	Function Test	RD/WT, Self Ref, Power Down	100%
	Margin Test	Speed, VDD, Async, Refresh	100%
	Repair	Cell Repair	100%



MBIST enable DRAM Cell Test and Repair through IEEE1500

- Conducted after SiP Assembly
- 4-Row Rep / 2-Bank (Repair DRAM)
- (64 row per channel @ 8Hi)
- Performed via MBIST

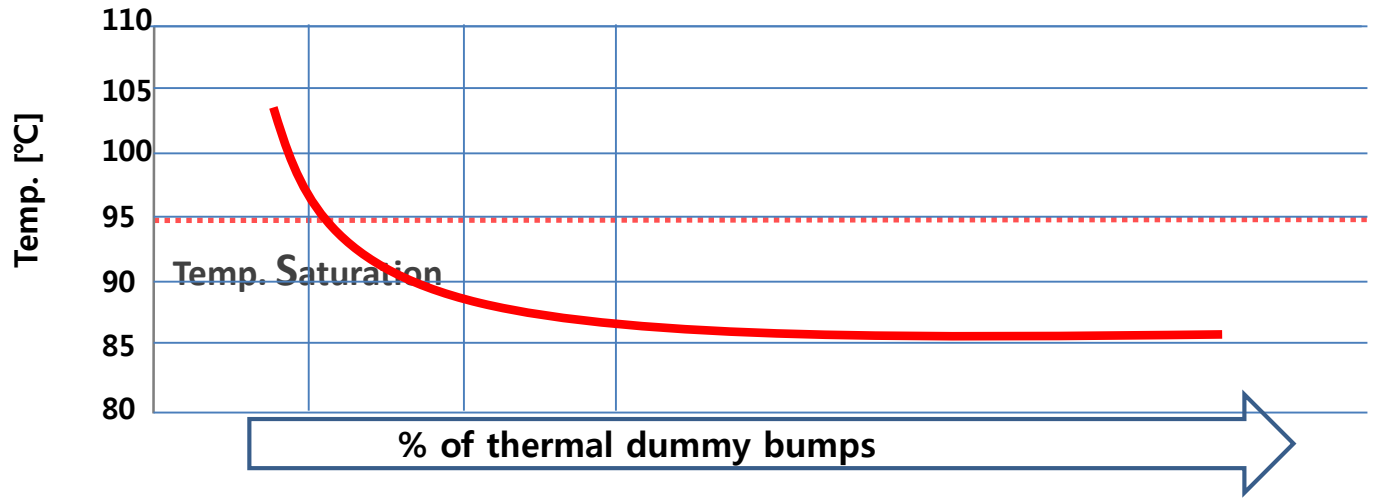


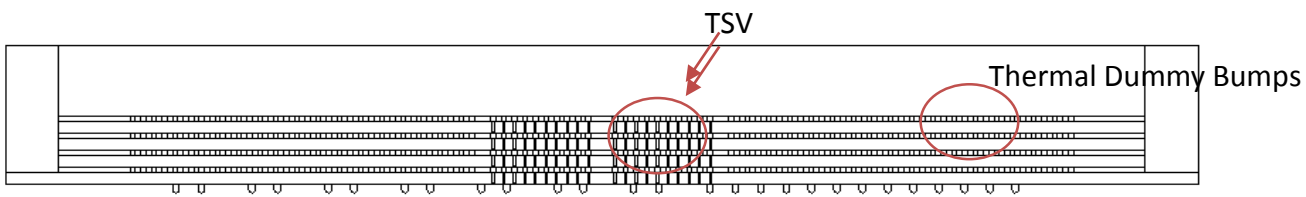
HBM supports interconnect lane remapping through IEEE1500 instructions

- Conducted after SiP Assembly
- Lane remapping is independent for each channel

HBM Thermal Management & Reliability

- Thermal dummy bumps enhance thermal dissipation
- There are no mechanical reliability issues by thermal dummy bumps





Collaterals Available from HBM Vendors

Item	Remarks
Functionality	Datasheet (Jedec / Vendor)
	Verilog (Mission mode & DFT)
	IBIS
	Hspice
Mechanical/Interposer Design	GDS
	Bump pad netlist
	Bump ballout
Thermal Simulation	Flotherm
	Icepak

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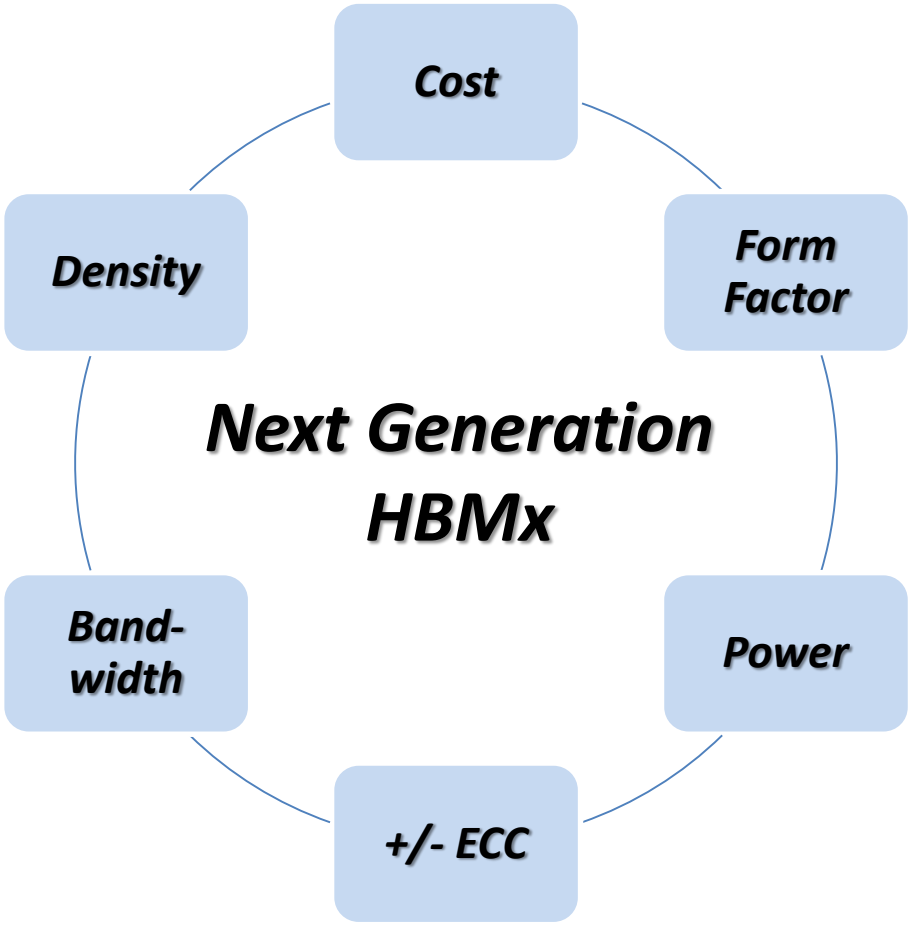
5. Future TSV based DRAM solutions

5. Next Generation TSV Solutions

Next generation HBMx will target multiple applications



Conclusion

- HBM is a breakthrough memory solution for performance, power and form-factor constrained systems by delivering high bandwidth, Low effective power & Small form factor
- HBM device provide various mechanisms to ensure quality/reliability at pre and post SiP assembly
- HBM is an industry standard solution with multiple supply sources

Thank You!