**Education**

**M.S** Electrical Engineering (Mixed Signal Circuit Design/Devices)

Arizona State University, Tempe AZ (2010 – May 2012)

**B.E** Electronics & Communications

PESIT, VTU University, Bangalore, India (2003 – 2007)

**Technical Skills**

Languages: Verilog, System Verilog, UVM, C, Pearl, Shell script, System Verilog Assertions, OVL Assertions, Tcl, Matlab, Verilog PLI, VHDL.

Tools: NCSim, Verdi, VCS/DVE, Virtuoso, Caliber, Silvaco(TCAD).

Interests: VLSI Design, Architecture, Circuit Design, Devices.

**Work Experience**

**Broadcom Corporation*,*** Bangalore, India, April 2015 – Present

Senior Staff (Design Verification Engineer).

**Wireless LAN Chips** – Contribution:

* MAC Verification at Chip and Block level:- Involved in some specific blocks verification and also data path verification from HOST to PHY.
* Hardware Accelerator Block. Started working on this block.

**Broadcom Corporation*,*** Irvine, CA, July 2012 – April 2015

Staff II (Design Verification Engineer).

**Touchscreen Controller –** Contribution:

* Projects: Kona, Citrine, Jasper, Hana, Viper, Racer.
* PSPI Verification.
* Brownout Verification.
* SPI UVC modification, base sequences and integration to chip level environment.
* Sleep State Machine Verification and Sleep/Wakeup scenarios at chip level.
* Touch Controller Micro-code to add features related to Pause and debug.
* UVM RAL Setup with AHB adapter, involved Perl scripting to generate proper register format.
* Timer, WDog, PWM, HSPI and Boot code/Reset Verification.
* Supported on verification of Scan Engine.
* RAM/Patch RAM verification with Power domains. SV Assertions were used to monitor switching of Power domains.

**Mobile Processor –** Contribution:

* Project: Malta
* Developed I2C Slave and SPI Master models.
* AXI and AHB bandwidth monitors along with register coverage.
* Responsible for RTL/TB releases to team, involved extensive debug.
* Multi-Core Testbench setup.
* Developed Perl Regression scripts to launch chip and block level regressions, consolidate results.
* Reset/POR Verification.
* GPIO/I2C/SPI/Event Logic between Cores Verification at Chip level.
* CPU Core Timers Verification in different modes of CPU operation.

**Broadcom Corporation*,*** Irvine, CA, May 2011 – Dec 2011

Intern (DV Team).

**Mobile Processor –** Contribution:

* Project: Capri
* Independently handled the testbench development to verify PLL’s debug bus mapping, connectivity, and status updates.
* Independently verified the connectivity of the SoC.
* Testbench development to check the functionality of LED Matrix.
* Analog blocks verification through AHB configurations.
* Verification of Audio block, SPI Interface, CIR verification through pre-developed testbench.
* JTAG check for oscillators, temperature monitors and PLLs.
* Developed Shell and Perl scripts to automate, create coverage reports, and monitoring of logs.

**Wipro Technologies**, India, Oct 2007 – March 2009

Project Engineer (Semiconductor division)

**Wireless LAN (802.11n) –** Contribution:

MAC Layer:

* Developed the PHY layer model using System Verilog, modeled the receive chain of the PHY layer.

PHY Layer:

* Involved in the Test bench Architecture design. As team of two developed the entire Test bench Architecture to verify the 802.11n MODEM.
* Developed modules for the Transmit chain Test bench: MAC Transmit model module, Data checker module, Timing Monitor, Matlab Interface module using PLI and AHB Interface using Verilog and C.
* Created Test plan for Legacy behavior of MODEM.
* Supported other team members in creating Test plan for Mixed mode and Green field behavior of MODEM.
* SV Assertions for MAC-PHY Interface protocol.

**Graduate Courses**

* VLSI Design
* Analog Integrated Circuits
* Semiconductor Device Theory 1
* Advance Analog Integrated Circuits
* Semiconductor Characterization
* Device oriented circuit design
* Advance VLSI Design
* Advance MOS
* Computer Architecture
* Design of Experiments

**Graduate Academic Projects**

Cache Design (Advance VLSI Design)

Designed (Schematic & Layout) 16 KB Level 1 cache in 45 nm technology with “Late way select architecture” and 4 entry TLB.

Design of PN diode to fit a particular IV curve (Independent Study)

A PN diode was designed to fit a particular IV curve by varying its doping and length, and model the PN diode with R and C value, which are close to the measured capacitance and resistance value of actual diode.

Advance Analog Integrated Circuits

1. Telescopic Cascode Amplifier
2. Folded Cascode Amplifier
3. Design of 50 ohm driver.

Eight-Band Audio Equalizer (VLSI Design)

Project deals with low-power circuit design of eight-band audio equalizer with layout. This project is implemented in 240 nm technology.

**Undergraduate Academic Project**

Simulation of WIMAX physical layer module

Project deals with the simulation of WIMAX physical layer module. The modulation scheme used is 64 QAM (Quadrature Amplitude Modulation) with OFDM (Orthogonal Frequency Division Multiplexing).Implemented completely in MATLAB and checked its consistency with real time audio input voice signal, and partly in MATLAB Simulink.