# A Semi –Analytical Model for III-V Semiconductor Quantum Well Field Effect Transistors

M.S. Rahman, M.S. Islam and A. Haque Department of EEE, East West University Aftabnagar, Dhaka-1212, Bangladesh

Abstract- Si MOS technology is reaching near the fundamental scaling limit. New materials are being explored to sustain the continual scaling of MOSFETs into the deca-nanometer regime or even lower. III-V semiconductor materials are potentially attractive as alternatives to Si.

In this paper we propose a semi-analytical model for the current-voltage characteristics of III-V semiconductor quantum well field-effect transistors (QWFET). The model calculates the quantized states in the well through numerical solution of one dimensional Schrodinger's equation. Channel carrier density and drain current as functions of gate and drain voltages are calculated analytically. It is expected that the model will be useful in qualitative studies of the device trends.

### I. INTRODUCTION

Silicon MOSFETs have dominated the integrated circuits industry for half a century through continual performance enhancement via scaling. As the physical scaling limit is reached, maintaining this trend has become very difficult [1-5]. New materials are being explored to continue the performance enhancement of MOSFETs. semiconductors are considered attractive alternatives due to their outstanding electron transport properties [3, 5-7]. High electron mobility transistors (HEMT) fabricated with III-V semiconductors are already in wide use [8]. Surface channel III-V semiconductor MOSFETs suffer performance degradation due to high density of interface states at oxidesemiconductor interface [9]. It has been proposed to mitigate this problem by using a quantum well channel which shifts the channel away from the interface. Analytical models of FETs are important to predict device behavior in circuits [10], but only a few analytical models have been developed for III-V semiconductor quantum well FETs (OWFETs).

In this work, a semi-analytical model for current-voltage characteristics is proposed for InGaAs QWFETs. Only the quantized energies in the quantum well channel are determined numerically from the solution of one dimensional Schrodinger's equation. The Channel charge densities and the currents are calculated analytically once the quantized energies are known.

## II. SEMI-ANALYTICAL MODEL

Figure 1 shows the schematic diagram of the device under our consideration. We have used  $In_{0.53}Ga_{0.47}As$  as the channel of the FET,  $In_{0.52}Al_{0.48}As$  as the barrier and InP as the

substrate. Al<sub>2</sub>O<sub>3</sub> is used as the oxide layer. Time independent one dimensional Schrodinger's equation (Eq. 1) is solved to determine the quantized energies of QWFET channel.

$$-\frac{\hbar^2}{2m}\frac{\partial^2 \psi(x)}{\partial x^2} + V(x)\psi(x) = E\psi(x) \tag{1}$$

To form the Hamiltonian matrix we have used the finite difference method. Conduction band diagram of the device is shown in Fig. 2. While calculating quantized energies we have considered the effective mass of InGaAs is  $0.045m_0$ , where  $m_0$  is the electron rest mass. Work function of InGaAs, InAlAs, InP and Al are respectively 4.5 eV, 4.095 eV, 4.35 eV and 4.25 eV.  $\ln_{0.53}$ Ga<sub>0.47</sub>As and  $\ln_{0.52}$ Al<sub>0.48</sub>As are assumed to be lattice matched to InP.

We have calculated two eigenenergies  $E_1$ =29.2 meV and  $E_2$ =111.1 meV with no applied gate voltage considering the well structure of Fig. 2. Figure 3 shows the lowest two wavefunctions along the channel width. Again Fig. 4 shows the lowest two wavefunctions along the channel width where two eigenenergies are  $E_1$ = - 930.03 meV and  $E_2$ = - 833.37 meV with 1 V bias applied between the gate and the substrate.

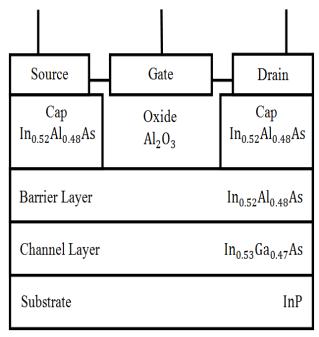


Fig. 1: The schematic diagram of the quantum well field effect transistor under consideration.

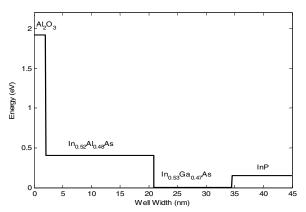


Fig. 2: Conduction band diagram of the device under consideration.

To verify the accuracy of our calculations, we have compared our result with those of [11] for a simple rectangular well with a 300 meV high barrier, 7.5 nm wide well and  $m^* = 0.067m_0$ . Figure 5 shows the wavefunctions of the lowest two energies. The lowest two eigenenergies are  $E_1$ =52.906 meV and  $E_2$ =200.595 meV which are very close to the values reported in [11] ( $E_1$ =53.474 meV and  $E_2$ =199.044 meV) for the same structure. Once we have calculated the eigenenergies we can find the carrier concentration ( $N_i$ ) associated with the ith quantized energy  $E_i$  using (Eq. 2) [12].

$$N_{i} = (n_{vi} m_{di} KT / \pi \hbar^{2}) F_{0} [(E_{f} - E_{i}) / KT]$$
 (2)

Where  $F_0(x) = ln(1 + e^x)$ ,  $m_{di}$  is the density-of-states effective mass in the *i*th valley,  $E_f$  is the Fermi energy,  $E_i$  is the eigen energy of subband *i*. The valley degeneracy,  $n_{vi} = 1$ . The total carrier concentration n is the sum of all  $N_i$  (Eq. 3).

$$n = \sum_{i=1}^{m} N_i \tag{3}$$

Using the carrier concentration we can find the drain current of the device using (Eq. 4) [13].

$$I_d = nev_d \tag{4}$$

Where,  $I_d$  is the drain current, n is the total electron (carrier) concentration, e is the electronic charge,  $v_d$  is the drift velocity. Again drift velocity  $v_d = \mu_d \in$ . Here  $\in$  is the electric field  $\in = V_{dd}/L$ ,  $V_{dd}$  is the drain voltage and L is the channel length. When calculating the relationship between  $V_{dd}$  and  $I_d$ , we assume that  $I_d$  will be saturated when  $V_{dd} \ge V_g - V_t$ .

## III. RESULTS

Figure 6 shows the carrier concentration for different energies and the total carrier concentration for the device shown in Fig. 1. Figure 7 shows the drain current as a function of the gate voltage showing the sub-threshold behavior of the drain current. We also can find the threshold voltage of device from the linear  $I_d - V_g$  characteristics as shown in Fig. 8,

which is 0.63 V for the device structure we have considered. Figure 9 shows the relationship between the drain voltage and the drain current.

It should be mentioned that various secondary and non-ideal effects are not considered in this intrinsic core model. If necessary, these may be included through an extrinsic module.

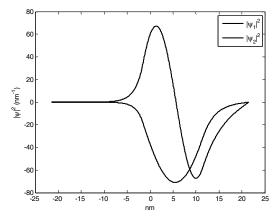


Fig. 3: Wave functions at the two eigenenergies for the quantum well shown in Fig. 2 with no applied gate voltage.

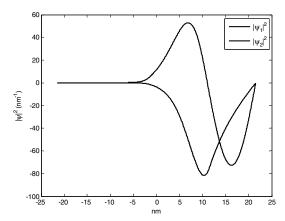


Fig. 4: Wave functions at the two eigenenergies for the quantum well shown in Fig. 2 with 1 V applied at the gate.

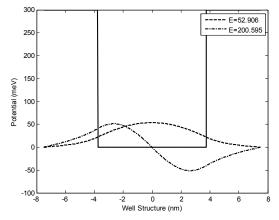


Fig. 5: Wave functions and the well structure for the comparison with results from [11].

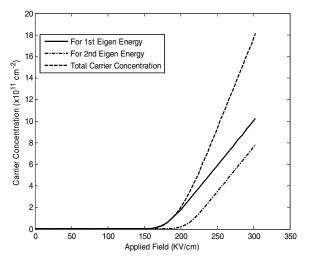


Fig. 6: Channel carrier concentrations as functions of the electric field along the gate direction.

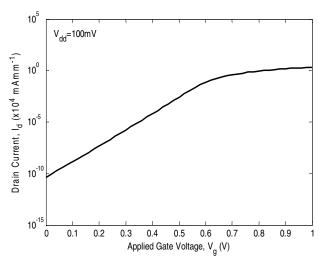


Fig. 7: Drain current as a function of the gate voltage showing sub-threshold behavior of the device.

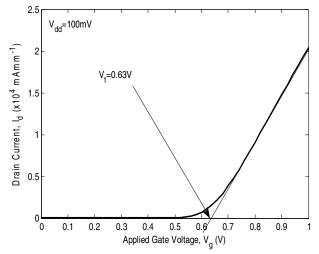


Fig. 8: Determination of the threshold voltage from the linear relationship between the drain current and the gate voltage. Here  $V_{dd} = 100 \text{ mV}$ .

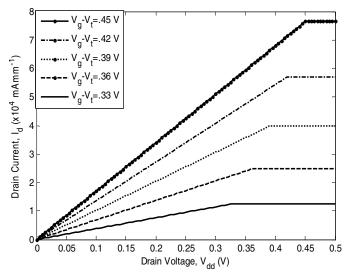


Fig. 9:  $I_d - V_{dd}$  relationship of the QWFET under consideration.

### IV. CONCLUSION

III-V semiconductor quantum well FET is an attractive candidate to replace the Si FET as the scaling limit is approached. We have presented a semi-analytical model for the current-voltage characteristics of a III-V semiconductor QWFET. Solutions to one dimensional Schrodinger's equation for quantized states in the channel are obtained numerically using the finite difference technique. The rest of the model is analytical. We have shown sample calculations of carrier concentration and current-voltage relationship of a typical device. This model is useful for qualitatively studying the device performance trends.

## REFERENCES

- H. .-P. S. Wong, "Beyond the convetional transistor," *IBM J. Res. & Dev.*, vol. 46, no. 2/3, pp. 133-168, Mar. 2002.
- [2] S. J. Wind, D. J. Frank, and H. .-S. Wong, "Scaling silicon MOS devices to their limits," *Micro. Eng.*, vol. 32, pp. 271-282, 1996.
- [3] J. A. del Alamo and D. .-H. Kim, "The prospects for 10 nm III-V CMOS," VLSI-TSA, pp. 166-167, Apr. 2010.
- [4] L. Wang, "Quantum mechanical effects on MOSFET scaling," PhD Thesis, Georgia Institute of Technology, 2006.
- [5] J. R. Chen Hu, "Device Technology for nanoscale III-V compound semiconductor field effect transistors," PhD Thesis, Stanford University, Stanford, 2011.
- [6] J. A. del Alamo, "III-V CMOS: What have we learned," CSW/IPRM, pp. 1-4, May 2011.
- [7] M. A. Khayer and R. K. Lake, "Modeling and Performance Analysis of III-V Nanowire Field-Effect Transistors," in *Nanowires Science and Technology*, N. Lupu, Ed. Croatia: INTECH, 2010, ch. 18, pp. 381-402.
- [8] N. Verma, M. Gupta, R. S. Gupta, and J. Jogi, "Quantum modeling of nanoscale symmetric double-gate InAlAs/InGaAs/InP HEMT," J. Semicon. Tech. & Sci., vol. 13, no. 4, pp. 342-354, Aug. 2013.
- [9] K. Raseong, T. Rakshit, R. Kotlyar, S. Hasan, and C. E. Weber, "Effects of surface orientation on the performance of idealized III–V thin-body ballistic n-MOSFETs," *IEEE Elec. Dev. Lett.*, vol. 32, no. 6, pp. 746-748, Jun. 2011.

- [10] R. Fernández-García, I. Gil, A. Boyer, S. BenDhia, and B. Vrignon, "A new approach to modelling the impact of EMI on MOSFET DC behaviour," *IEICE Trans. Elect.*, vol. E94-C, no. 12, pp. 1906-1908, Dec. 2011.
- [11] A. Haque and A. N. Khondker, "An Efficient Technique to Calculate the Normalized Wave Functions in Arbitary One-Dimensional Quantum Well Structures," *J. Appl. Phys*, vol. 84, no. 10, pp. 5802-5804, Nov. 1998
- [12] F. Stren, "Self-consistent results for n-type Si invertion layers," *Phys. Rev. B*, vol. 5, no. 12, pp. 4891-4899, Jun. 1972.
- [13] S. O. Kasap, *Principle of electronic materials and devices*, 3rd ed. New Delhi, India: Tata McGraw Hill, 2006.