Novel FinFET Domino Logic Circuit Using Dual Keepers

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***Abstract*—Extreme power density due to leakage currents and scaling of CMOS technology in the nanometer region using single gate MOSFET has become tentative. To alleviate this situation double gate devices like the FinFET can be used, which provide significantly lower leakage and considerably superior control over the current through it. In this paper we utilize the property of FinFET to switch dynamically between low and high threshold devices to design a novel domino logic style circuit configuration. Domino logic circuits are preferred for high speed operations but they suffer from considerable power loss. The proposed dual keeper domino logic circuit achieves the performance of traditional domino logic with significantly reduced power consumption and increased evaluation speed while maintaining similar input noise margin.**

Keywords— FinFET, Domino Logic, Independent Gate, Low Power, High Speed

I. INTRODUCTION

The cardinal barrier behind the advancement of the CMOS technology is scaling [1]. Channel length of MOSFET has been scaled from 10μm to 45nm over the past 40 years. This dramatic scaling of CMOS technology has led to a large increase in energy consumption for both active and idle states. Power consumption is now a challenging issue for battery lifetime in every portable device. Even in the case of non-portable device power consumption is also very important because of the increase in packaging density and cooling cost. The increased gate-dielectric and sub threshold leakage currents and enhanced device sensitivity to process parameter fluctuation have emerged as the chief obstacle against further CMOS technology scaling in the sub-45nm regime. It is important to develop efficient techniques to handle and reduce energy consumption while maintain other performance parameter such as delay, noise margin, etc. Fin type field effect transistor or FinFET [2] offer interesting power-delay tradeoff and better performance in the nanometer regime. Moreover the two gates of the FinFET can be used in novel circuit configurations to get optimum performance from a wide range of characteristics. The two gates of the FinFET can be shorted together to make the short gate (SG) mode which can be used in place of traditional CMOS transistor. On the other hand, the two gates can be used independently in the Independent Gate (IG) mode to get better control over the transistor current.

Domino logic circuit techniques are extensively applied in high-performance microprocessors due to the superior speed and area characteristics of dynamic CMOS circuits as compared to static CMOS circuits [1]. However they suffer from reliability problems due to the dynamic storage of charge. So, noise immunity vs. speed and power tradeoff need to be carefully observed. SG/IG- mode FinFET domino logic provides excellent power-delay characteristics. In the conventional domino logic gate, a feedback keeper is employed to maintain the state of the dynamic node against coupling noise, charge sharing, and sub-threshold leakage current. The keeper transistor is fully on at the starting of the evaluation phase. The keeper and the pull-down network transistors compete to determine the logical state of the dynamic node. This contention between the keeper and the pull-down network transistors degrades the circuit speed while increasing the power consumption [1, 3]. A standard domino logic circuit in SG-mode FinFET is shown in Fig. 1.

Domino logic using SG-mode FinFET has insignificant power-delay characteristic improvement in comparison to the conventional CMOS domino logic. The circuit suffers from inconsiderable evaluation delay and power dissipation. This problem is minimized by IG-mode domino logic [4] (Fig. 2) while circuit area and number of FinFET increase. The NAND gate itself consumes substantial power as well.

In this paper, we propose a novel domino logic circuit to reduce both power consumption and evaluation delay keeping noise margin in comparable range. The paper is organized as follows. Section II gives an overview of the FinFET technology. The standard domino logic circuit using SG FinFET is reviewed in Section III. Previously published some leakage control techniques are also discussed concisely in this Section. The operation of the proposed novel domino logic is explained in Section IV, while Section V shows the simulation results, followed by conclusion in Section VI.

II. THE FINFET TECHNOLOGY

Contrast to planar single and double gate devices, the FinFET effective channel width is perpendicular to the surface. That's why increasing of effective channel width and on current is possible by varying fin height. FinFET transistors overcome the static power dissipation problem by providing

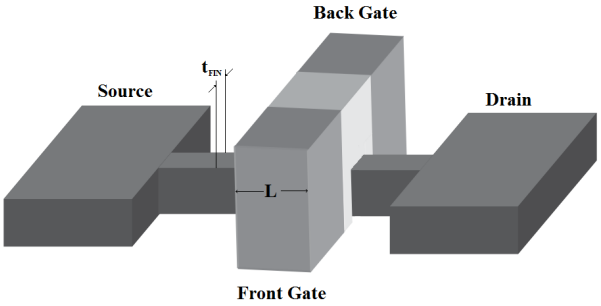

Fig. 1. Four Terminal FinFET Device [6].

effective control over the channel potential by using two gates wrapped around the fin [5]. A FinFET can be used to replace two parallel transistors with one if the gate signals of the two transistors are applied to it its two independent gates. This makes it useful for low power area efficient circuits. FinFET device parameters used throughout this paper are listed in T able I. For traditional bulk CMOS simulation, channel length of 32nm, channel width for the NMOS of 100nm and for 250nm for PMOS channel width was chosen. These parameters were selected to make the power and speed of CMOS comparable to the FinFET technology being used. Table I lists the parameters of the used FinFET model. At the sub-32nm technology, it is evaluated that leakage power might account for as much as 40-50% of total power consumption in CMOS technology [7]. This problem can be significantly mitigated by the use of FinFET. Independent control of front gate and back gate of FinFET can be effectively used to reduce power consumption and to improve circuit performance. FinFET also provides much less sub-threshold leakage.

III. Domino Logic Circuits

The standard domino logic [8] as shown in Fig. 2 consists of a pre-charge p-type transistor, M1 and a pull down network. The pre-charge transistor M1 charges a dynamic node during pre-charge stage when the clock signal at its gate is low. After this stage the clock returns to high and the evaluation period starts. At this time, the pre-charge transistor M1 is turned off and the foot transistor M4 is turned on. If the input of the circuit is such that the output must be low, then the pull down network turns on. This pulls the dynamic node to ground. If the output must be high however, the pull down network does not turn on and the dynamic node remains charged to a high voltage. This voltage is not stable as leakage current through the pull down network can cause the dynamic node to fall to low voltage. To prevent this, a keeper transistor M2 is employed with the dynamic node. This transistor turns on when the dynamic node is high and the pull down network is low, replenishing any charge lost due to leakage through the pull down network.

TABLE I. Device Parameters of the FinFET Model

Parameter	Value
Length of the channel (L)	32nm
Thickness of front gate/back gate oxide	1.4nm
Thickness of the fin (T_{FIN})	20nm
Height of the fin (h_{FIN})	15nm
Power supply (V_{dd})	0.9V
Channel Doping	$2\times10^{16}cm^{-3}$

One of the causes of power loss in the standard domino logic circuit is the momentary short circuit current when the pull down network turns on, and the clock signal has just been applied. At this time, the keeper is on, the pull down network is on as well and there is a momentary short circuit between the Vdd and the ground. Through proper choice of the keeper size, it is made sure that the dynamic node falls to a low voltage, which in turn turns off the keeper transistor, preventing any further power loss. However with the standard approach the momentary short circuit current cannot be completely prevented.

A proposed circuit utilizing independent gate FinFET as keeper [4] use delayed non-inverting clock signal to keep the keeper at a high threshold state to minimize this current (Fig. 3). This method utilizes an independent gate keeper. The delayed clock and the dynamic node are connected to the input of the NAND gate. The output of a NAND gate is connected to the back gate of the keeper transistor. The invert of the dynamic node, the output is connected to the front gate of the keeper M2 in a fashion similar to the standard domino logic circuit. During early phase of the evaluation stage, the output of the NAND gate is high, keeping the keeper at a high threshold state. If the pull down network is turned on, the high threshold keeper passes a relatively low amount of current preventing increased power loss. On the other hand if the pull

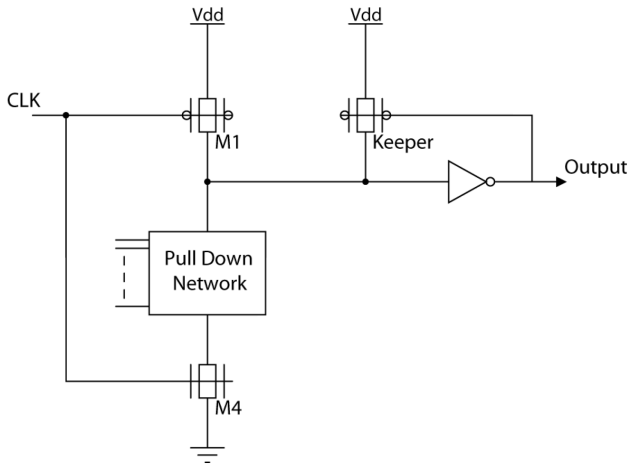

Fig. 2 Standard Domino Circuit using IG FinFETs

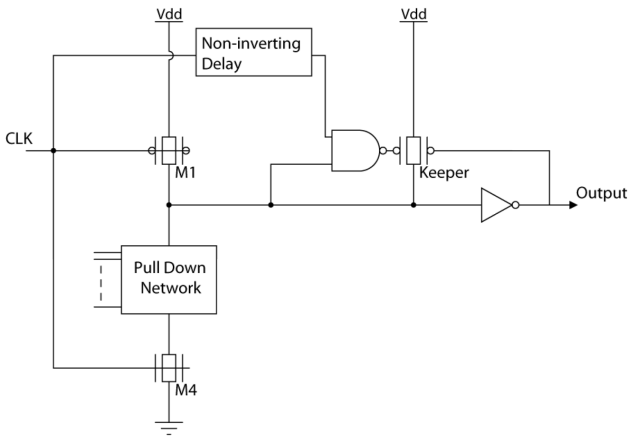

Fig. 3. FinFET Domino Logic using Independent Gate Keeprs

down network is not turned on, the high threshold keeper has insignificant adverse effect on the dynamic node's voltage. After the delayed clock signal reaches the keeper's back the keeper switches to a low threshold mode, enabling itself to pass high levels of current to sustain the dynamic node to a high enough voltage.

IV. Novel Domino Circuit using Dual Keepers

A novel circuit configuration is proposed in this paper to reduce the dynamic power consumption by reducing the aforementioned short circuit current in domino logic circuits using multiple independent gate FinFETs. This circuit is showed in Fig. 4. In this circuit two p-type FinFETs M2 and M3 are connected in series for the keeper action. A delayed inverting clock signal is connected to the top keeper M2's front gate. The output signal, obtained by inverting the dynamic node using a standard inverter is connected to the front gate of the other FinFET. The output is also connected to both the back gates of the FinFETs.

When the clock signal is low, the pre-charge FinFET M1 is on, the top keeper M2 is off and the foot transistor M4 is off as well. Since the output is low, M2 will be in a high threshold state. The dynamic node is charged to high voltage through the pre-charge transistor during this pre-charge stage. When the clock transits to high, the pre-charge transistor M1 is turned

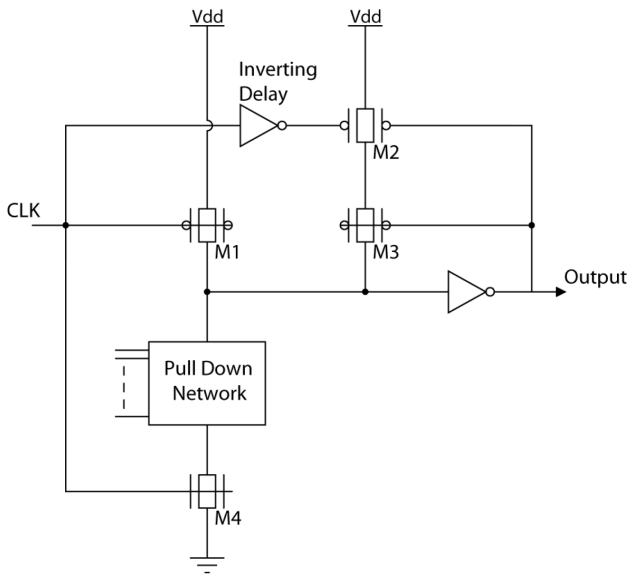

Fig. 4. Proposed Novel FinFET Domino Logic Circuit

off, and the foot transistor M4 turns on. The top keeper M2 remains off, however, until the clock transition can propagate through the delay. At this time, if the pull down network is on, the dynamic node can go to a lower voltage, without causing any Vdd ground short circuit current and turn the second keeper M3 off. This will cause M2 to alter itself to a high threshold state as well, making it faster and hence ready for future operations. When the clock transition reaches the top keeper through the delay, the top keeper can turn on without causing any effect of the dynamic node. If pull down network is off however, and the dynamic node was supposed to stay at a high voltage, the novel keeper configuration will not have any serious adverse effects of the performance as both the transistors M2 and M3 will turn on in time and keep the dynamic node charged to the proper high voltage

V. Simulation and Results

In this section, the simulation results for dynamic power, noise margin level and delay is presented for the novel circuit as well as standard domino logic circuit with respect to various keeper sizes. The simulation was done on Synopsys HSPICE [9] using Arizona State University Predictive Technologies Model (ASU-PTM) Double Gate model [10]. The model parameters used in the simulation is given in Table I. The effective width per fin of the device was calculated from the fin width and fin height using the following equation [11]:

$$W_{eff} \cong 2 \times h_{FIN} + W_{FIN} \quad (1)$$

The aforementioned circuit was loaded with fan out of four inverters to simulate heavy load. For dynamic power calculation, transient analysis was made with uniformly distributed input vectors and clock applied at 50MHz. The propagation delay was calculated from transient analysis of the circuits. Various voltage values were applied at one input after pre-charging the dynamic node and the minimum voltage required to bring the voltage of the dynamic node to ninety percent of supply voltage was noted as the input noise margin. From the simulation results it is apparent that the novel circuit configuration utilizing two p-type transistors as keepers performs better in terms of power consumption, delay in most cases, and input noise margin for similar sized keeper.

Fig. 5, 7 and 8 show the simulation results for dynamic power dissipation, propagation delay and input noise margin for the circuits under investigation. Dynamic power dissipation, delay, and input noise margins are also summarized if Table II, Table III and Table IV, respectively.

TABLE I. Dynamic Power (μW) of the Circuits

Circuit	Keeper Width/pull down transistor width				
	0.125	***0.25***	***0.5***	***1.0***	***2.0***
Independent Gate Keepers	9.35	8.05	9.28	9.15	9.49
Standard Domino	7.92	8.29	7.83	8.05	8.95
Novel Dual-Keepers	7.75	7.16	7.4	7.48	7.68

TABLE II. DELLAY (PICOSECOND) OF THE CIRCUITS

Circuit	Keeper Width/pull down transistor width				
	0.125	***0.25***	***0.5***	***1.0***	***2.0***
Independent Gate Keepers	63.3	66.2	67.7	75.1	76.2
Standard Domino	68.5	64	68.8	70.1	76
Novel Dual-Keepers	68.6	66.5	66.4	64.1	61.8

TABLE III. INPUT NOISE MARGIN (MILI VOLT) OF THE CIRCUITS

Circuit	Keeper Width/pull down transistor width				
	0.125	***0.25***	***0.5***	***1.0***	***2.0***
Independent Gate Keepers	85	100	118	145	85
Standard Domino	80	120	145	180	80
Novel Dual-Keepers	82	120	145	180	82

VI. CONCLUSIONS

In this paper, we have shown the design and simulation of a novel domino logic style circuit using independent gate FinFETs. The back gates of the FinFETs were used to control the threshold voltage of the front gate. This ability to control the threshold voltage of the front gate dynamically provides the design opportunity to construct digital circuits in various modes to optimize for leakage, power, area or delay according to the needs. From the simulation results it was evident that the proposed novel dual keeper domino logic circuit performs better than the standard domino logic circuit in terms of dynamic power, delay in most cases, and input noise margin.

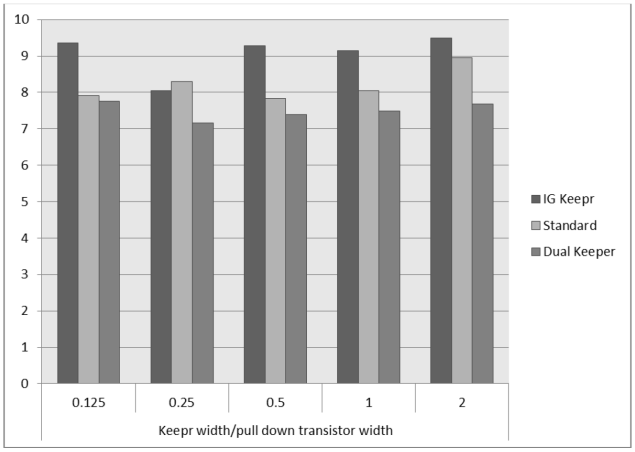

Fig. 5. Dynamic Power (μW) of the Circuits

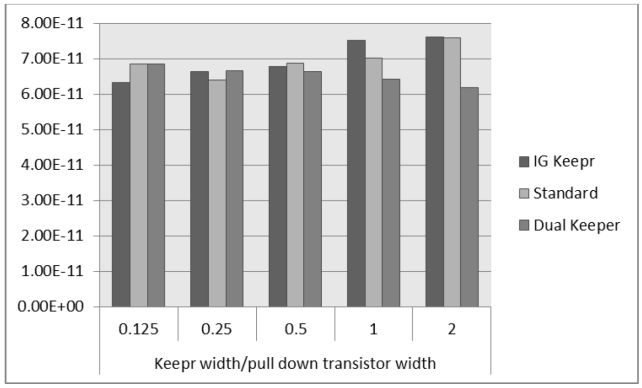

Fig. 6. Delay (seconds) of the Circuits

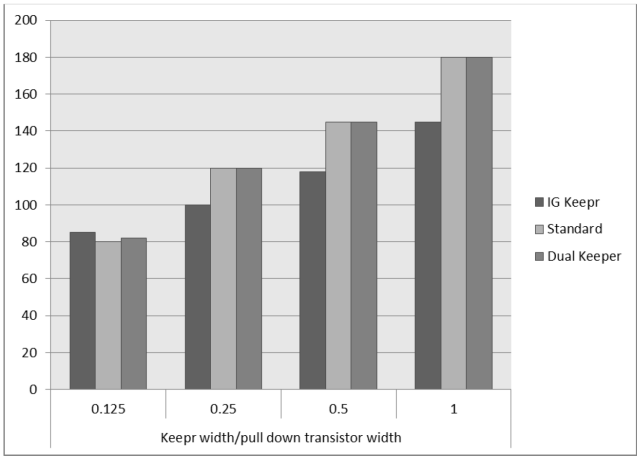

Fig. 7. Input Noise Margin (mV) for the Circuits

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