Ĉuk Topology Based Power Factor Correction and Output Voltage Regulation of AC-DC Converter

Md. Ismail Hossain[*1] and Dr. Mohammad Jahangir Alam[*2]
[*]Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology
[1]jewel04eee@yahoo.com
[2]mjalam@eee.buet.ac.bd

***Abstract*—This paper focuses on the analysis of a power factor correction (PFC) converter using close loop Ĉuk topology. Regardless of the input line voltage and output load variations, input current drawn by the buck or buck-boost converter is always discontinuous. The Boost converter suffers from high voltage stresses across the power electronic devices. The input current in Ĉuk converter is comparable to boost converter's input current. In this paper output voltage is controlled by inner current and outer voltage control loop along with power factor correction (PFC). It shows less input current THD (less than 5%), nearly unity power factor and better output voltage regulation of AC-DC converter under variable input voltage and output load. Small signal model analysis is presented for obtaining frequency response of the control loop. The MATLAB Simulink programming environment is used as a simulation tool.**

Keywords*—State space averaging technique, small signal ac model, PWM technique, average current control etc.

I. INTRODUCTION

Uses of Computer and telecommunications equipment have become important in our society. Electric vehicle is rapidly increasing in use due to its environment friendly technology. DC power supply is the heart of these devices and most of the case it comes from AC-DC converter. The efficiency, total harmonic distortion of input current, input power factor and regulated output voltage etc are the main concern of these AC-DC converters.

Uncontrolled diode rectifiers followed by L-C smoothing filters are widely used as a cheap power supply. Un-controlled charging of DC filter capacitor results in 50Hz pulsed ac current waveform at the input of the rectifier. Several power quality problems arise at the source side, which includes poor power factor, high input current total harmonic distortion (THD), failure of transformers due to overheating and harmonic pollution on grid [1-2] etc. Grid disturbances may result in malfunction or damage of electrical devices. Many methods for elimination of harmonic pollution in the power system are in use and new methods are being investigated. Restrictions on current and voltage harmonics are maintained in many countries through IEEE 519-1992 and IEC 61000-3-2/IEC 61000-3-4[3] standards. The restrictions are associated with the idea of "clean power". The power factor correction (PFC) converter topology using active wave shaping techniques can overcome the problem in line current. The PFC Converter forces the line to draw near sinusoidal AC current in phase with its voltage. Most of the single phase AC to DC conversion PFC works are done with Buck, Boost, and buck-boost or fly-back topology between the source and the load. Buck and buck-boost topology suffer from input discontinuous current [4-7] and Boost topology needs large value capacitance [8] to minimize the output voltage ripple therefore initial inrush current is higher than Ĉuk converter [9-10]. Ĉuk converter requires low value intermediate capacitance to transfer energy to output capacitance and load [9-10].

In this paper output voltage and input current control variable duty cycle Ĉuk converter has been proposed for minimizing output voltage variation due to line voltage and load variation and obtaining sinusoidal AC mains current. Fixed frequency is chosen due to easier parameter design comparable to hysteresis control.

II. PROPOSED CLOSE LOOP ĈUK REGULATOR BASED AC-DC CONVERTER

Proposed close loop Ĉuk regulator based AC-DC converter is shown in Fig. 1. The technique used here is the Average Current Mode control. In Average Current Mode control, the output voltage is controlled by varying the average value of the current signal. The Voltage feed forward compensator controls the input voltage variation in such way that if the input voltage reduces then the output of Voltage feed forward compensator increases and vice versa. The actual output DC voltage is sensed and compared with a reference voltage then the voltage error is processed through the proportional integral controller. The output of the proportional integral controller is multiplied with the rectified input voltage and output of voltage feed forward compensator to make a reference current in phase with rectified input voltage. The real current is forced to track the reference current through current error compensator. The error between the actual current and reference current is processed through the proportional integral controller and then its output is compared with the Saw-tooth wave to generate the required PWM signal.

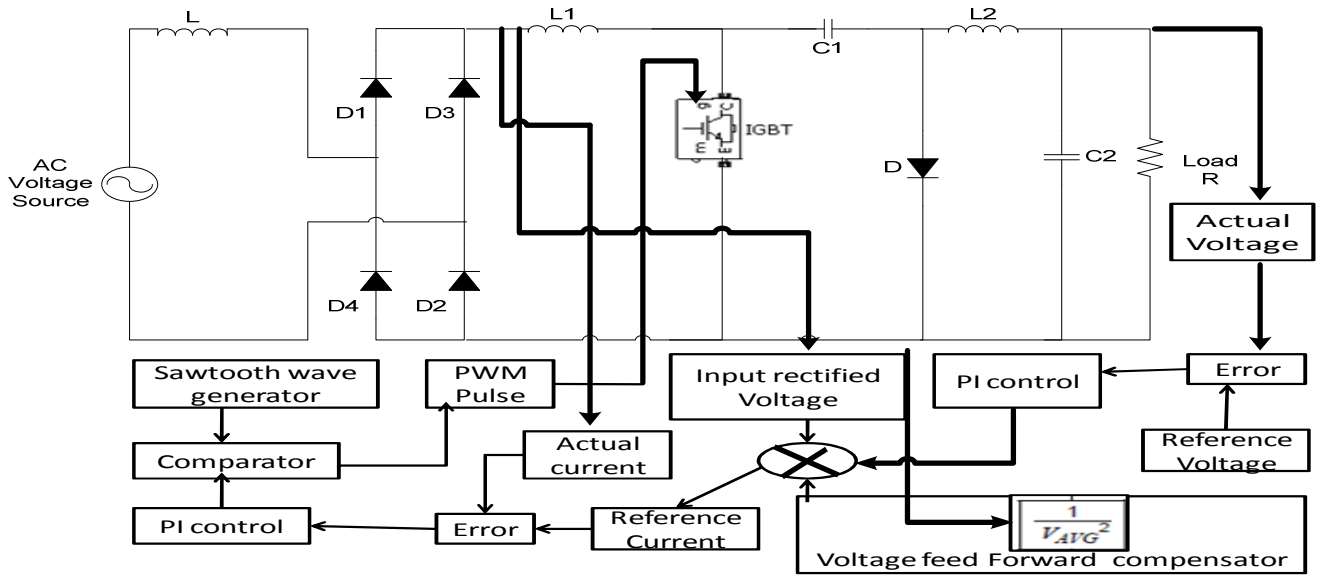


Fig. 1. Proposed close loop Ĉuk regulator based AC-DC converter.

III. CLOSE LOOP RESPONSE ANALYSIS OF AC–DC ĈUK CONVERTER USING STATE SPACE AVERAGING TECHNIQUE

For analysis the stability of the proposed control system using bode plot open loop transfer function is needed. For continuous conduction mode (CCM), dc-dc converters operate in two circuit states in one switching period, (i) when switch is on for a time interval dT and (ii) when switch is off for a time interval (1-d) T, where d is a duty cycle and T is switching period. According to Leverrier's Algorithm modeling of dc-dc converters using SSA method needs three steps in general as discussed below.

a. During each circuit state, the linear circuit is Described by the state variable vector x.
Generally inductor currents and Capacitor voltages are chosen as state variables. The state space equations of two circuit states, in standard form, are obtained as
When switch is on during time interval dT, state-space equations of converter can be written as

$$\frac{dx(t)}{dt} = A_1x(t) + B_1u(t) \quad \text{and}$$
$$y(t) = C_1x(t) + E_1u(t) \quad \text{.....(1)}$$

The matrices A_1, B_1, C_1 and E_1 describe the network connections during the time interval dT. x(t), u(t) and y(t) are the state variable, input variable and output variable respectively.
When switch is off during time interval (1-d)T, state-space equations of converter can be written as

$$\frac{dx(t)}{dt} = A_2x(t) + B_2u(t) \text{ and}$$
$$y(t) = C_2x(t) + E_2u(t) \text{.....(2)}$$

The matrices A_2, B_2, C_2 and E_2 describe the network connections during the time interval (1-d)T.
Equation (1) and (2) are time weighted and averaged over one switching period as

$$\frac{dx(t)}{dt} = A_{12}x(t) + B_{12}u(t) \text{ and}$$

$$y(t) = C_{12}x(t) + E_{12}u(t) \text{.....(3)}$$
Where
$A_{12} = A_1d + A_2(1-d)$, $B_{12} = B_1d + B_2(1-d)$
$C_{12} = C_1d + C_2(1-d)$, $E_{12} = E_1d + E_2(1-d)$

b. Now Linearization by introducing small ac perturbation around a DC operating point. To obtain a small signal ac model around a quiescent operating point, the following small perturbation as shown in equation (4) is added to state space model represented by equation (3)

$$x(t) = X + \tilde{x}(t),\ y(t) = Y + \tilde{y}(t)$$
$$u(t) = U + \tilde{u}(t)\ ,\ d(t) = D + \tilde{d}(t) \text{.....(4)}$$

The capital letter represents a DC value. Small signal linearization is justified under the following condition

$$X > \tilde{x}(t),\ Y > \tilde{y}(t), U > \tilde{u}(t) \text{ and } D > \tilde{d}(t)$$

Now replacing equation (3) in equation (4) we can get small signal state space model as

$$\frac{d\tilde{x}(t)}{dt} = A\tilde{x}(t) + B\tilde{u}(t) + B_d\tilde{d}(t)$$
$$\tilde{y}(t) = C\tilde{x}(t) + E\tilde{u}(t) + E_d\tilde{d}(t) \text{ .....(5)}$$
Where
$A = A_1D + A_2(1-D)$, $B = B_1D + B_2(1-D)$
$C = C_1D + C_2(1-D)$, $E = E_1D + E_2(1-D)$
$B_d = [(A_1 - A_2)X + (B_1 - B_2)U]$
$E_d = [(C_1 - C_2)X + (E_1 - E_2)U]$

Taking Laplace transform of equation (5) we have

$$\tilde{X}(s) = (sI - A)^{-1}[B\tilde{u}(s) + B_d\tilde{d}(s)] \text{ .....(6)}$$
$$\tilde{Y}(s) =$$
$$C(sI - A)^{-1}\left[B\tilde{u}(s) + B_d\tilde{d}(s)\right] + E\tilde{u}(s) + E_d\tilde{d}(s) \text{ ..... (7)}$$

Using equation (6) and (7) for DC value of input voltage $V_{IN,}$ output Voltage V_O and duty Cycle D, the control-to-output and the input-to-output small signal transfer functions of the converter are respectively given as

$$\frac{\widetilde{V_O}(s)}{\tilde{d}(s)} = C(sI - A)^{-1}B_d + E_d \quad \text{.....(8)}$$

$$\frac{\widetilde{V_O}(s)}{\widetilde{V_{IN}}(s)} = C(sI - A)^{-1}B + E \text{.....(9)}$$

Now for Ĉuk converter in Fig. 2 the parameter $A_{1,}$ $B_{1,}$ C_1 and E_1 is derived by the following way

When switch is on for dT time then from Fig. 2(a) we have

$$\frac{diL1}{dt} = \frac{V_{rect_{average}}}{L1}, \quad \frac{diL2}{dt} = \frac{VC1-VC2}{L2}$$

$$\frac{dVC1}{dt} = \frac{-iL2}{C1}, \quad \frac{dVC2}{dt} = \frac{iL2-\frac{VC2}{R}}{C2}$$

$$V_{\_out} = -VC2 \text{ ....(10)}$$

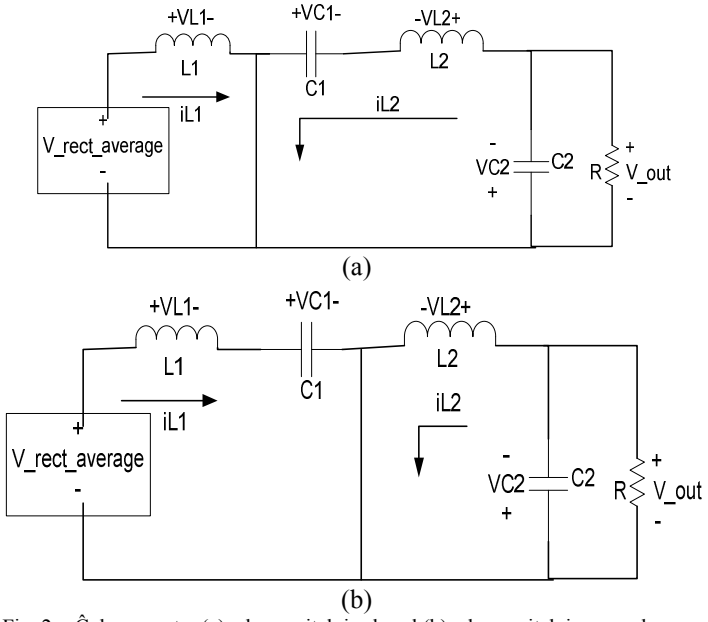


Fig. 2. Ĉuk converter (a) when switch is closed (b) when switch is opened

When switch is off for (1-d)T time then from Fig. 2(b) we have

$$\frac{diL1}{dt} = \frac{-VC1+V_{rect\_average}}{L1}$$

$$\frac{diL2}{dt} = \frac{-VC2}{L2}, \quad \frac{dVC1}{dt} = \frac{iL1}{C1}$$

$$\frac{dVC2}{dt} = \frac{iL2-\frac{VC2}{R}}{C2}$$

$$V_{\_out} = -VC2 \text{ .....(11)}$$

Therefore

$$A_1 = \begin{vmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L2} & \frac{-1}{L2} \\ 0 & \frac{-1}{C1} & 0 & 0 \\ 0 & \frac{1}{C2} & 0 & \frac{-1}{RC2} \end{vmatrix}, \quad B_1 = \begin{vmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \end{vmatrix},$$

$$C_1 = |0 \quad 0 \quad 0 \quad -1| \text{ and } E_1 = [0] \text{ .....(12)}$$

$$A_2 = \begin{vmatrix} 0 & 0 & \frac{-1}{L1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L2} \\ \frac{1}{C1} & 0 & 0 & 0 \\ 0 & \frac{1}{C2} & 0 & \frac{-1}{RC2} \end{vmatrix}, \quad B_2 = \begin{vmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \end{vmatrix},$$

$$C_2 = |0 \quad 0 \quad 0 \quad -1| \text{ and } E_2 = [0] \text{ ....(13)}$$

So using the state space Averaging method we have

$$A = \begin{vmatrix} 0 & 0 & \frac{-D/}{L1} & 0 \\ 0 & 0 & \frac{D}{L2} & \frac{-1}{L2} \\ \frac{D/}{C1} & \frac{-D}{C1} & 0 & 0 \\ 0 & \frac{1}{C2} & 0 & \frac{-1}{RC2} \end{vmatrix}, B = \begin{vmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \end{vmatrix},$$

$$C = |0 \quad 0 \quad 0 \quad -1|, \; E = [0]$$

$$B_d = \begin{vmatrix} \frac{V\_rect\_average}{D/L1} \\ \frac{V\_rect\_average}{D/L2} \\ \frac{-V\_rect\_averageD}{RC1D/^2} \\ 0 \end{vmatrix} \text{ and } E_d = [0] \text{....(14)}$$

IV. STABILITY ANALYSIS OF THE CONTROLLER USING BODE PLOT

The main objective of the control system is to draw a sinusoidal current, in phase with the input voltage. The reference inductor current $i_L^*(t)$ as shown in Fig. 3 is of the full wave rectified form. The requirements on the form and the amplitude of the inductor current lead to two control loops as shown in Figure 3 to pulse width modulate the switch of the Ĉuk converter. The inner current loop ensures the form of $i_L^*(t)$ based on the input voltage. The outer voltage loop determines the amplitude $\grave{I}_L^*$ of $i_L^*(t)$ based on the output voltage feedback. If the inductor current is insufficient for a given load supplied by the control system, the output voltage will drop below its pre-selected reference valueV_d^*. By measuring the output voltage and using it as the feedback signal the voltage loop adjust the inductor current amplitude to bring the output voltage to its reference value. In addition to determining the inductor current amplitude, this voltage feedback control acts to regulate the output voltage to the preselected dc voltage. In order to follow the reference with as little THD as possible, an average current mode control is used with a high bandwidth, where the error between the reference $i_L^*(t)$ and the measured inductor current $i_L(t)$ is amplified by a current controller to produce the control voltage $v_c(t)$ and finally gives PWM signal. The current control loop and voltage control loop are shown in Fig. 4 and Fig. 5 respectively.

The open loop transfer function of the current loop is

$$T_{I(s)} = H1(s)H2(s)H3(s) \text{ ..... (15)}$$

Where, $H1(s) = K_{pI} + \frac{K_{iI}}{S}$ and $H2(s) = \frac{1}{V_r}$

$$\text{H3(s)} = \frac{2.121\times10^{-12}S^3 - 8.094\times10^{7}S^2 + 2.576\times10^{12}S - 2.76\times10^{16}}{S^4 + 1.667S^3 + 9.849\times10^{8}S^2 + 1.641\times10^{9}S + 1.55\times10^{13}}$$

The open loop transfer function of the voltage loop is

$$T_{V(s)} = H4(s)H5(s)H6(s) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (16)$$

Where $H4(s) = K_{pV} + \frac{K_{iV}}{S}$, $H5(s) = 1$

$$H6(s) = \frac{\begin{array}{c}2.196 \times 10^{-12}S^7 - 2.961 \times 10^{7}S^6 - 2.965 \\ \times 10^{12}S^5 - 2.192 \times 10^{17}S^4 - 2.471 \times 10^{22}S^3 \\ +2.3 \times 10^{26}S^2 + 3.997 \times 10^{25}S + 3.198 \times 10^{30}\end{array}}{\begin{array}{c}2.221 \times 10^{4}S^7 + 1.073 \times 10^{9}S^6 + 2.71 \times 10^{14}S^5 \\ +8.943 \times 10^{18}S^4 + 7.154 \times 10^{23}S^3 \\ +3.7 \times 10^{24}S^2 + 9.947 \times 10^{27}S + 3.314 \times 10^{28}\end{array}}$$

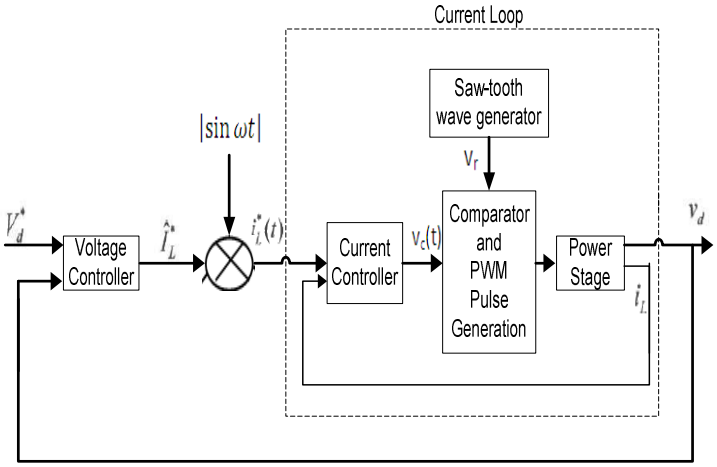
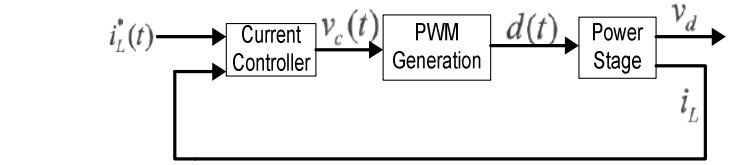


Fig. 3. **C**ontrol loop of the proposed control system.



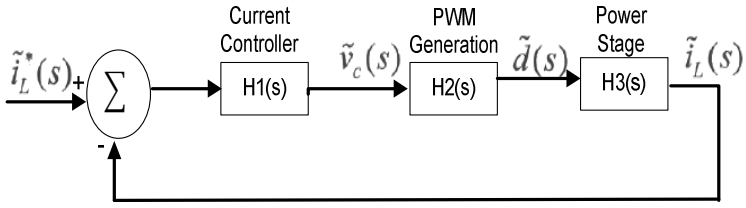


Fig. 4. **C**urrent loop of the control system

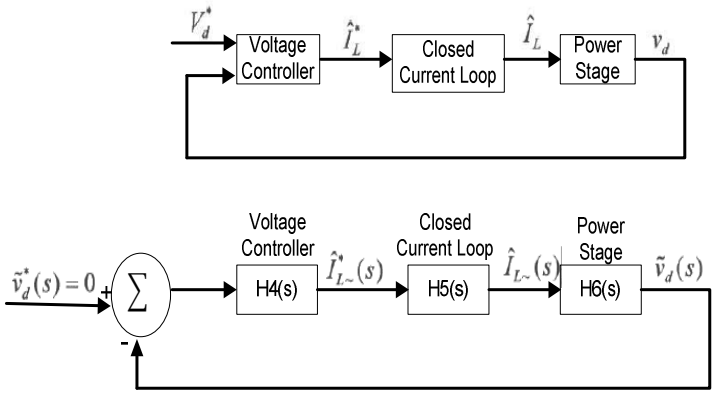


Fig. 5. Voltage loop of the control system

V. SIMULATION IN MATLAB SIMULINK

L= 100uH, L1= 10mH, L2=5mH, C1=0.1uF, C2=1500uF and switching frequency = 80000Hz are used for simulation.

For voltage loop K_p = 27 and K_i = 0.1 and for current loop K_p = 0.2 and K_i = 0.4 are used. Fig. 6 shows the bode plot of transfer function $T_V(s)$ and $T_I(s)$. Fig. 7 to Fig. 10 show the reference /real current, input voltage/current/output voltage, input current THD, power factor/efficiency respectively for 400Ω load resistance and -400V reference voltage under 325V(peak) input voltage and 50Hz supply frequency. Fig. 11 to Fig. 13 show the dynamic response due to load and input voltage disturbance.

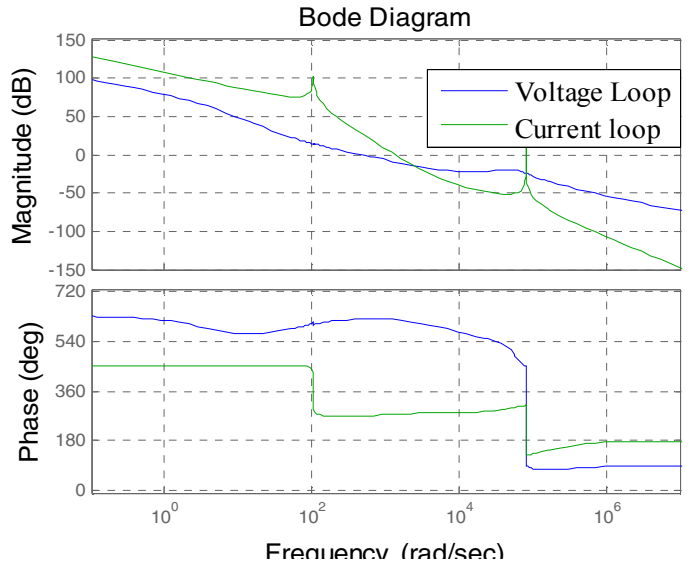


Fig. 6. Stability analysis of voltage/current loop using bode plot.

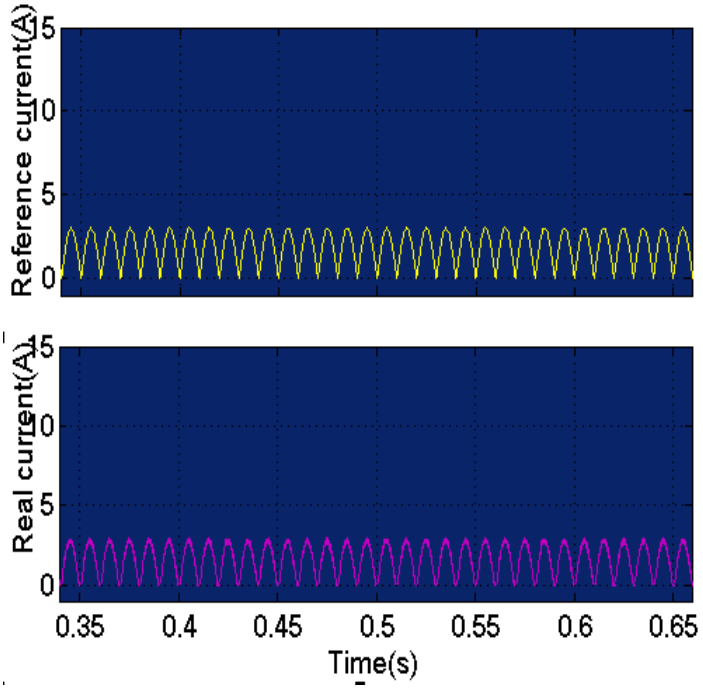


Fig. 7. Reference and real current for 400Ω load

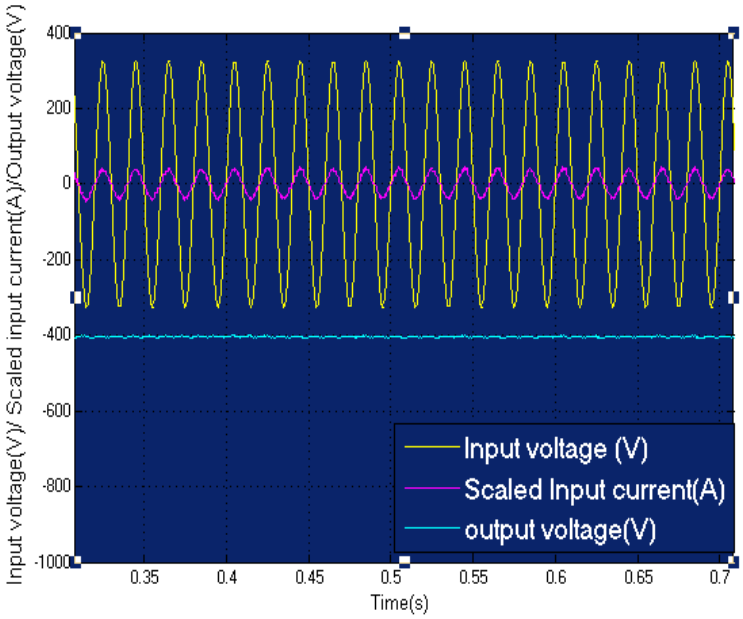


Fig. 8. Input voltage, input current and output voltage for 400Ω load

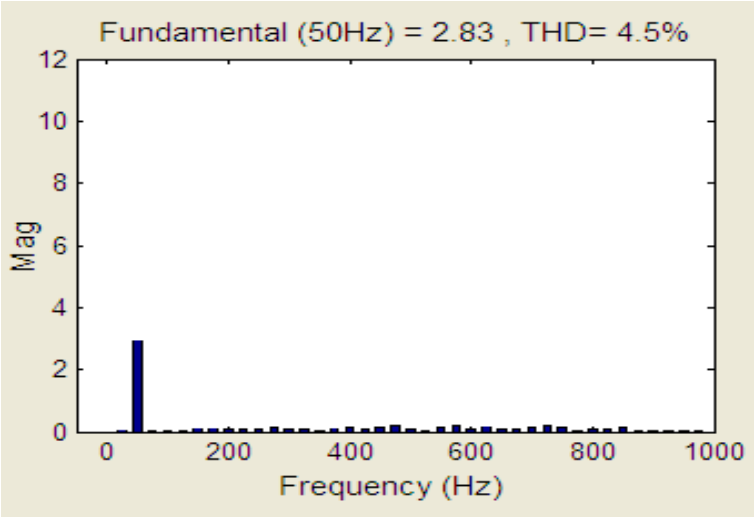


Fig. 9. FFT analysis of input current

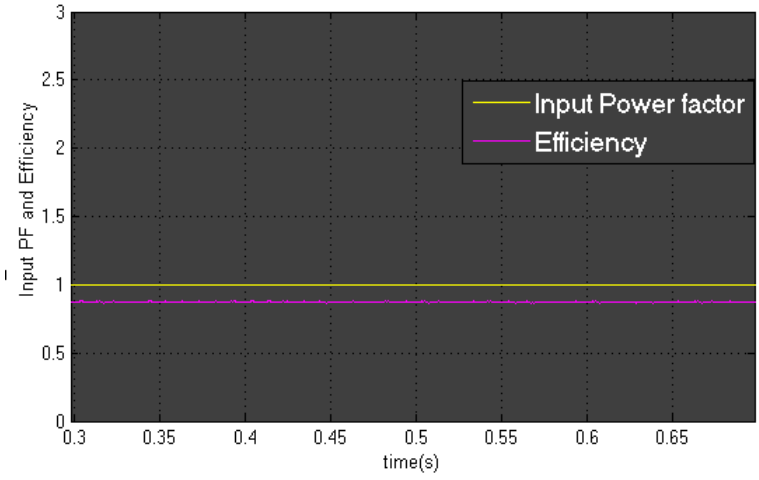


Fig. 10. Input power factor and efficiency

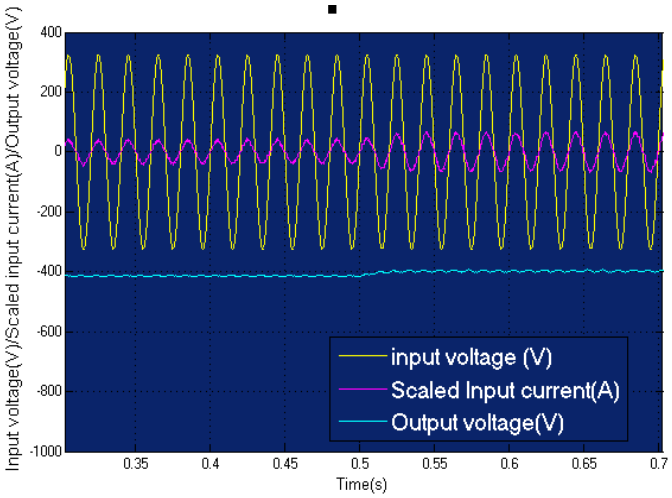


Fig. 11. Dynamic input voltage, input current and output voltage after load changed from 250W to 400W at 0.5s

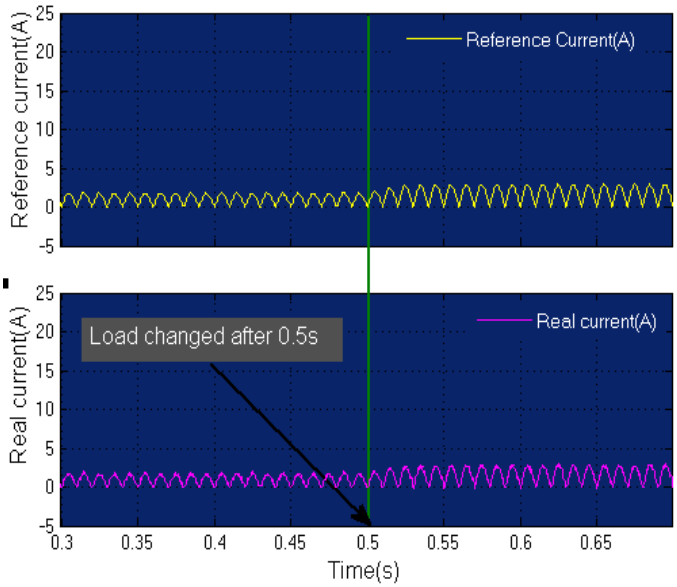


Fig. 12. Dynamic reference and real current after load changed from 250W to 400W at 0.5s

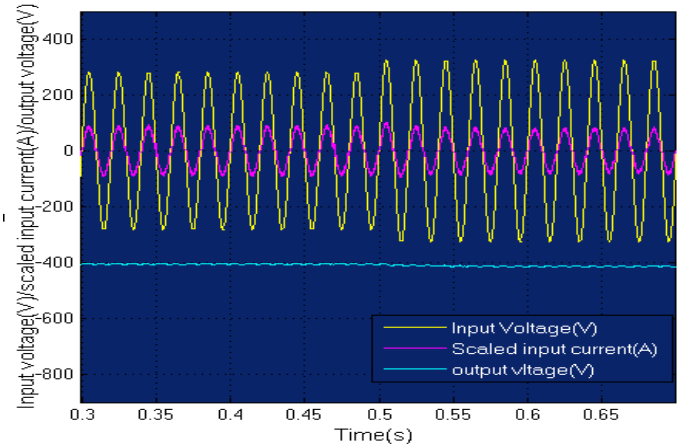


Fig. 13. Dynamic input voltage, input current and output voltage after input voltage changed from 200V(rms) to 230V(rms).

VI. DISCUSSION

From the Bode plot it has been shown that the proposed current loop and voltage loop controller operate in the stable region. According to load demand and input voltage shape the controller is capable to provide required generated reference sine current. The controller adjusts its PWM signal to force the real current to follow the reference current which is shown in Fig. 7. As a consequence we get the in phase input current with voltage with good load voltage regulation, less input current THD and approximately unity power factor which are shown in Fig. 8, Fig. 9 and Fig. 10 respectively. Now the dynamic response is obtained under the load change from 250W to 400W. It has been shown from Fig. 11 and Fig. 12 that reference and real current automatically adjust to tackle the load disturbance with little output voltage change. Similarly from Fig. 13 the system provides the response under input voltage changes from 200V(rms) to 230V(rms) and it has been found the reduction of input current to mitigate the rise of input voltage with little load voltage change.

VII. CONCLUSION

The use of outer voltage and inner current control loop in Ĉuk topology based AC-DC converter has been analyzed and simulated in Matlab Simulink in this paper. The results show the effectiveness of this proposed controller. It has been found unity input power factor along with less than 5% input current THD. The proposed system has significantly improved the overall efficiency and provided good output voltage regulation under the variable load and input voltage disturbance.

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