A Novel Presentation of Reversible Logic Gate in Quantum-dot Cellular Automata (QCA)

Ali Newaz Bahar
Mawlana Bhashani Science and Technology University, Tangail, Bangladesh.
e-mail: bahar_mitdu@yahoo.com

Sajjad Waheed
Mawlana Bhashani Science and Technology University, Tangail, Bangladesh.

Md. Ahsan Habib
Mawlana Bhashani Science and Technology University, Tangail, Bangladesh

***Abstract*— In last few decades, low power processing and small scaling have been successfully achieved by conventional lithography-based VLSI technology. However, this trend confronts serious challenges due to fundamental physical limits of Complementary Metal–Oxide–Semiconductor (CMOS) technology such as ultra-thin gate oxides, short channel effects, doping fluctuations at nano-scale regimes. Quantum-dot Cellular Automata (QCA) technology has been extensively conceivable as one of the alternative, that gives not only the solution of CMOS technology at nano-scale, but also it offers a new method of computation and information transformation. This paper presents a novel representation of reversible gate in QCA. Those proposed circuit has a promising future in constructing of nano-scale low power consumption information processing system and can be stimulated higher digital applications in QCA.**

Keywords—QCA, Majority gate (MV), Feynman gate, Double Feynman gate, Fredkin gate and BJN gate

I. INTRODUCTION

Reversible logic circuits are widely used in power minimization having the application of such as low power CMOS design, quantum computing, optical computing, DNA computing, digital signal processing (DSP), optical information processing, nanotechnology, cryptography, communication, and computer graphics [1], [2], [3], [4]. In the early 1960s, R. Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss. According to Landauer's principle, the loss of one bit of information dissipates $kTln2$ joules of energy, where, k is the Boltzmann's constant and T is the operating temperature [5]. For room temperature T, the amount of dissipating heat is small (i.e. 2.9×10-21 joule), but not negligible. Later Bennett, in 1973, showed that in order to avoid this energy dissipation in a circuit, it must be built from reversible circuits [6].

Now a day's, CMOS technology is approaching its physical limits and facing serious challenges by designing constantly increasing frequencies and downscaling of computational devices. However such technology has found many problems like high leakage current, high power consumption, high lithography cost, low density problem and limitation of speed in GHz range. One of the alternatives is known as Quantum-dot Cellular Automata (QCA) [7], [8], which has recently been recognized as one of the top six emerging technologies with potential applications in future computing [9], [10] for its high speed, high scale integration and low power consumption in various computational applications [8], [11]. A recent study shows quantum dot cellular automata (QCA) are one of the promising new technologies capable to implement the reversible logic circuit [7], [11], [12], [13], [14], [15], [16].

II. QCA BASICS

The basic element of QCA devices is the QCA cell shown in Figure 1(a). The basic structure in QCA is a cell that has four dots positioned at the corners of the squared cell and two mobile electrons [15], [17]. Depending on the position of the electrons, QCA cell has two type of polarization (p) [14], [18]. A polarization of P = +1 (Binary 1) results if cells 1 and 3 occupied, while electrons on sites 2 and 4 result in P = -1 (Binary 0) as shown in Figure 1(b). The cell polarization is defined [11] as equation 1.

$$P=\frac{(\rho_2+\rho_4)-(\rho_1+\rho_3)}{(\rho_1+\rho_2+\rho_3+\rho_4)} \quad (1)$$

Where ρ_i denotes the electronic charge at dot i.

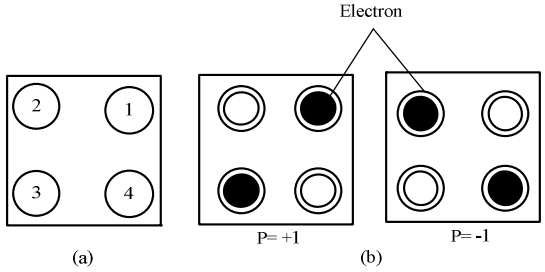


Fig. 1: Basic structure of QCA cell with four dots (a), different position of the electrons based on polarization (b)

The fundamental unit of QCA-based design is QCA wire, three input majority gate and inverter [15]. QCA wire is an array of cells that are aligned one by one shown in Figure 2. The polarization of each cell in a QCA wire is directly affected by the polarization of its neighboring cells on account of electrostatic force. Accordingly, QCA wires can be used to propagate information from one end to another [19].

Three input Majority gate consists of five cells; three inputs, one output and a middle cell. The middle cell named device cell by reason of its function, switches to major

polarization [15], [17] and determines the stable output. Majority gate can be programmed such that it functions as a 2-input AND or a 2-input OR by fixing one of the three input cells to p = -1 or p = +1 respectively as shown in figure 3. The Boolean expression of majority gate is as follows:

$$MV(A, B, C) = AB+AC+BC \quad (2)$$

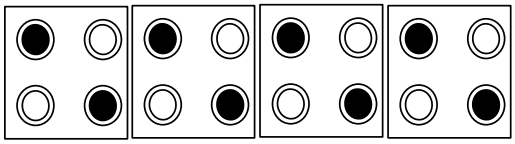


Fig. 2: QCA wires

To make AND gate, we need to set one of the MV input is zero, Equation (3) presents the AND gate equation.

$$MV(A, B, 0) = AB+A.0+B.0= AB \quad (3)$$

To make OR gate, we need to set one of the MV input is 1, Equation (4) presents the OR gate equation.

$$MV(A, B, 1) = AB+A.1+B.1= A+B \quad (4)$$

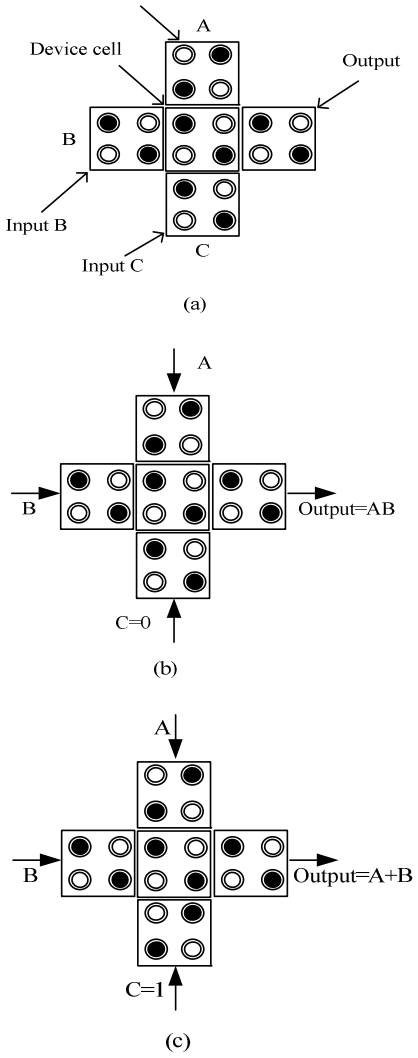


Fig. 3: The QCA majority gate (a), function as (b) the AND gate and (c) the OR gate

III. PROPOSED CIRCUIT AND PRESENTATION

The inverting gate in QCA holds a different structure [11] shown in Figure 4 (a), (b), (c) since the last one (c) operates properly in all various circuits. This inverter is made of seven cell or four QCA wires. The input polarization is split into two polarizations and in the end, two wires join and make the reverse polarization.

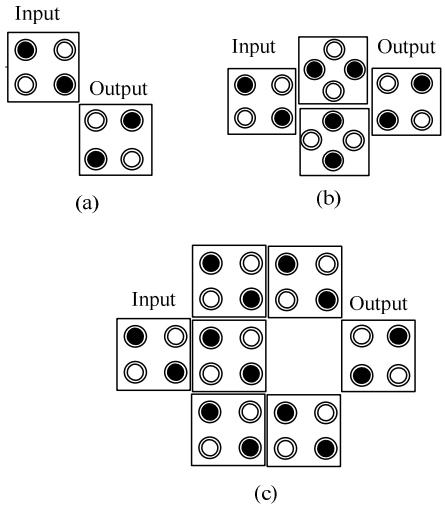


Fig. 4: Three different structure of Inverter gates (a) (b) (c)

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs.

A. Feynman Gate

Feynman gate which is a 2*2 gate and also known as controlled NOT. The inputs vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P = A, Q = A⊕B [Q=MV (MV (A', B, -1), MV (A, B', -1), 1].Figure 5 (a) shows the block diagram of Feynman gate and (b) shows the QCA representation.

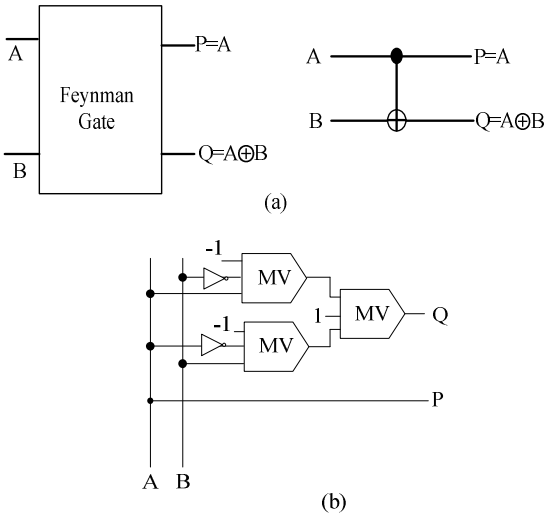


Fig. 5: Block diagram of (a) Feynman gate (b) proposed diagram of Feynman gate in QCA

B. *Double Feynman gate*

Figure 6 (a) shows a 3*3 Double Feynman gate [20].The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q=A⊕B, R=A⊕C. Figure 6 (a) shows the block diagram of Double Feynman gate and (b) shows the QCA representation of this gate.

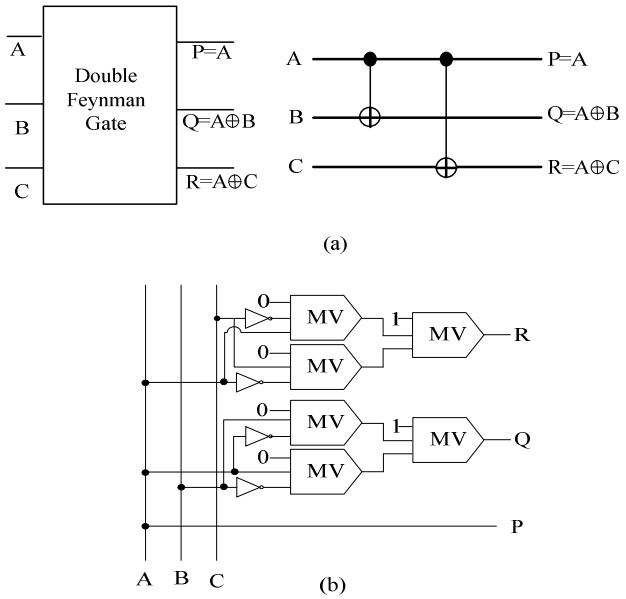


Fig. 6: Block diagram of (a) Double Feynman gate (b) proposed diagram of Double Feynman gate in QCA

C. *Fredkin gate*

Figure 7 (a) shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The outputs are defined by P = A, Q = A'B+AC [Q=MV (MV (A', B, 0), MV (A, C, 0), 1], R = AB+A'C [R= MV (MV (A, B, 0), MV (A', C, 0), 1)]. Figure 7 (b) shows the QCA representation of this gate.

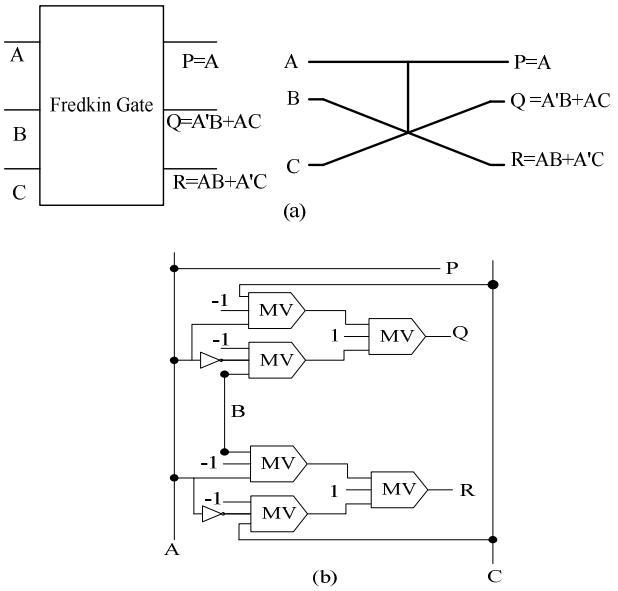


Fig.7: Block diagram of (a) Fredkin gate (b) proposed layout design in QCA omitting multilayer crossing

D. *BJN gate*

The basic 3*3 reversible logic gates "BJN Gate" shown in figure 8 (a) and figure 8 (b) shows the block diagram of this gate in QCA. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q= B, R= (A+B) ⊕ C.

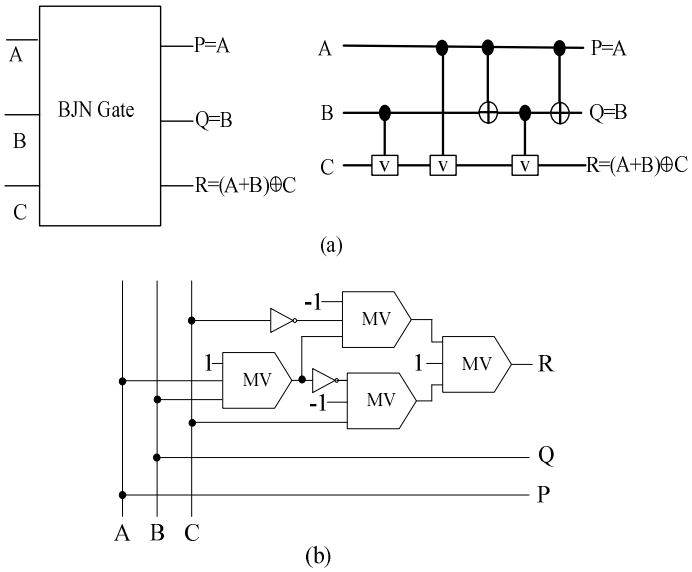
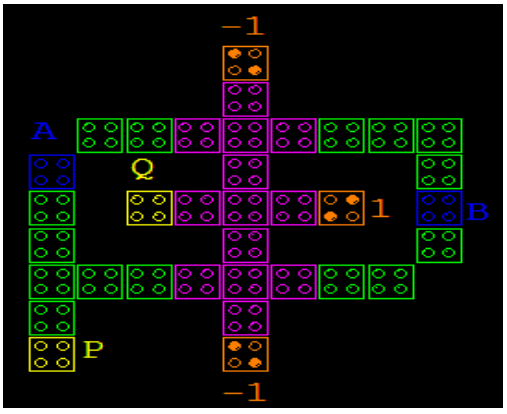


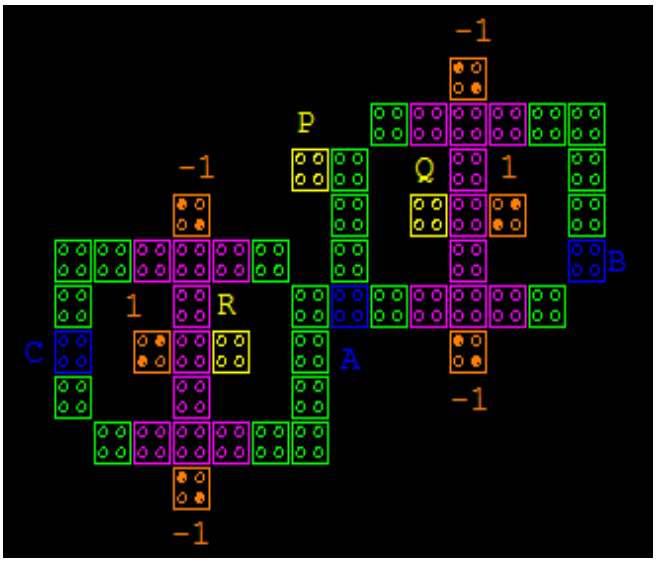
Fig. 8: Block diagram of (a) BJN gate (b) proposed diagram of BJN gate in QCA

IV. Simulation And Results

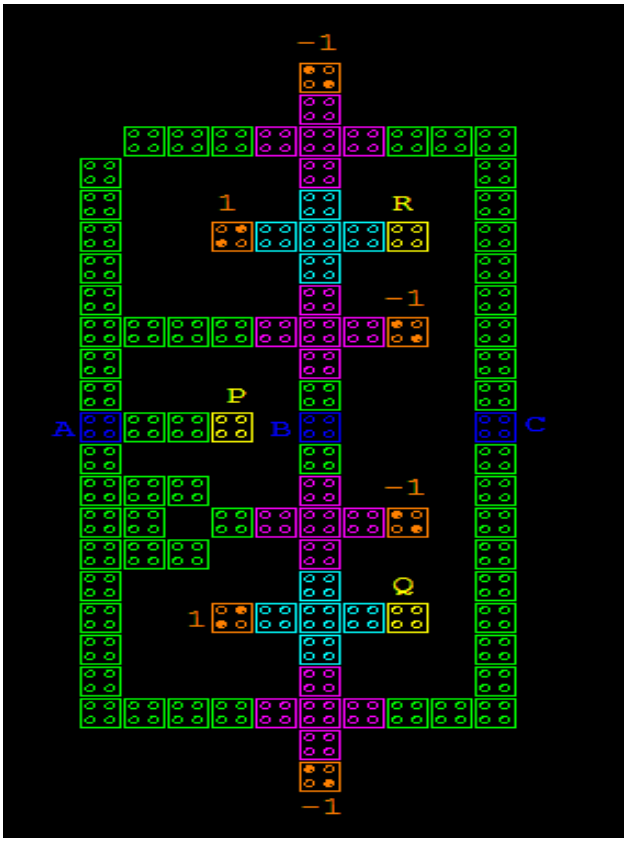
Our proposed circuits were functionally simulated using the QCADesigner [21]. The following parameters are used for a Bistable Approximation: cell size=18nm, number of samples=50000, convergence tolerance=0.0000100, radius of effect=65.000000nm, relative permittivity= 12.900000, clock high= $9.800000e^{-022}$ J, clock low= $3.800000e^{-023}$J, clock shift= 0, clock amplitude factor= 2.000000, layer separation=11.500000 and maximum iterations per sample=100. Most of the above mentioned parameters are default values in QCADesigner. The figure 9 shows the simulated circuit design and figure 10 shows input and output waveforms of our proposed gate in QCADesigner.



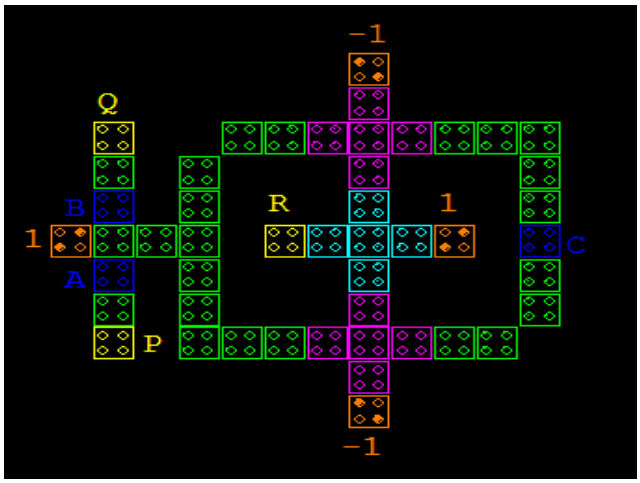
(a)



(b)

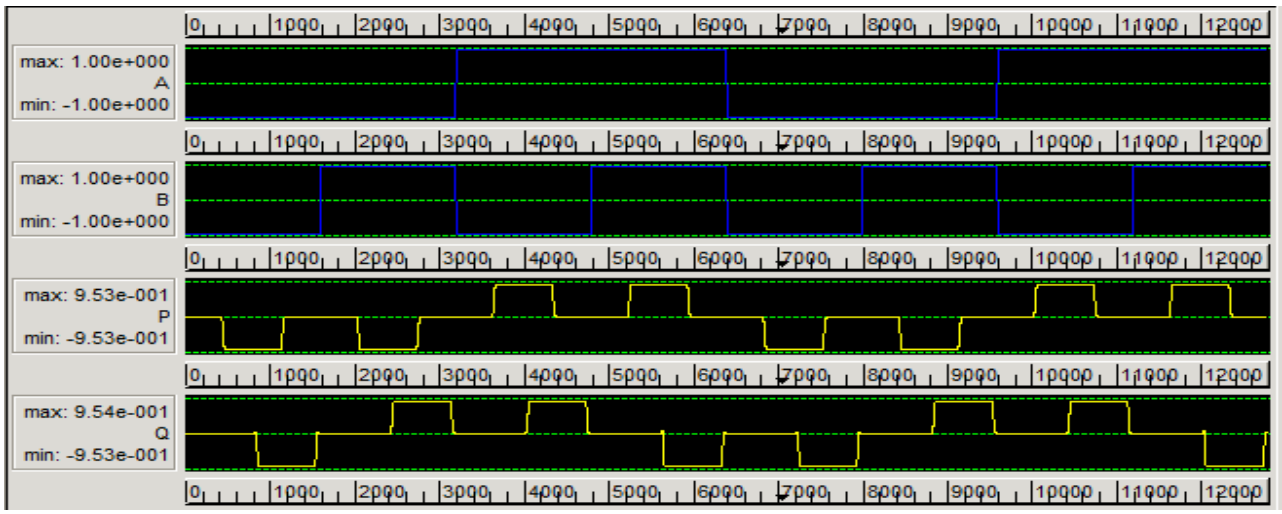


(c)

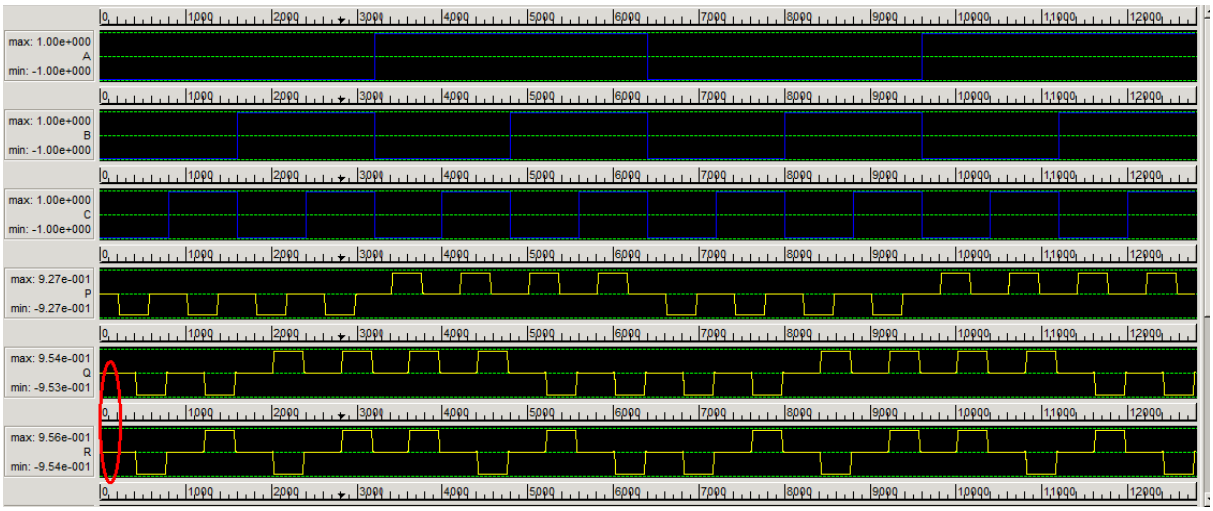


(d)

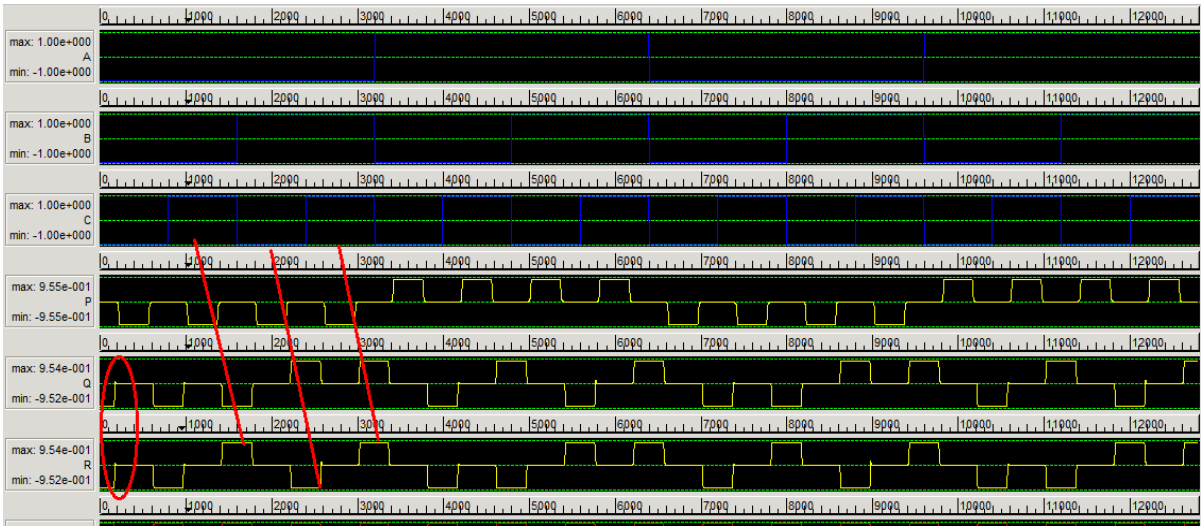
Fig. 9: Simulated gate in QCADesiner (a) Feynman gate (b) Double Feynman gate (c) Fredkin gate (d) BJN gate



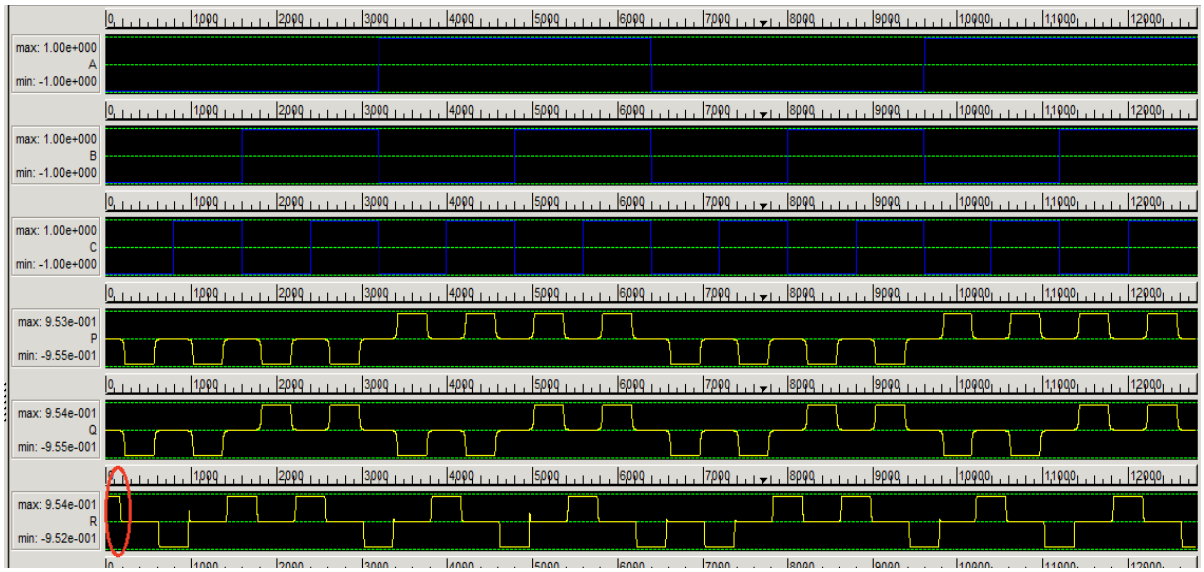
(a)



(b)



(c)



(d)

Fig. 10: Input output waveforms of (a) Feynman gate (b) Double Feynman gate (c) Fredkin gate (d) BJN gate

TABLE I. PERFORMANCE ANALYSIS OF PROPOSED GATE

Parameter	Feynman gate	Double Feynman gate	Fredkin gate	BJN gate
Number of cells	34	51	100	48
Covered area (μm^2)	0.036	0.06	0.092	0.0525
Clock used	2	2	3	3
Time delay (clock cycle)	0.5	0.5	0.75	0.75

V. CONCLUSION

Quantum-dot cellular automata, one of the most emerging nanotechnologies, which is suitable for designing low power consuming logic circuits. A number of QCA-based logic circuits with smaller feature size, higher operating frequency, and lower power consumption than CMOS have been presented in this paper. Furthermore, those proposed circuits have been simulated using QCADesigner and tested in terms of complexity (cell count) and area.

REFERENCES

[1] Al-Rabadi, A. N.: Reversible logic synthesis: From fundamentals to quantum computing. Springer (2004)

[2] Thapliyal, H., & Ranganathan, N.: Testable reversible latches for molecular QCA. In Nanotechnology, NANO'08. 8th IEEE Conference, pp. 699-702 (2008)

[3] Ma, X., Huang, J., Metra, C., & Lombardi, F.: Reversible gates and testability of one dimensional arrays of molecular QCA. J. Electronic Testing **24**, 297-311(2008)

[4] Thapliyal, H., & Ranganathan, N.: Reversible logic-based concurrently testable latches for molecular QCA. Nanotechnology, IEEE Transactions on**9**, 62-69 (2010)

[5] Landauer, R.: Irreversibility and heat generation in the computing process. IBM J. Research and Development **5**,183-191 (1961)

[6] Bennett, C. H.: Logical reversibility of computation. IBM J. Research and Development**17**, 525-532 (1973)

[7] Lent, C.S., Tougaw, P.D., Porod, W.: Bistable saturation in coupled quantum dots for quantum cellular automata. Appl. Phys. Lett. (1993). doi:10.1063/1.108848

[8] Orlov, A.O., Amlani, I., Bernstein, G.H., Lent, C.S., Snider, G.L.: Realization of a functional cell for quantum- dot cellular automata. Science (1997). doi:10.1126/science.277.5328.928

[9] Amlani, I., Orlov, A. O., Kummamuru, R. K., Bernstein, G. H., Lent, C. S., & Snider, G. L.: Experimental demonstration of a leadless quantum-dot cellular automata cell. Appl. Phys. Lett. **77**, 738-740 (2000)

[10] Wilson, M., Kannangara, K., Smith, G., Simmons, M., & Raguse, B.: Nanotechnology: basic science and emerging technologies. CRC Press (2002)

[11] Tougaw, P. D., & Lent, C. S: Logical devices implemented using quantum cellular automata. J. Appl. Phys. **75**, 1818-1825 (1994)

[12] Meurer, B., D. Heitmann & Ploog, K.: Single electron charging of quantum-dot atoms. Physical review letters. **68**, 1371 (1992)

[13] Ashoori, R. C., et al.: N-electron ground state energies of a quantum dot in magnetic field. Physical review letters. **71**, 613 (1993)

[14] Lent, C. S., & Tougaw, P. D.: Device architecture for computing with quantum dots. Proceedings of the IEEE**85**, 541-557 (1997)

[15] Amlani, I., Orlov, A.O., Toth, G., Bernstein, G.H., Lent, C.S., Snider, G.L.: Digital logic gate using quantum-dot cellular automata. Science (1999). doi:10. 1126/science.284.5412.289

[16] Orlov, A. O., Amlani, I., Toth, G., Lent, C. S., Bernstein, G. H., & Snider, G. L.: Experimental demonstration of a binary wire for quantum-dot cellular automata. Appl. Phys. Lett. **74**, 2875-2877 (1999)

[17] Ling-gang, Z., Qing-kang, W., & Yong-bing, D.: A new phenomenon of quantum-dot cellular automata. Journal of Zhejiang University Science A, **6**, 1090-1094 (2005)

[18] Meurer, B., Heitmann, D., & Ploog, K.: Excitation of three-dimensional quantum dots. Phys. Rev. B, 48, 11488 (1993)

[19] Arman, R., Hossein, K., Samira, S., Keivan, N.: A Novel Architecture for Quantum-Dot Cellular Automata Multiplexer. Int. J. Computer Science Issues. **8**, 55-60 (2011)

[20] Parhami, Behrooz. "Fault-tolerant reversible circuits." In Signals, Systems and Computers, 2006. ACSSC'06. Fortieth Asilomar Conference on, pp. 1726-1729. IEEE, 2006.

[21] Walus, K., Dysart, T. J., Jullien, G. A., & Budiman, R. A.: QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata. Nanotechnology, IEEE Transactions on**3**, 26-31(2004)