Measurement of Gate Delay in Armchair Graphene Nanoribbon Considering Degenerate Regime

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Abstract—**Graphene nanoribbons (GNRs) are considered as a tremendous discovery in the beginning of 21st modern science.For the demanding of using semiconducting electronic properties armchair GNRs are born.To observe the electron transport through A-GNR based field effect transistor one of the important properties of these device is capacitance through channel and dielectric substance, gate delay. The classical capacitance which is only determined by GNR width and insulator thickness failed to discuss the behavior of electron through channel .In these factor quantum capacitance which works in any integer nature of gate voltage is termed as degenerate regime quantum capacitance .Including above all mentioned capacitance gives a total capacitance in gate which is faced by electron.Upon this observation delay faced by carrier for gate capaciatnce and cut off frequency can be observed without considering other capacaitance. This work presents an investigation and calculation of the bandgap structure and the classical and quantum capacitance in degenerate regime of A-GNRs .Then using calculated value the gate delay will be observed for corresponding gate voltage. At last we will measure cutoff frequency neglecting other capacitance formed in A-GNR based FET.**

Keywords—Graphene nanoribbon, bandgap, classical capacitance, quantum capacitance,degenerate regime,gate delay, cutoff frequency.

I. INTRODUCTION

Graphene a single layer of carbon atoms which is a hexagonal lattice like a two dimensional crystal structure [1] is a promising material in the era of nanoscience. Nowadays it is paying attention because of its extraordinary electronic properties. Because of its high carrier mobility(~10000 $cm^2V^{-1}s^{-1}$ at room temperature) it has an alternate of silicon (Si) as a channel of FETs with a view to high switching speed and ballistic transport [2].The high switching speed can be observed upon the proper experimentation on carrier transit delay. Even high frequency performance of the GFETs can also be investigated by extracting its carrier delays [3]throughout the graphene channel.

The foremost criteria to demonstrate electronic properties of a material are considerable bandgap and material should have semiconducting behavior. But unfortunately naturally graphene is a zero band gap semiconductor which incapable to being turns off. Bandgap can be created by using narrow strips of graphene which is termed as GNRs[4].There are different kinds of GNRs. One is the edges which is terminated by hydrogen atoms are called armchair GNRs shown in Fig.1 another is zigzag pattern edge shape are called zigzag GNRs [5].Among them the A-GNRs demonstrate semiconducting properties depending upon the number of hexagonal rings (N or dimer line)across the width.

To observe the switching speed it is necessary to have a look upon electron transport properties where A-GNR is placed on the dielectric substance like SiO_2 .Here the current through GNR is controlled by back gate voltage and capacitance in these devices is visualized by oxide layer capacitance[6] (classical capacitance). For this the quantum phenomena cannot be resolved here as already device goes to nanoscale. In this condition quantum capacitance is only a solution. There are considerable amount of gate delay is occurred because of the presence of these capacitance which is controlled by a gate voltage.

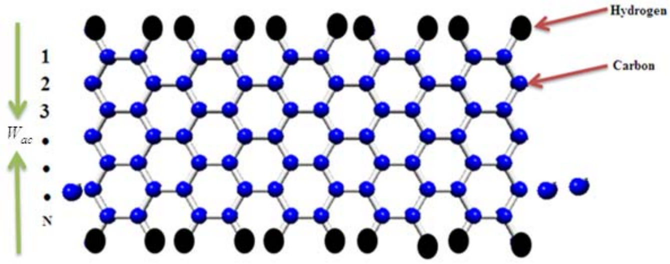

Fig.1.Schematic of a A-GNR. The black circles denote hydrogen atoms terminating the edge carbon atoms(blue circles). The number of dimmer line and the ribbon width are represented by *N* and W_{ac}, respectively.

In this we will first calculate a definite logical width of A-GNR from its number of dimer line across the width. Then we will calculate an amount of band gap energy for nanosized width. By using this bandgap energy and width we will calculate classical capacitance, quantum capacitance in degenerate regime which means all time in operation without regarding the value of gate voltage. Upon this value we will calculate gate delay through A-GNR which will be valuable information in designing of high performance GNR based device.

II. Theory

As stated earlier A-GNR structure is like armchair pattern where the width can be calculated from the dimerline as[7]

$$W_{ac} = (N-1)\frac{\sqrt{3}}{2}a \qquad (1)$$

where $a=0.142\ nm$ is the nearest neighbor distance.

Bandgap energy which is the first criteria for the materials showing semiconducting behavior .Now the relations between band gap energy E_G and width of GNRs can be derived as [5]

$$E_G = -\frac{2\pi(\gamma_1 - 2\gamma_3)}{\sqrt{3}(N+1)} + \frac{6(\gamma_3 + \Delta_{\gamma_1})}{N+1} \qquad (2)$$

where γ_1 = - 3.2 eV is the first nearest neighbor hopping parameter, γ_3 = - 0.3 eV is the third nearest neighbor hopping parameter, Δ_{γ_1} = - 0.2 eV is the correction factor on γ_1 .

The bandgap energy can be clearly understood from its E-k relation which is expressed as [4]

$$E = \sqrt{\left(\left(\frac{\Delta}{2}\right)^2 + (\hbar\gamma_s k)^2\right)} \qquad (3)$$

where $\hbar$ is the reduced plank constant,

Capacitance is one of the important properties to observe the electron transport behavior through a material.As the current is controlled through A-GNR by back gate voltage capacitance in these device completely determined by simple classical capacitance which is[8]

$$C_{ins} = N_G \varepsilon_o k\left(\frac{W_{ac}}{t_{ox}} + \alpha\right) \qquad (4)$$

where N_G is the number of gates, k is the relative dielectric constant of SiO_2 , ε_0 is the permittivity of vacuum is $8.854\times10^{-12} C^2 m^{-2} N^{-1}$, t_{ox} represents oxide thickness and $\alpha = 1$ is a dimensionless fitting parameter [8].

As the electron pass from gate insulator it will later face a path which is named GNR channel.As the A-GNR is nanoscale the capacitance in these region demonstrate quantum phenomena so the capacitance formed in this area is called quantum capacitance which is expressed as[9]

$$C_{QND} = \frac{e^2}{3ta\pi}\left(\frac{x + \frac{E_G}{2k_B T}}{\sqrt{x + x\frac{E_G}{k_B T}}}\right) f(E) \qquad (5)$$

where k_B = $8.6\times10^{-5}\ eVK^{-1}$ (Boltzmann constant), $e = 1.6\times10^{-19}$ Columb, T = 300k Room temperature, t = 2.7 eV, hopping integral of perfect GNR [10], and $x = E - E_G/2$.

And the Fermi probability function is given by

$$f(E) = \frac{1}{\exp\left(\frac{E - E_F}{k_B T}\right) + 1} \qquad (6)$$

It is stated that under thermal equilibrium the Fermi level is exactly at the Dirac point $E_F = 0$.

If local electrostatic potential in a GNR is tuned by a gate voltage, the Fermi level locates within the conduction band. when degeneracy of capacitance can be determined. There are two types of degeneracy occurred .But one regime runs in all positive or negative value of gate voltage which is called degenerate regime.

In degenerate regime, $E_F - \frac{E_G}{2} < 3k_B T$ and therefore, the Fermi function can be approximated as $f(E)$ = 1. This condition can be understood from Fig. 2.

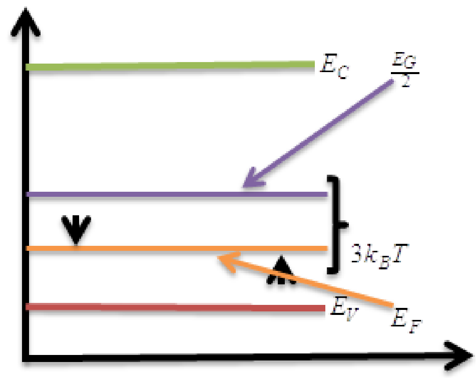

Fig.2.Energy Band diagram where E_V is valence band energy , E_C denotes conduction band energy and E_F Fermi level energy

The degenerate regime only work if the variable $E_F = eV_g$ is so that $E_F - \frac{E_G}{2}$ is lower than $3k_B T$.

Now the reduced Fermi function is related to gate voltage, V_g which is denoted by [10]

$$\eta = \frac{eV_g - eV_T}{k_B T} \quad (7)$$

Here, V_T is the threshold voltage for $\frac{E_G}{2}$.

So the gate capacitance including classical and quantum capacitance in degenerate regime is denoted as [8]

$$\frac{1}{C_G} = \frac{1}{C_{QND}} + \frac{1}{C_{ins}} \quad (8)$$

which indicates that the gate capacitance is the serial combination of the quantum capacitance in degenerate regime and the classical capacitance.

From this we can calculate the gate delay for corresponding gate capacitance is

$$\tau_G = \frac{C_G |V_g|}{I_{on}} \quad (9)$$

To calculate the delay, an arbitray value is used $\mathrm{Ion} = 10^{-2}\,\mathrm{A}$ represents on current.

In future for observing performance of A-GNR frequency for RF A-GNR FETs can be calculated neglecting other capacitance like[3]

$$f = \frac{1}{2\pi \tau_G} \quad (10)$$

III. RESULTS AND DISCUSSION

The electronic properties of GNRs can be measured by varying the width of the ribbon. The width of the GNRs is derived by their number of dimer lines which is obtained from equation (1) and shown in Fig. 2.

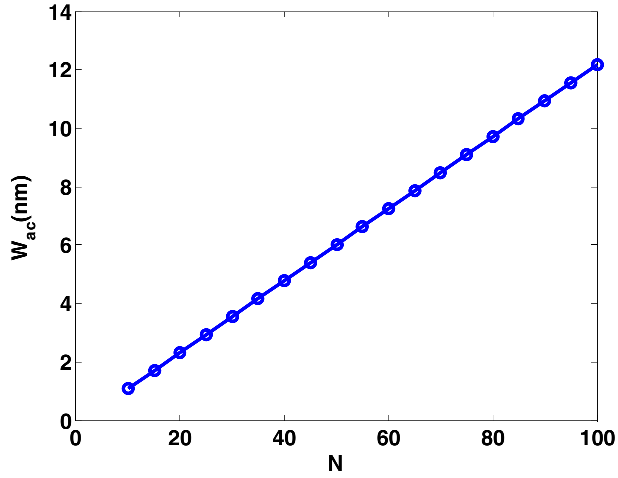

Fig.3.Width of Armchair nanoribbon in (nm) vs. Number of dimer line.

The curve shows that the width of A-GNR is increasing for increasing number of dimerline.Here the response between dimerline and width is linear.

Fig. 4 plots the bandgap energy (E_G) as a function of the width (W_{ac}) of A-GNR. The bandgap energy is calculated using equation (2).

As shown in Fig. 4, the A-GNRs are semiconductor with energy gaps which is inversely proportional to the channel width. In order to go to the conduction band from valence

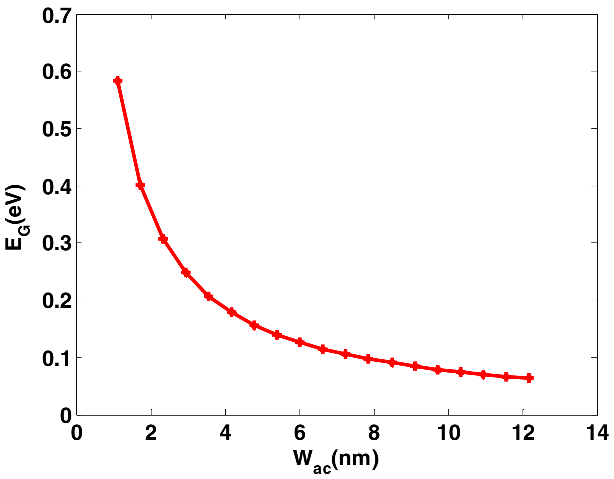

Fig.4.Bandgap Energy (*eV*) vs. width (nm)of A-GNR .

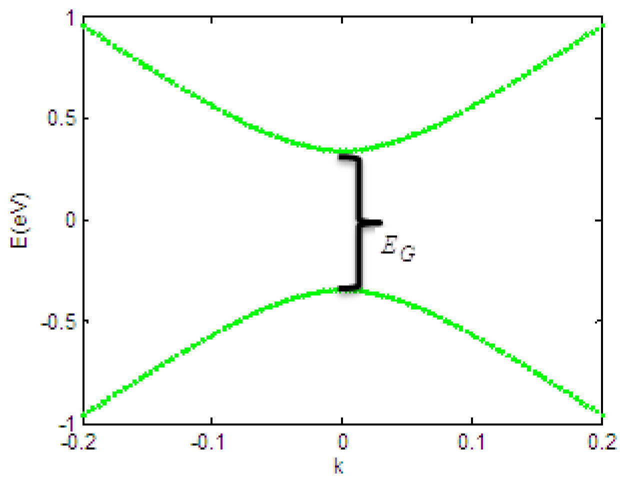

Fig.5.First sub-band structure of A-GNRs using *N=90.*

band the electron must have to achieve an amount of energy which is equal to the bandgap energy.

Fig. 5 shows clear idea of bandgap energy between conduction band and valence band. The negative portion is valence band and positive portion is conduction band.

Here for using N=90 we get energy band gap 0.0707 eV which is much lower for the sake large structure with 10.94nm width of A-GNR.

Now the capacitance which can be designed from device geometry(width of A-GNR, insulator thickness, number of gate) is shown in Fig.6.

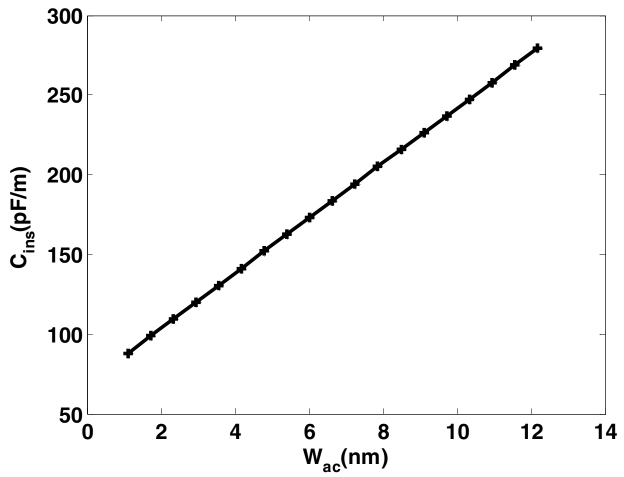

Fig.6.Classical capacitance (*pF/m)* vs. A-GNR width (*nm*) at oxide thickness (*nm)* of 4 nm for double gate GNRFET.

From Fig. 6, it is observed that classical capacitance has a linear response with width of A-GNR.The figure is plotted using SiO_2 thickness at 4nm and number of gate is 2.Here capacitance value is noted as 88.17 pF/m to 279.25 pF/m.

When the electron pass from gate to channel the classical capacitance does not give full information of electron movement through the channel. As the device structures decreasing into nanoscale quantum capacitance become dominant and therefore must be taken into account.

But here two types of regime is assumed where one regime run all time without regarding the nature of gate voltage. For this regime electron movement is all time on. Fig.7 shows the nature of quantum capacitance for the corresponding gate voltage.

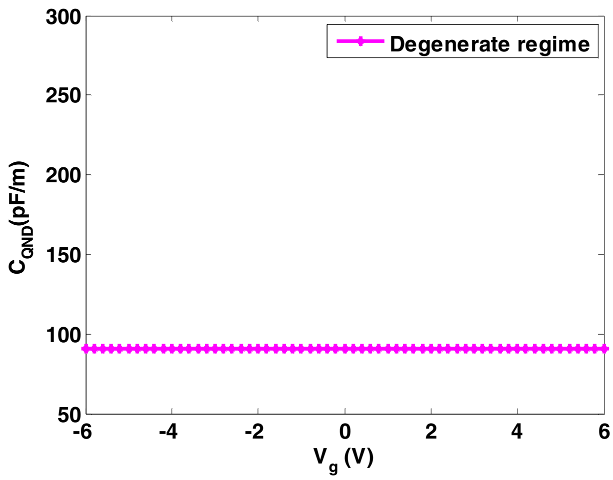

Fig.7.Quantum capacitance (C_{QND}) vs. gate voltage (V_g) in, degenerate regime for W_{ac} = 10.94 nm (*N =90).*

Because of $E_F - \frac{E_G}{2} < 3k_BT$ condition the $f(E)=1$ for this capacitance give a constant value without regarding the gate voltage.Here the quantum capacitance in degenerate regime is calculated as 90.9670 pF/m.

Now if we look quantum capacitance along with classical capacitance the Fig.8 shows classical capacitance is dominant over quantum capacitance. But as the A-GNR is in nanoscale quantum capacitance in degenerate regime hampers electron movement through nanoscale channel.

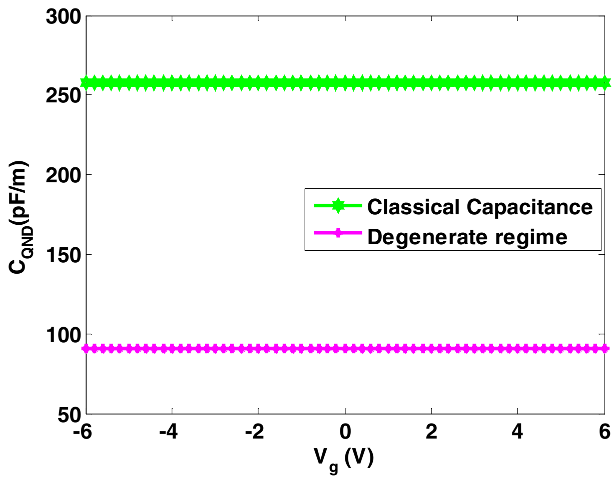

Fig.8.Capacitance (Quantum capacitance in degenerate regime and Classical) vs. gate voltage (V_g) for W_{ac} = 10.94nm.

For the series combination of quantum capacitance in degenerate regime and classical capacitance which gives total gate capacitance that is sown in Fig.9.

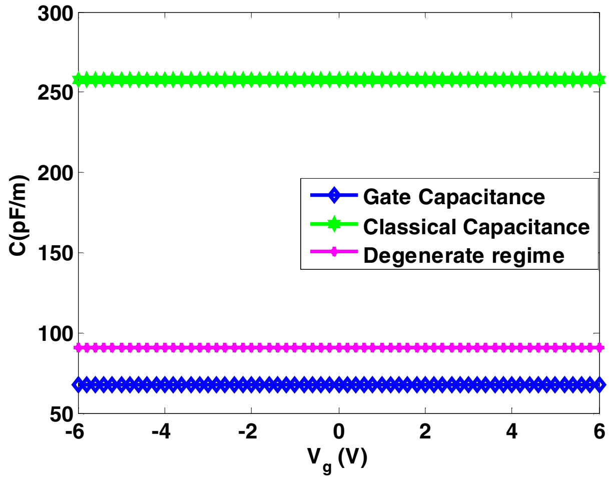

Fig.9.Capacitance (Gate,Quantum capacitance in degenerate regime and Classical) vs. gate voltage (V_g) for W_{ac} = 10.94nm.

Fig.8 shows that because of their mutual impact gate capacitance is lower than the quantum capacitance in degenerate regime and classical capacitance. The gate capacitance is noted here 67.2560 pF/m

From this obtained value we will get the delay faced by the carrier in the gate which can be controlled by gate voltage. But the delay is only positive so we have to count the positive value of gate voltage. Now the gate delay is shown in Fig.9.

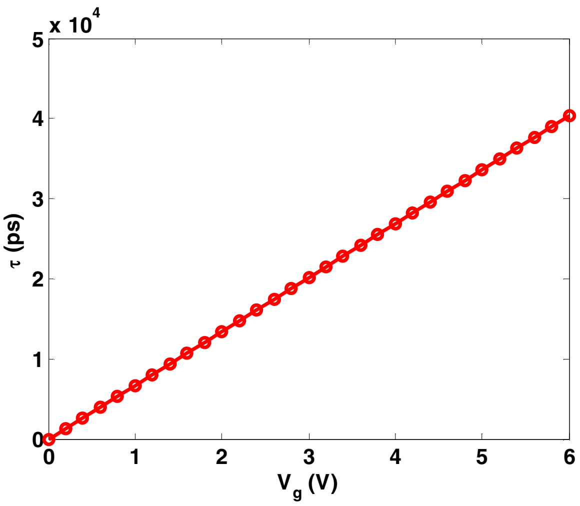

Fig.10.Gate delay (ps) vs. gate voltage (V)

Fig.10 shows an linear response of gate delay with gate voltage and with the gate capacitance. So gate delay ocuured in such manner as the gate capacitance and gate voltage behave.Here the gate delay measured from 0.1345 $\times 10^4$ to 4.0354×10^4 ps.

If the other is somehow minimized than the cutoff frequency curve for gate voltage will be like Fig.11.

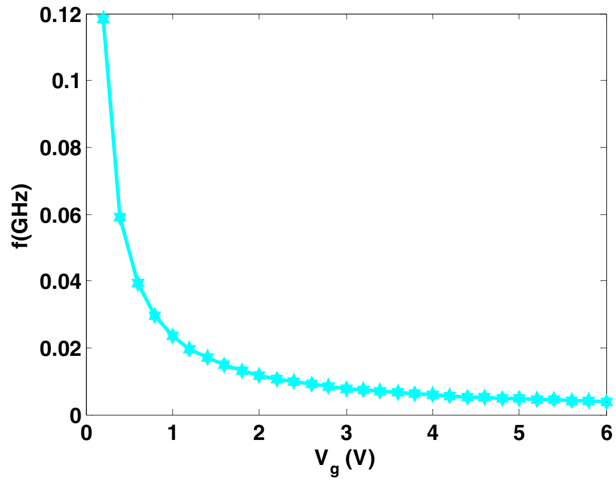

Fig.11.Cutt off Frequency(GHz) vs. Gate volage(V)

Here the cutoff frequency is measured from 0.1183 to 0.0039 GHz.

IV. Conclusion

In this paper our investigation follows an continuous interrelated path. Like at first, the band structure of A-GNRs is investigated as a function of ribbon width. Then for using one layer of A-GNR is used as 10.94nm width.Then we have investigated the classical capacitance as well as the quantum capacitance in A-GNRs. The classical capacitance increases with the increase with width of A-GNR. The quantum capacitance is discussed in degenerate regime which is all time give a value from -6V to 6V gate voltage. The results show that the classical capacitance dominates over the quantum capacitance in the degenerate regime and gate capacitance. Later we have measured and notice response of the gate delay occurred with gate capacitance. If we can neglect other capacitance than we will find a cutoff frequency which is also measured and it decreases with the increase of gate delay.

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