Implementation of a Driver Circuit in 65nm CMOS technology for Body-Coupled Communication

Md Hasan Maruf and Abdulah Korishe
Department of Electrical Engineering
Linköping University
Linköping, Sweden
Email: mdma699@student.liu.se, korab992@student.liu.se

Sajib Roy
Faculty, Department of ETE
University of Liberal Arts Bangladesh
Dhaka, Bangladesh
Email: sajib.roy@ulab.edu.bd

Abstract—**This paper presents a newly cascaded voltage mode tri-state driver circuit for body-coupled communication (BCC) designed in 65 nm CMOS technology. Each stage of the driver circuit has been resized to meet the requirement of the BCC. It has a driving capability of 6 mA from 1.2 V supply with 10 MHz operating frequency. Different analysis has been performed to get the optimum results for the proposed circuit. The analysis shows cycle to cycle jitter to be less than one and power supply rejection ratio (PSRR) 65 dB, indicating the good emission of supply noise. In addition, the driver circuit does not require a filter to emit the noise because the body acts like a low pass filter.**

Keywords—BCC, driver circuit, noise analysis, corner analysis, PSRR

I. INTRODUCTION

The fast growth of low power integrated circuit, wireless communication such as Bluetooth, ZigBee, Wi-Fi and wireless sensor network has created a new generation of wireless body area network (WBAN) [1]. The human body is modeled as an electrical channel for communication by using the concept of capacitive coupling or AC coupling which allows only AC signal while blocks the DC signal. The concept of near field communication is first introduced by Zimmerman [2] in 1995 since then it turns to be an important pathway in the area of personal area networks (PANs).

The strongest motivation of using human body as a communication channel is its speed, less interference, low power consumption and inherent security system compared with the existing wireless communication systems like Bluetooth, Zigbee and WiFi. The low power transceivers for BCC is mainly focused on developing architecture of transceivers using human body as a communication channel that is capable of higher data rate (10 Mbs) operating at 10 MHz frequency range. This application of near field communication (NFC) with BCC is going to increase the number of application as well as solves the problem with cell based communication system depending upon the frequency allocation. The cell based communication systems which make the basic of the today's mobile or wireless communications, are quite unable to meet the requirements of huge number of information load from all over the world because of the fixed number of frequency allocation table. So it is time to look for such a communication system, which is capable of solving the issue with limited number of frequency careers as well as the speed and low power consumption. Actually the big companies like Apple, Google, Ericsson and Telenor are also looking forward to find a way of solution that does not require the frequency spectrum. So the inductive or capacitive coupling technique by using a human body as a communication channel could be a solution for the wireless or mobile communication. Moreover, a low power transceiver for BCC would be given in favor of capacitive coupling as viable means of next generation touch-and-go communication.

Apart from, this type of body based communication is more secure compared with the existing wireless systems because the electrostatic fields are used with low range and the strength of the fields falls extensively with the distance cube. So this kind of body based device is less risk of hacking, eavesdropping, interference and so on. The BCC devices could be suffered less from interference because the high attenuation by human body, which is a big concern for any wireless and wired communication system.

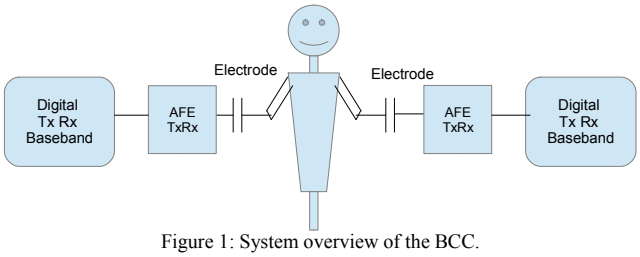

Figure 1: System overview of the BCC.

In this paper, a driver circuit has been implemented to control the overall BCC in a right way. Figure 1 shows overview of a transceiver to develop the BCC. The transmitted signal can be high in amplitude, but after the first electrode the amplitude is decayed on the other side of the capacitor plate. The signal is more attenuated after the human body and the signal strength can be found in mV or μV range. So, it is important to design a strong output driver that provides high amplitude, capable of driving high capacitor at load, high current obviously that costs more power consumption that is not desired. The proposed driver circuit meets the basic requirement and gives more useful features.

II. BASIC REQUIREMENTS FOR AFET$_X$

The analog front end transmitter requires a high supply voltage to produce a significant amount of current [3]. The driving capability of the driver needs to be strong enough to drive a huge capacitor of 100 pF. The carrier frequency for BCC is selected in a range of 10 MHz to 12 MHz. The average current and the peak current of the driver circuit can be expressed by the following equation,

$$I_{avg} = P_{Txout}/V_{DD} = \alpha V^2_{swing} fC / V_{DD} \quad (1)$$

$$I_{peak} = C(dv/dt) \quad (2)$$

where P_{Txout} is the output power transmitter, V_{DD} is supply voltage, α is switching activity, V_{swing} is voltage swing, f is operating frequency, C is load capacitor or electrode capacitor, I_{peak} is the driver circuit current. Assuming V_{DD} is 1.2 V, α is 0.5 (Manchester encoding), V_{swing} is V_{DD} / 2 = 0.6 V, f is 10 MHz, C is 100 pF, dv/dt = 0.6 V / 10 ns = $6x10^7$. So we get the following values,

$$I_{avg} = 0.15 \text{ mA}$$
$$I_{peak} = 6 \text{ mA}$$

So, the minimum required current is 6 mA for the driver circuit to operate the load capacitor. Another important issue regarding the propagation delay of the signal is that the delay must be minimized to avoid the long term jitter. The propagation delay depends on the termination resistor and the load capacitor value.

III. BASIC ARCHITECTURE OF THE OUTPUT DRIVER

The standard requirement, for designing a strong driver circuit, is a significant amount of current due to high attenuation of the human body at the same time low capacitance (small plates) at the transmitter side. On the other hand, the receiver might not detect the weak signal so that the driver circuit need to maintain the voltage level. Basically, there is no filter block for this design because of very well noise reduction by the body channel which is a great advantage of BCC. In this paper, the driver circuit is designed in such a way that it can maintain the signal quality which depends on the pulse distortion, skew and systematic jitter.

The basic architecture of the output driver is chosen as tri-state voltage mode driver [4]. In figure 2, the tri-state voltage mode is shown where it requires the less power for the BCC transmitter because it does not need any modulation block having only one inverter type driver. Due to impedance mismatch it is very difficult to maximize the transmitting power with single inverter driver. A double inverter topology can be used to increase the transmitting power with constant output impedance. The output driver can be prompt in double stage by combining a single inverter and an identical inverter with drain resistor or termination resistor. The second stage consists of two buffer circuit connected to the gate of the two push-pull transistor having same delay with the single inverter. The circuit draws a sufficient amount of current at termination end of the transmitter which is transferred to the body as a function voltage. From the paper, it is clear that the output impedance is near about 400 Ω while the transmitting power is almost double compared with the conventional approach.

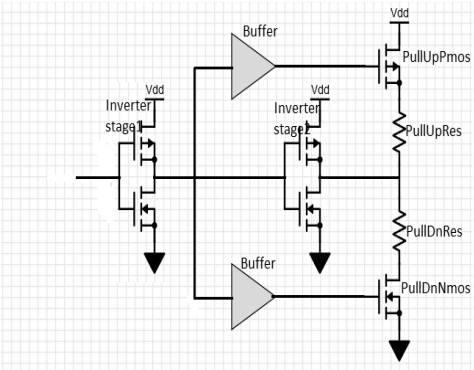

Figure 2: Basic architecture of the tri-state voltage mode driver circuit.

IV. TRANSISTOR LEVEL PERFORMANCE

The basic requirement of the driver is to drive a huge load capacitor hence it needs to draw at least 6 mA current. The transistor width need to high enough to draw that amount of current at the same time it increases the power consumption of the circuit. So, the sizing of the transistors is very crucial in respect to the driving capability and the power consumption. Usually 1 μm length draws 1 mA current. Actually the driver is formed by cascading of two inverter stage and an identical inverter with push-pull mechanism. In table 6, the sizing of the transistors are shown for the BCC,

Table 1: Sizing technique of the transistors in the driver chain

Inverter stage	Width (NMOS)	Value (μm)	Width (PMOS)	Value (μm)
Stage 1	$W_{nStage1}$	119	3* $W_{nStage1}$	357
Stage 2	2* $W_{nStage1}$	238	3*2* $W_{nStage1}$	714
Stage 3	3* $W_{nStage1}$	476	3*2*2*$W_{nStage1}$	1428

In table 1, it is shown that the width of the PMOS is three times with the NMOS of the same inverter. On the other hand, the width of the NMOS is two times with the preceding stage NMOS. Finally, the sizing technique improves the driving capability of the driver circuit. The length of the transistor is set to 195 nm which provides proper pulses at the transmitter. The DC analysis provides 6 mA current through the load capacitor with the above sizing technique.

In figure 3, the transistor level behavior is shown in the different nodes of the BCC system. Actually the entire system is run for 1μs only keeping the driver circuit in transistor level to observe the overall performance of the BCC. In figure 3, the results are input data, transmitter output, left and right i/o pads, input of the receiver and final receiver output respectively. The transistor level behavior is pretty similar to

the system level performance. Finally, the receiver detects the transmitted signal properly. The propagation delay of the transmitted signal is increased due to the large width of the transistors which adds more parasitic capacitance and resistance to the load. The propagation delay is measured 6.14 ns at 100 pF load which is increased by 0.26 ns compared to the calculated value.

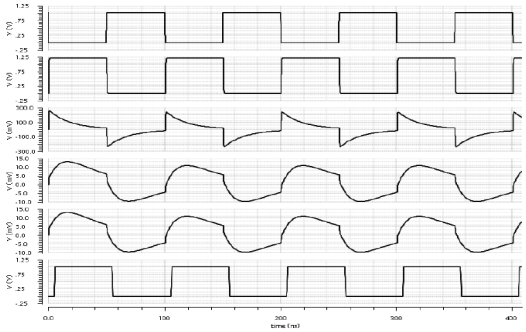

Figure 3: Transistor level performance at different nodes of the BCC

V. PERFORMANCE ANALYSIS

A. *Noise Analysis*

As the body attenuation is more than 60 dB, it is important to consider all possible noise sources. In the Tx side, there is no need of filter because the body acts as a low pass filter but the possible noise sources should be consider which can affect the original signal.

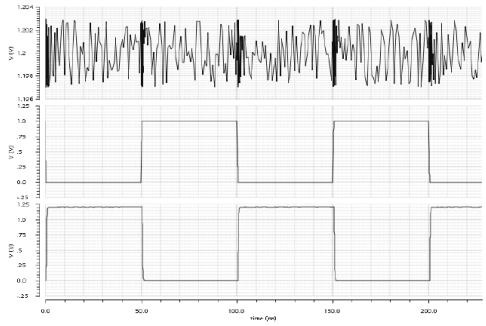

Figure 4: The waveform of the input data and transmitter output by adding 3 mV noise.

Figure 4 shows noise performance by adding 3 mV noise in the supply voltage of the proposed driver circuit. The effect of noise is significant to the output by adding the different level of noise to the transmitter. If the supply noise is increased, the propagation delay is also increased. And for this, the pulses need to be shaped. In addition, the signal cannot be recovered if noise more than 10 mV. So noise sensitivity of the transmitter is 10 mV.

B. *Eye diagram*

The eye diagram is a spontaneous graphical representation of the electrical signal for the high-speed digital data communication. In figure 5, the eye diagram is plotted for 30ns period with 10 mV supply noise. The cycle to cycle jitter and the long term jitter are main specifications for the BCC project. The cycle to cycle jitter is defined as the variation of the cycle time of a signal among the adjacent cycles over a random sample of adjacent cycle pairs [5]. Basically, the maximum deviation of the two rising edges of the two adjacent clocks are defined by the cycle to cycle jitter. In this case, the cycle to cycle is measured as 0.87% which meets the specification.

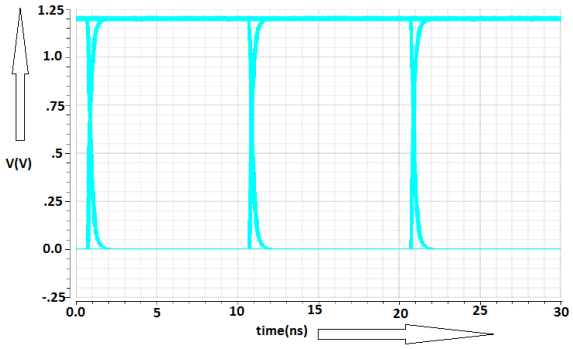

Figure 5: Eye diagram at 10 mV supply noise for 30 ns period.

Table 2: Showing results for eye diagram

Vertical eye opening	1.1 V
Horizontal eye opening	2.5 ns
Noise margin	0.25 V
Timing variation at zero crossing	0.55 ns
Eye level zero	5 mV
Eye level one	10 mV
Rise time	1.2 ns
Fall time	1.5 ns
Jitter	0.87%

In table 2, the different parameters are evaluated from the eye diagram. The two basic characteristics of the eye diagram are horizontal eye opening and vertical eye opening. In this case the horizontal eye opening is 2.5 ns and the vertical eye opening is 1.1 V. The timing variation at zero crossing indicates the amount of noise where the zero crossing occurs. The timing variation at zero crossing is measured as 0.55 ns. The noise margin is another important parameter for eye diagram and it gives 0.25 V. The rise time and the fall time are 1.2 ns and 1.5 ns respectively. The cycle to cycle jitter with respect to the data clock is 0.87% in this case.

C. *Corner analysis*

Corner analysis measures a circuit performance while under simulation stage with sets of parametric values which represents the worst case variations in manufacturing process. In this paper, the corner analysis is run over the variation of supply voltage, temperature and process. The supply voltage varies from 1 V to 1.4 V and temperature from -40 °C and 120 °C. The simulation is run for 9 process corners. So, the corner analysis is run for in total 9*3*3=81 points where 3 for supply voltage variation and another 3 for temperature variation.

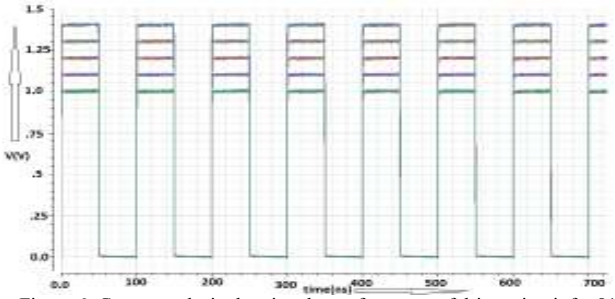

Figure 6: Corner analysis showing the performance of driver circuit for 81 corners.

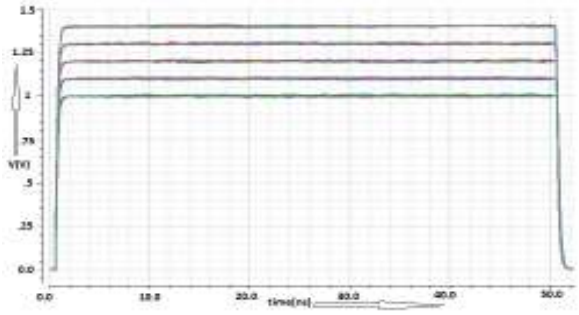

Figure 7: Corner analysis showing a single pulse of the transmitter.

In figure 6 and 7, it is clear that the circuit works for all 81 corners. In a corner analysis perspective the transmitter is performed properly. The digital signal can be decoded by the baseband after getting sampled in AFE. Basically the sampling frequency is eight times with the clock frequency. The clock frequency is 100 ns and thus a one can be detected very easily if its length is more than 12.5 ns. In general, the length of one and length of zero should be 50 ns. From figure 6, it is clear that the length of one is approximately 49 ns which can be easily detected by the baseband. The transmitted signal can be detected in receiver even for the worst case at 1.4 V and 120 °C. In addition, the sampling frequency may be 10 times to the clock frequency for better reorganization.

VI. RESULTS

The findings of the transmitter circuit are shown in table 3.

Table 3: The performance of the driver circuit

Parameters	**Value**
Technology	ST65 nm CMOS process
Supply Voltage	1.2 V
Operating Frequency	10 MHz
Power Consumption	7.398 mW
Propagation delay	6.14 ns
Jitter	0.87%
PSRR	65 dB
Acceptable supply noise	10 mV
Leakage power	1.954 µW or -27 dBm

In table 3, the signal strength has been increased as well as the driving capability due to attenuation factor of the body. Thus overall power consumption of the transmitter is quite high. The propagation delay is 6.14 ns which is quite a good number in respect to the parasitic effect to the load. The cycle to cycle jitter is lower than 1% which is acceptable. The power supply rejection ratio is very standard in this case which indicates the good noise performance. Leakage power is 1.94 µW which is considerably low.

VII. FUTURE WORK

The power consumption of the driver circuit is one of the main challenges. The requirement of high driving current via increased transistor size causes high power consumption. Reduced power buffer, RPB [6] can be used which introduces a storage capacitance C_S to recycle some of the charge normally discharged during each logic transition by load capacitor C_L. The power savings is related to the storage capacitor and the load capacitor. [Power savings (%) = C_S / (C_L + 2C_S)*100%]

Table 4: Power savings of the reduced power buffer (RPB)

C_S/C_L	Power savings (%)
0.25	16.70
1	33.30
4	44.40
∞	50.00

In table 4, the power savings is represented according to the ratio of storage capacitor and the load capacitor [7]. Thus the power consumption is reduced significantly for application dominated by switching of large capacitive load independent of the supply voltage.

ACKNOWLEDGMENT

We thank Dr. Jacob Wikner for his support in the completion of this paper.

REFERENCES

[1] S. Corroy, A. Argyriou, Z. Wadood, H. Baldus, " A Body-Coupled Communication and Radio Frequency Dual Technology Cooperation Protocol for Body-Area Networks" , in IEEE International Conference on Communications Workshops (ICC 2010): MAN, Cape Town, South Africa, May 2010.

[2] T.G. Zimmerman, "Personal Area Networks: Near-field intrabody communication," IBM Systems Journal, vol. 35, no. 3.4, pp. 609,617,1996.

[3] C. Zamarreno-Ramos, T. Serrano-Gotarredona, B. Linares-Barranco, "A 0.35 µm Sub-ns Wake-up Time ON-OFF Switchable LVDS Driver-Receiver Chip I/O Pad Pair for Rate-Dependent Power Saving in AER Bit-Serial Links,"*Biomedical Circuits and Systems, IEEE Transactions on*, vol.6, no.5, pp.486,497, Oct. 2012.

[4] S. Song, N.Cho, and H. Yoo, " A 0.2mW 2Mbps Digital Transceiver Based on Wideband Signaling for Human Body Communications," in IEEE Journal of Solid State Circuits, Vol. 42, No. 9, September 2007, pp. 2021-2033.

[5] Eduard Sackinger, "Broadband Circuits for Optical Fiber Communications" John Wiley & Sons INC, 2005.

[6] J. Ridenour, Hu Jianghai, N. Pettis, Lu Yung Hsing "Low-power buffer management for streaming data", IEEE transactions on circuits and systems for video technology, vol:17, issue: 2, pages 143-157, February 2007.

[7] M. Hahm, "Modest power savings for applications dominated by switching of large capacitive loads," Low Power Electronics, Digest of Technical Papers, IEEE Symposium, pp. 60-61, 10-12 Oct, 1994.