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Multiplexer(MUX) and Multiplexing

JULY 20, 2015 BY ADMINISTRATOR — 8 COMMENTS

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Multiplexer

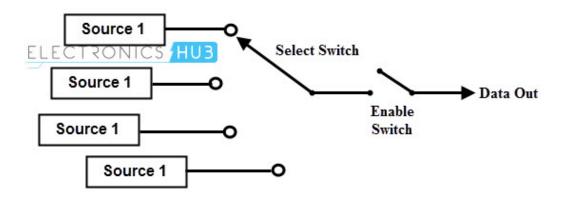
Multiplexing is the property of combining one or more signals and transmitting on a single channel. This is achieved by the device multiplexer. A multiplexer is the most frequently used combinational circuits and important building block in many in digital systems.

These are mostly used to form a selected path between multiple sources and a single destination. A basic multiplexer has various data input lines and a single output line. These are found in many digital system applications such as data selection and data routing, logic function generators, digital counters with multiplexed displays, telephone network, communication systems, waveform generators, etc. In this article we are going to discuss about types of multiplexers and its design.

What is a Multiplexer?

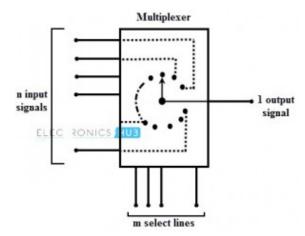
The multiplexer or MUX is a digital switch, also called as data selector. It is a combinational circuit with more than one input line, one output line and more than one select line. It allows the binary information from several input lines or sources and depending on the set of select lines, particular input line, is routed onto a single output line.

The basic idea of multiplexing is shown in figure below in which data from several sources are routed to the single output line when the enable switch is ON. That is how the multiplexers are also called as 'many to one' combinational circuits.



The below figure shows the block diagram of a multiplexer consisting of n input lines, m selection lines and one output line. If there are m selection lines, then the number of possible input lines is 2m. Alternatively we can say that if the number of input lines is equal to 2m, then m selection lines are required to select one of n (consider 2m = n) input lines.

This type of multiplexer is referred to as $2n \times 1$ multiplexer or 2n -to-1 multiplexer. For example, if one of the 4 input lines has to be selected, then two select lines are required. Similarly, to select one of 8 input lines, three select lines are required.



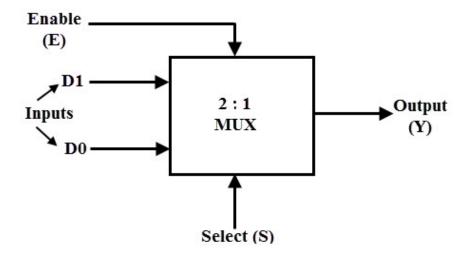
Generally the number of data inputs to a multiplexer is a power of two such as 2, 4, 8, 16, etc. Some of the mostly used multiplexers include 2-to-1, 4-to-1, 8-to-1 and 16-to-1 multiplexers.

These multiplexers are available in IC forms with different input and select line configurations. Some of the available multiplexer ICs include 74157 (2-to-1 MUX), 78158 (2-to-1 MUX), 74352 (4-to-1 MUX), 74153 (4-to-1 MUX), 74152 (8-to-1 MUX) and 74150 (16-to-1 MUX).

2-to-1 Multiplexer

A 2-to-1 multiplexer consists of two inputs Do and D1, one select input S and one output Y. Depends on the select signal, the output is connected to either of the inputs. Since there are two input signals only two ways are possible to connect the inputs to the outputs, so one select is needed to do these operations.

If the select line is low, then the output will be switched to D0 input, whereas if select line is high, then the output will be switched to D1 input. The figure below shows the block diagram of a 2-to-1 multiplexer which connects two 1-bit inputs to a common destination.



The truth table of the 2-to-1 multiplexer is shown below. Depending on the selector switching the inputs are produced at outputs , i.e., D0 , D1 and are switched to the output for S=0 and S=1 respectively . Thus, the Boolean expression for the output becomes D0 when S=0 and output is D1 when S=1.

From the truth table the Boolean expression of the output is given as

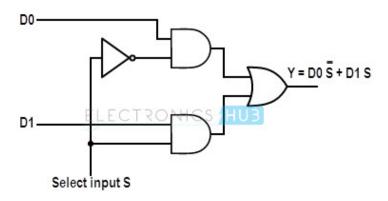
$$Y = D_0 \overline{S} + D_1 S$$

Select	Inp	Output	
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1

From the above output expression, the logic circuit of 2-to-1 multiplexer can be implemented using logic gates as shown in figure. It consists of two AND gates, one NOT gate and one OR

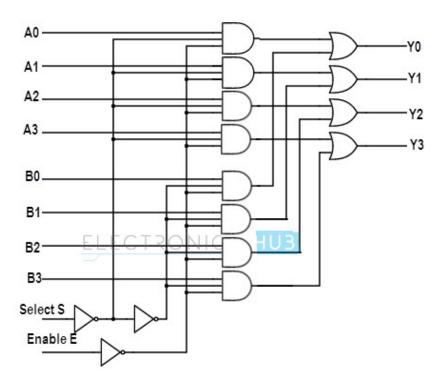
gate. When the select line, S=0, the output of the upper AND gate is zero, but the lower AND gate is Do.

Thus, the output generated by the OR gate is equal to Do. Similarly, when S=1, the output of the lower AND gate is zero, but the output of upper AND gate is D1. Therefore, the output of the OR gate is D1. Thus, the above given Boolean expression is satisfied by this circuit.



In some cases, two or more multiplexers are fabricated on a single IC because simple logic gates can implement the multiplexer. Generally four 2 line to 1 line multiplexers are fabricated in a single IC as shown in figure below. Some of these ICs of 2 to 1 multiplexers include IC 74157 and IC 74158. The selection line controls the input lines to the output in all four multiplexers.

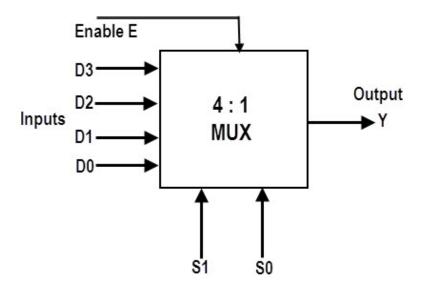
The output Y1 can be selected such that its value may be equal to A1 or B1, Y2 can be either A2 or B2 and so on. The control input E enables and disables all the multiplexers, i.e., when E=1, outputs of all the multiplexer is zero irrespective of the value of S



4-to-1 Multiplexer

A 4-to-1 multiplexer consists four data input lines as Do to D3, two select lines as So and S1 and a single output line Y. The select lines S1 and S2 select one of the four input lines to connect the output line. The particular input combination on select lines selects one of input (D0 through D3) to the output.

The figure below shows the block diagram of a 4-to-1 multiplexer in which the multiplexer decodes the input through select line.



The truth table of a 4-to-1 multiplexer is shown below in which four input combinations 00, 10, 01 and 11 on the select lines respectively switches the inputs D0, D2, D1 and D3 to the output. That means when S1=0 and S0 =0, the output at Y is D0, similarly Y is D1 if the select inputs S1=0 and S0=1 and so on.

Select Da	Select Data Inputs		
S ₁	S ₀	Y	
0	0	D ₀	
0	1	D ₁	
1	0	D ₂	
1	1	D ₃	

From the above truth table, we can write the output expressions as

If S1=0 and S0=0 then Y = D0

Therefore, Y = Do (S1) (S0)

If S1= 0 and S0=1, the Y = D1

Therefore, Y = D1 (S1) So

If S1=1 and S0=0, then Y = D2

Therefore, Y = D2 S1 (S0)

If S1=1 and S0=1 the Y = D3

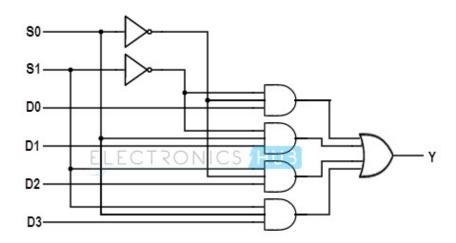
Therefore, Y = D3 S1 S0

To get the total data output from the multiplexer, all these product terms are to be summed and then the final Boolean expression of this multiplexer is given as

$Y = D0 \overline{S1} \overline{S0} + D1 \overline{S1} S0 + D2 S1 \overline{S0} + D3 S1 S0$

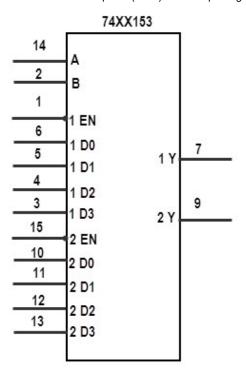
From the above expression of the output, a 4-to-1 multiplexer can be implemented by using basic logic gates. The below figure shows the logic circuit of 4:1 MUX which is implemented by four 3-inputs AND gates, two 1-input NOT gates, and one 4-inputs OR gate.

In this circuit, each data input line is connected as input to an AND gate and two select lines are connected as other two inputs to it. The AND gate output is connected to with inputs of OR gate so as to produce the output Y.



Generally, this type of multiplexers is available in dual IC forms and most common type is IC 74153 which is a dual 4-to-1 line multiplexer. It consists of two identical and independent 4-to-1 multiplexers. It has two separate enable or strobe inputs to switch ON or OFF the multiplexers.

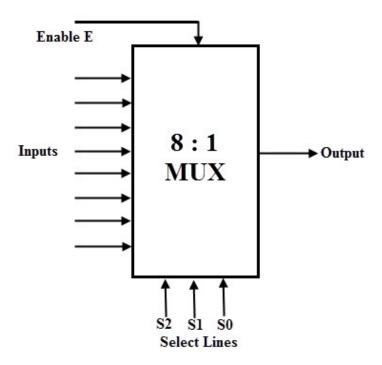
Usually, the enable input or strobe can be used to cascade two or more multiplexer ICs to construct a multiplexer with large number of inputs. Each multiplier is supplied with separate inputs. The figure below shows the pin diagram of IC74153.



8-to-1 Multiplexer

An 8-to-1 multiplexer consists of eight data inputs Do through D7, three input select lines S2 through So and a single output line Y. Depending on the select lines combinations, multiplexer decodes the inputs.

The below figure shows the block diagram of an 8-to-1 multiplexer with enable input that enable or disable the multiplexer. Since the number data bits given to the MUX are eight then 3 bits (23=8) are needed to select one of the eight data bits.



The truth table for an 8-to1 multiplexer is given below with eight combinations of inputs so as to generate each output corresponds to input.

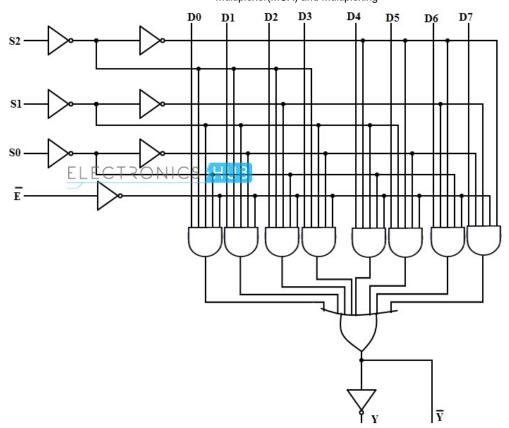
For example, if S2= 0, S1=1 and S0=0 then the data output Y is equal to D2. Similarly the data outputs D0 to D7 will be selected through the combinations of S2, S1 and S0 as shown in below figure.

Se	Select Data Inputs			
S ₂	S ₁	S ₀	Y	
0	0	0	D ₀	
0	0	1	D ₁	
0	1	0	D ₂	
0	1	1	D ₃	
1	0	0	D ₄	
1	0	1	D ₅	
1	1	0	D ₆	
1	1	1	D ₇	

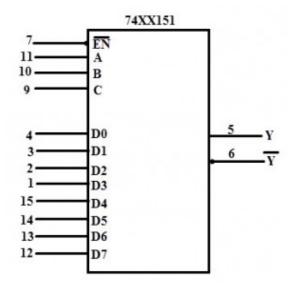
From the above truth table, the Boolean equation for the output is given as

$$Y = D0 \overline{S2} \overline{S1} \overline{S0} + D1 \overline{S2} \overline{S1} S0 + D2 \overline{S2} S1 \overline{S0} + D3 \overline{S2} S1 S0 + D4 S2 \overline{S1} \overline{S0} + D5 S2 \overline{S1} S0 + D6 S2 S1 \overline{S0} + D7 S2 S1 S0$$

From the above Boolean equation, the logic circuit diagram of an 8-to-1 multiplexer can be implemented by using 8 AND gates, 1 OR gate and 7 NOT gates as shown in below figure. In the circuit, when enable pin is set to one, the multiplexer will be disabled and if it is zero then select lines will select the corresponding data input to pass through the output.



A typical IC 74151 is an 8-to-1 multiplexer with eight inputs and two outputs. The two outputs are active low and active high outputs. It has three select lines A, B and C and one active low enable input. The pinout of this IC is given below.



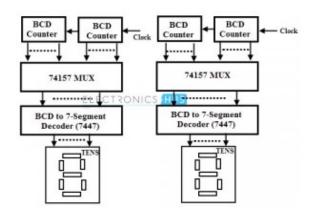
Application of Multiplexer

In all types of digital system applications, multiplexers find its immense usage. Since these allows multiple inputs to be connected independently to a single output, these are found in

variety of applications including data routing, logic function generators, control sequencers, parallel-to-serial converters, etc.

Data Routing

Multiplexers are extensively used in data routing applications to route the data to a one particular destination from one of several sources. One of the applications includes the displaying of two multidigit BCD counters, one at a time. In such application, 74157 multiplexer ICs are used to select and display the content of either of two BCD counters using a set of decoder and LED displays.



Logic Function Generator

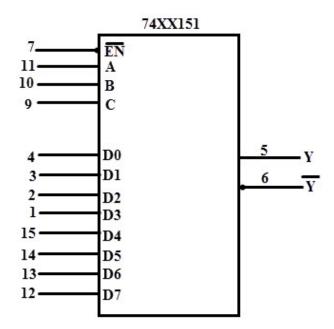
In place of logic gates, a logical expression can be generated by using a multiplexer. It is possible to connect the multiplexer such that it duplicates the logic of any truth table. In such cases it can generate the Boolean algebraic function of a set of input variables.

This abruptly reduces the number of logic gates or integrated circuits to perform the logic function since the multiplexer is a single integrated circuit. In this kind of applications, multiplexers are viewed as logic function generators.

For example consider the below logic diagram to implement the ex-OR function of three inputs. A 74151A 8-to-1 multiplexer is used in this logic generator. This multiplexer works exactly similar to the set of logic gates implementing the same function.

The output F is 1 for data inputs D1, D2, D5 and D6 which are selected by making selection lines to 001, 010, 100 and 111 respectively.

Sele	ect Data In	Y = A ⊕ B ⊕ C	
S ₂	S ₁	S ₀	1-АФРФС
Α	В	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



Parallel to Serial Conversion

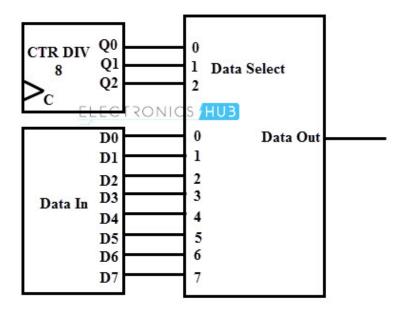
A multiplexer circuit can be used to convert the parallel data to serial data, so as to reduce parallel buses to serial signals. This type of conversion is needed in telecommunication, test and measurement, military/aerospace, data communications applications.

In digital systems, mostly data processed in parallel for achieving higher speeds. But for transmission of the data signals over long distances need more number of lines to process the data. In such cases parallel data is converted into serial form using multiplexers.

The figure below shows the parallel to serial data conversion using an 8 input multiplexer. Parallel data from the data in or some other register is applied to the 8 input lines of the

multiplexer.

The selection codes for the multiplexer are generated by a 3-bit counter. With the application of each clock pulse to the counter the data is serially out from the multiplexer.



Other applications of multiplexers include control sequencers, pulse train generators, encoders, register to register data transfer, waveform generators, etc.

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