Rakesh Bhatia

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Education

University of California, Santa Barbara (UCSB) Graduated in March 2014

- M.S. in Computer Engineering
- Major: Very Large Scale Integration (VLSI) and Computer Aided Design (CAD); Minor: Computer Architecture
- Cumulative GPA: 3.88
- Completed Courses:
  - *CS 240A*, Applied Parallel Computing
  - *CS 254*, Advanced Computer Architecture
  - *ECE 220B*, Semiconductor Device Processing
  - *ECE 224A*, VLSI Project Design
  - *ECE 225*, High Speed Digital Integrated Circuit Design
  - *ECE 254B*, Advanced Computer Architecture: Parallel Processing
  - *ECE 255B*, VLSI Design Validation
  - *ECE 256A*, Introduction to Logic Design Automation
  - *ECE 279*, Computer Systems Performance Evaluation
  - *ENGR 240*, Business Strategy
  - *ENGR 241*, Managing Innovation
  - *ENGR 255*, New Product Development

Stanford University September 2011 - March 2012

- Took courses through the Stanford Center for Professional Development
- Cumulative GPA: 3.35
- Courses taken:
  - *EE 214A*, Fundamentals of Analog Integrated Circuit Design
  - *EE 214B*, Advanced Analog Integrated Circuit Design

University of California, Los Angeles (UCLA) Graduated in March 2010

- B.S. in Electrical Engineering with a pathway in Signals and Systems
- Cumulative GPA: 3.27

Work Experience

Analog Engineer, **Intel Corporation** March 2014 – Present

- Worked on a variety of validation projects for DDR3/DDR4 memory in the Mem-IP group
- Managed System Verilog behavioral models (BMODs) for several different circuit blocks in the analog front end (AFE)
- Ran BMOD vs. SCH simulations for these blocks to ensure BMODs accurately capture analog circuit behavior
- Ran mixed-signal validation (MSV) simulations for various blocks in the AFE using VCS+XA (ACE-XA) simulation tool
- Completed various POLO simulations for DNV blocks, utilizing Cadence testbenches and extracted views for the block being tested
- Developed python scripts for post-silicon validation on the DNV monitor port block
- Developed a perl script for extracting critical IP drop information from Central Runs
- Also continued work from internship on analog fault injection and reduction methods for MSV
- Made enhancements to C++ software methodology for improving efficiency of high-volume manufacturing (HVM) tests
- Utilized the methodology to analyze the effects of open/short faults in high-speed serial I/O circuits
- Used Virtuoso Cadence environment to analyze circuit schematics, extract SPICE netlists, and extract layout parasitics
- Ran full lane-level simulations of high-speed I/O's in the presence of faults, using Synopsys' VCS+XA simulator
- Worked on integrating the above software into a new Hardware Development Kit being created at Intel

Software Engineering Intern, **Intel Corporation** June 2013 – December 2013

- Developed a SPICE netlist parser and analog fault injection flow in C++, using existing data structures
- Designed a hierarchy file generator (using a breadth-first search algorithm) for pulling hierarchy information from a SPICE netlist
- Used the flow to perform fault injection and reduction on various analog blocks in a high-speed serial interface circuit
- Utilized the XA (fast SPICE) simulator to simulate and analyze the output waveforms in the presence of faults
- Learned about a variety of other tools, including Scarlet (for parasitics extraction), and nWave (for viewing XA simulation results)

Awards & Additional Information

- Named to Dean's Honors List at UCLA with a 4.0 GPA in the Fall quarter of 2009
- Winner of the 19th annual Dr. Martin Luther King, Jr. Oratorical Contest held at UCLA in January 2007
- Received certificate of completion for System Verilog training from Doulos, sponsored by Intel
- Knowledge of C++ programming and MATLAB
- US Citizen and qualified to work in the United States