Rakesh Pandey

M.Tech+Ph.D., CSE, IIT Guwahati

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I am a Dual Degree (M.Tech + Ph.D.) student in the Dept. of CSE, IIT Guwahati. I have submitted my Ph.D. thesis in Sep 2019. My research specializations are in Computer Architecture. Specifically, focused to reduce the execution time and power requirement of the chip-multiprocessor systems.

Education

- **Dual-Degree (M.Tech+Ph.D),** Department of Computer Science and Engineering, *Indian Institute of Technology (IIT) Guwahati*, India.
  - Thesis Topic: "Efficient Mapping of Multi-threaded Workloads on to Large Chip-Multiprocessors".
  - *Ph.D:* Computer Architecture (**Thesis Submitted**)
  - *M.Tech:* Computer Science and Engineering, 7.04 CPI.
  - Advisor: Dr. A. Sahu (Associate Professor).
- **B.Tech:** Electronics and Communication Engineering, *UPTU*, Lucknow, India, *70.98* %.
- **12th:** U.P. Board Allahabad, India, *75.6* % *(Honours)*.
- **10th:** U.P. Board Allahabad, India, *62.83* % .

Research Publications

- Rakesh Pandey, Aryabartta Sahu. *Efficient mapping of Multi-threaded Applications onto 3D-stacked Chip-Multiprocessor*, in 19th IEEE International Conference on High Performance Computing and Communications (**HPCC-2017, EI Index, Core Ranking B**).
- Rakesh Pandey, Aryabartta Sahu. *Access-Aware Self-adaptive Data Mapping onto 3D-stacked Hybrid DRAM-PCM based Chip-Multiprocessor*, in 21st IEEE International Conference on High-Performance Computing and Communications (**HPCC-2019, EI Index, Core Ranking B**).
- Rakesh Pandey, Aryabartta Sahu. *Performance and Area Trade-off of 3D-stacked Chip-Multiprocessor with Hybrid Interconnect*, in IEEE Transaction of Emerging Topics and Computing **(Accepted for Publication, Impact factor 4.98)**.
- Rakesh Pandey, Aryabartta Sahu. *Run-time Self-Adaptive Data Page Mapping on Chip-Multiprocessor*, in Elsevier Journal of System Architecture (Under Review).
- Rakesh Pandey and Aryabartta Sahu, *Adaptive Data Page Mapping onto 3D Stacked Chip- Multiprocessor With Multiple Memory Controllers and Channels*, in Elsevier Journal of System Architecture (Submitted).

Experience

- **Teaching Assistant:** at IIT Guwahati.
  - CS461: Computer Graphics.
  - CS101: Introduction to Computing and CS110: Computing Lab.
  - CS349: Networks Lab.
  - CS512: Data Structures and Algorithms.
  - CS321: Hardware and Peripherals Lab.
  - CS431: Programming Language Lab.
  - CS203: Formal Languages and Automata Theory.
  - CS241: System Software Lab.
- **Summer Intern:** at ITI Ltd.,Mankapur, U.P.
  - Carried out analysis of BSNL BTS, Note-counting Machine, and their PCBs manufacturing process. Gained experience from real working environment of a Public Sector Unit (PSU).

Projects

- **Terrain Mapping Robot**: Used an autonomous Robot to map the real-time environment by using GPS and Ultrasonic sensors. Map generated is used by another Robot, that is unaware about the environment, for the movement. In this project we have used Mobile Agent.
- **Serial Task Completion**: Developed an autonomous Robot driven using Mobile Agents.
- **Security System With Dialup Logic**: Developed this project to detect the security breach. Further, it automatically dials a mobile number to inform about the breach.
- **Web Portal for Report submission and Teacher-Student Interaction**: Developed a PHP based web application that would allow students to submit their final project report online. They can also view the PDF version of their report.

Computer skills

- **Languages:** C, C++, Prolog, HTML, PHP, Cilk, Pthread, OpenMP, 8085-Assembly Language Programming, Basics of Verilog.
- **Scripting:** Shell, Python
- **Simulator tools:** Multi2Sim, and Sniper6.1 simulators.
- **Application tools:** LaTeX, gnuplot, Xilinx, and Pintool.
- **Operating Systems:** Linux, Windows.

Miscellaneous

- Qualified Graduate Aptitude Test in Engineering (GATE) 2012 (95.6 Percentile) and 2013 (98.8 Percentile).
- Carried out *Session Chair's* responsibility at IEEE HPCC-2019, Zhangjiajie, China.
- Research *Paper Reviewer* for 16^th IEEE ICIT-2017.
- Event manager at 20th IEEE International Symposium on VLSI Design and Test (VDAT-2016), IIT Guwahati.
- Participated in Research Scholars Workshop organized by Student Affair Board at IIT

Guwahati.

- Participated in the cricket team and, the football team in Spardha-2016, the Inter Hostel Sports Competition, IIT Guwahati.

Talk

Title - **Multi-threaded Application Mapping onto CMP to improve the Overall Communication Cost**, in TEQIP-III Sponsored 5-day Short Term Course on Advanced Computer Architecture at Dept. CSE IIT Guwahati.

Declaration

I at this moment declare that all the details furnished above are true to the best of my knowledge and belief.