Verilog code:

```
module mp_2(input  reset,s1,s2,clk,output reg r,g,switch,
                    output reg [1:0]count);
localparam IDLE=2'd0,ENTRY=2'd1,EXIT=2'd2;
//output reg [1:0]count;
reg [1:0]ps,ns;
initial
  begin
    count=2'd0;
  end
always @ (posedge clk)
begin
  if(reset)
    begin
       ps<=IDLE;
    end
  else
    begin
        ps<=ns;
    end
end
always@ (s1,s2,ps)
begin
    case(ps)
       IDLE: begin
               if(s1==1'b1)
                  begin
                    if(s2==1'b1)
```

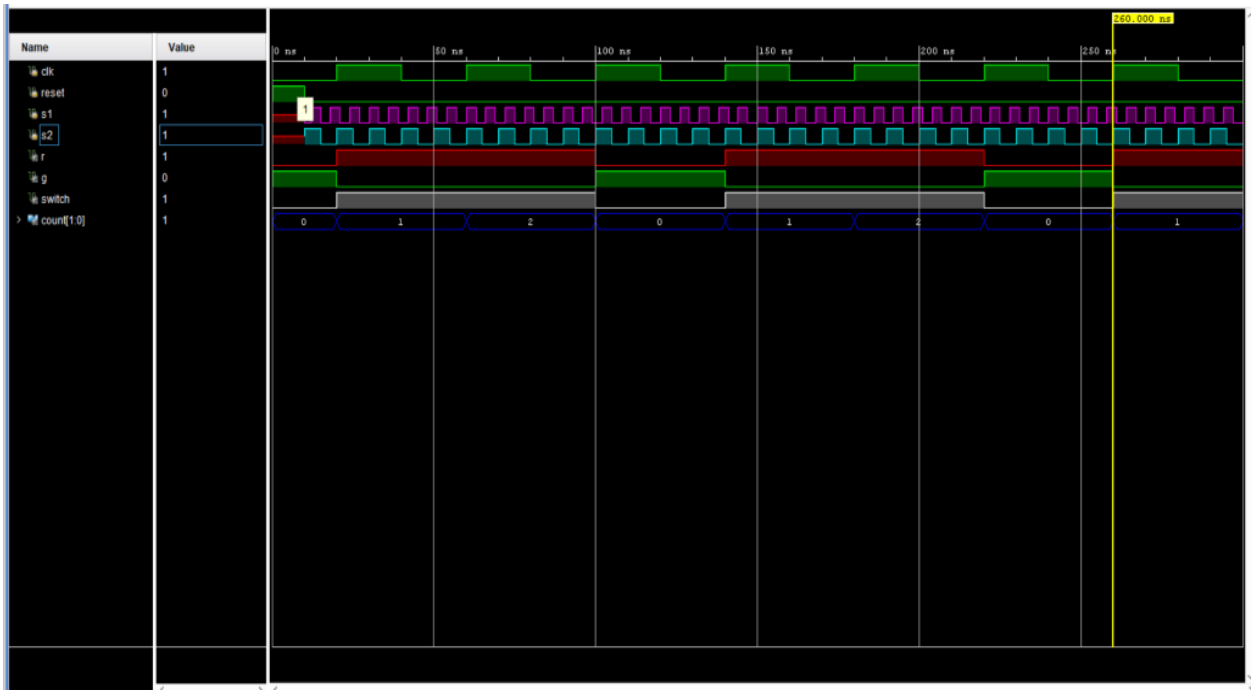
```
                    begin
                     ns=ENTRY;
                    end
                  end
            end
        ENTRY:begin
                  if(s2==1'b1)
                    begin
                      if(s1==1'b1)
                        begin
                          ns=EXIT;
                        end
                    end
                end
        EXIT:begin
                   if(s1==1'b0||s2==1'b0)
                      ns=IDLE;
               end
        default: ns=IDLE;
    endcase
end
always@(posedge clk)
begin
 if(r)
       count=count+1;
    else
      count=1'd1;
  end
 always @(ns,count)
```

```
begin
    case(ns)
      IDLE:begin
       if (count==2'd2)
        begin
            g=1'b1;r=1'b0;switch=1'b0;
             count=2'd0;
        end
         end
      ENTRY:begin
             r=1'b1;g=1'b0;switch=1'b1;
            if (count==2'd3)
                    begin
                     g=1'b1;r=1'b0;switch=1'b0;
                     count=2'd0;
                    end
          end
      EXIT:begin
           if (count==2'd3)
                          begin
            g=1'b1;r=1'b0;switch=1'b0;
                            count=2'd0;
                          end
        end
      default:begin
            r=1'b0;
            g=1'b1;
            switch=1'b0;
           end
```

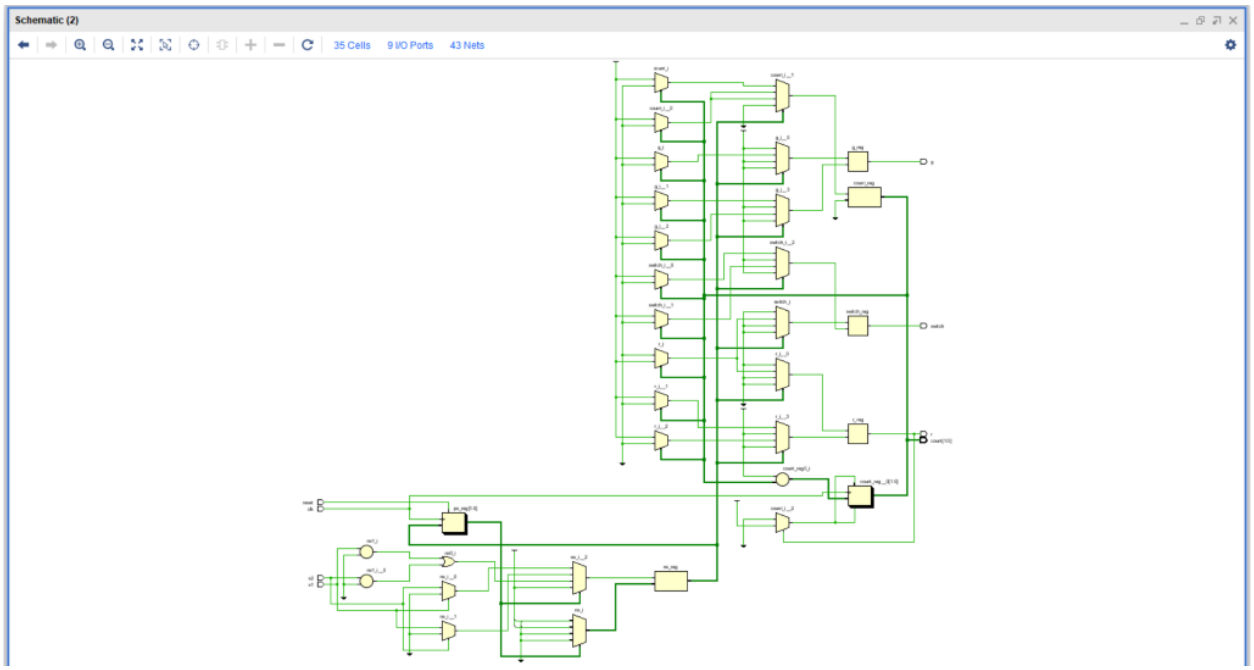
```
    endcase
        end
endmodule
```

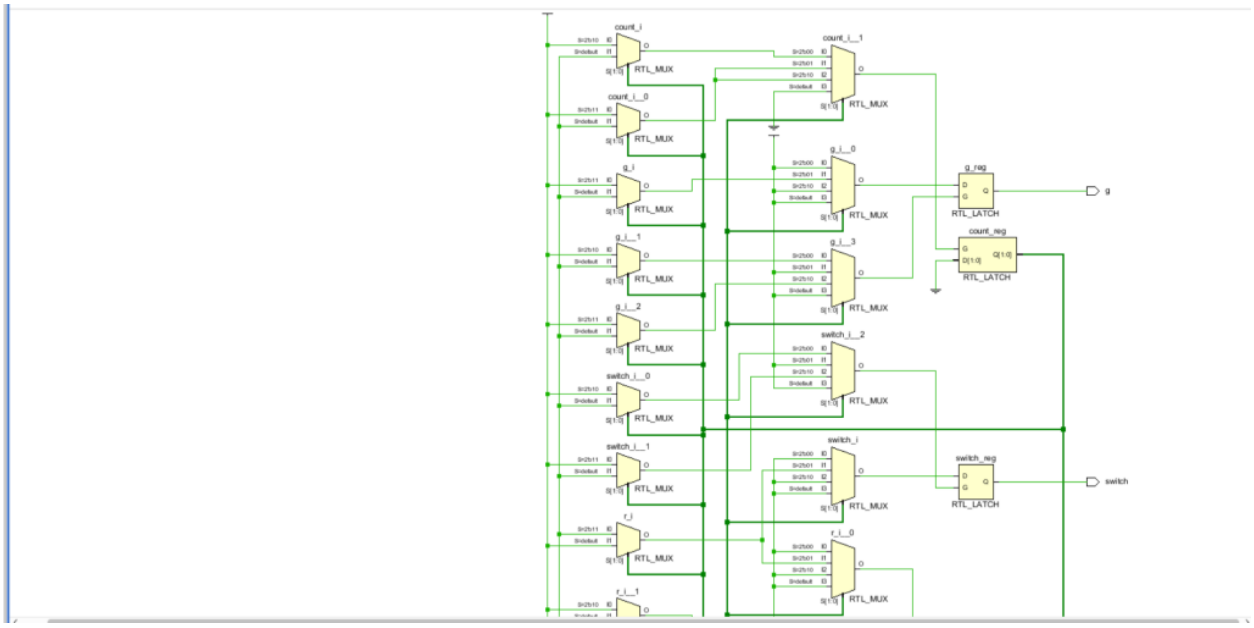
Results:

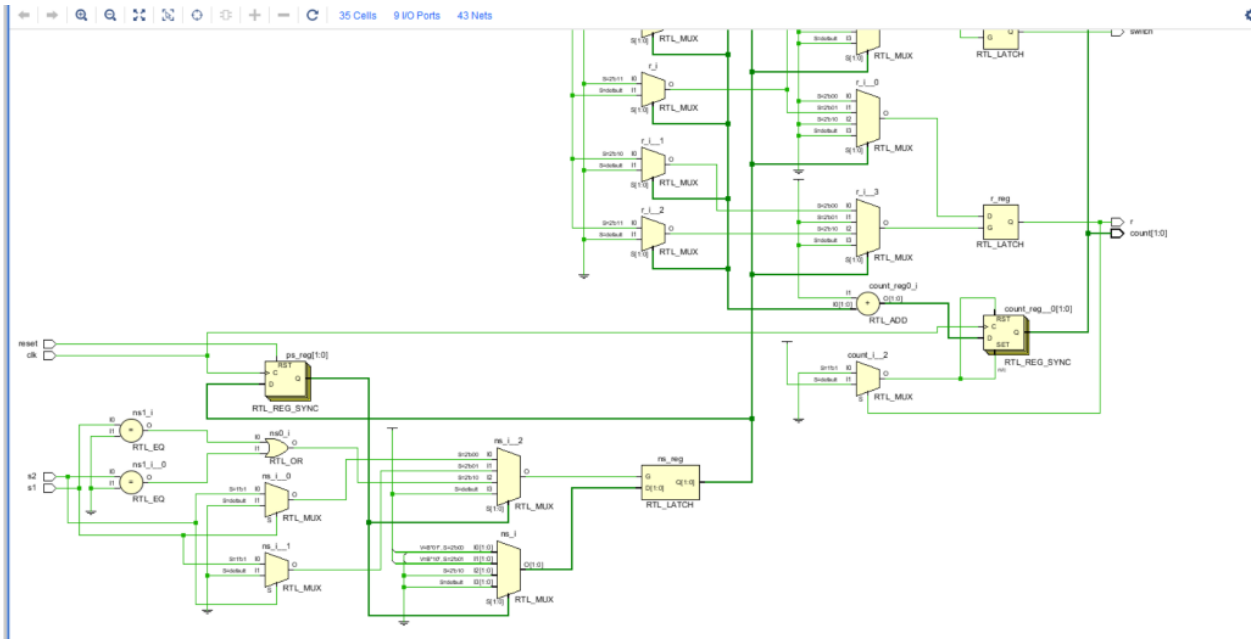
Simulation Results:



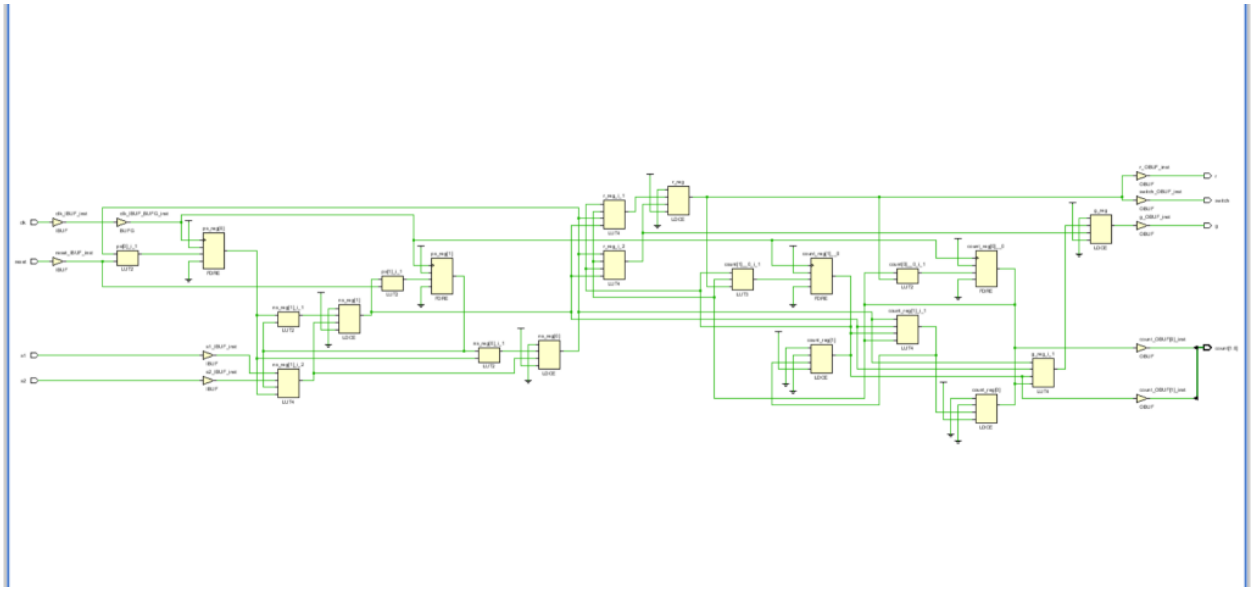
RTL schematic:

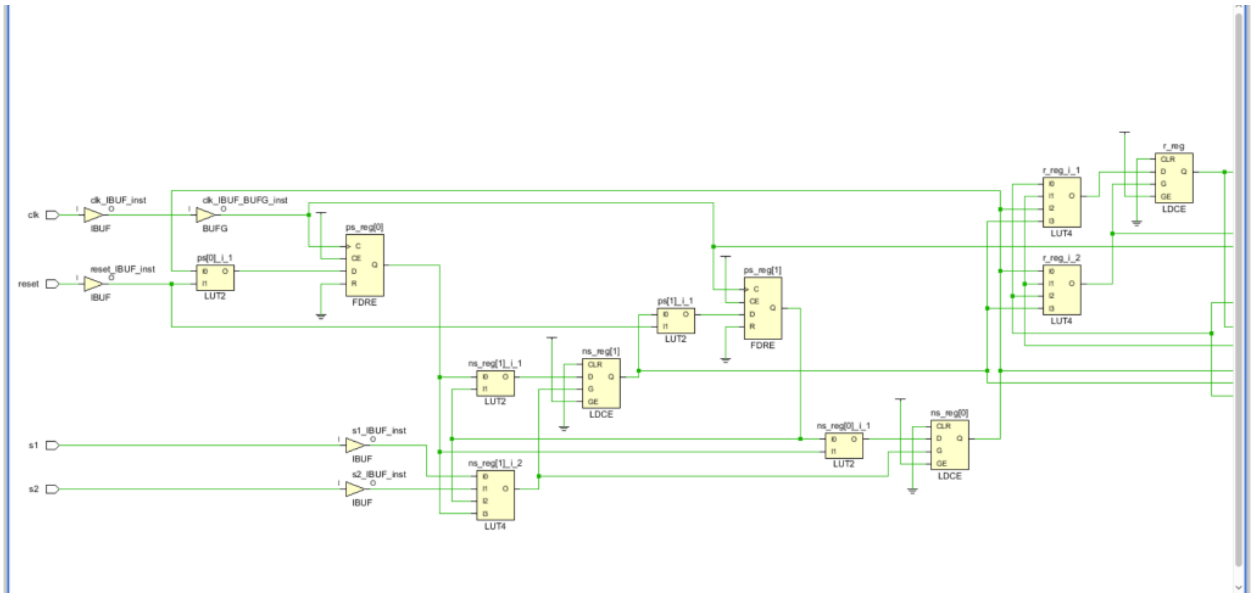

Schematic (2)
35 Cells
9 I/O Ports
43 Nets

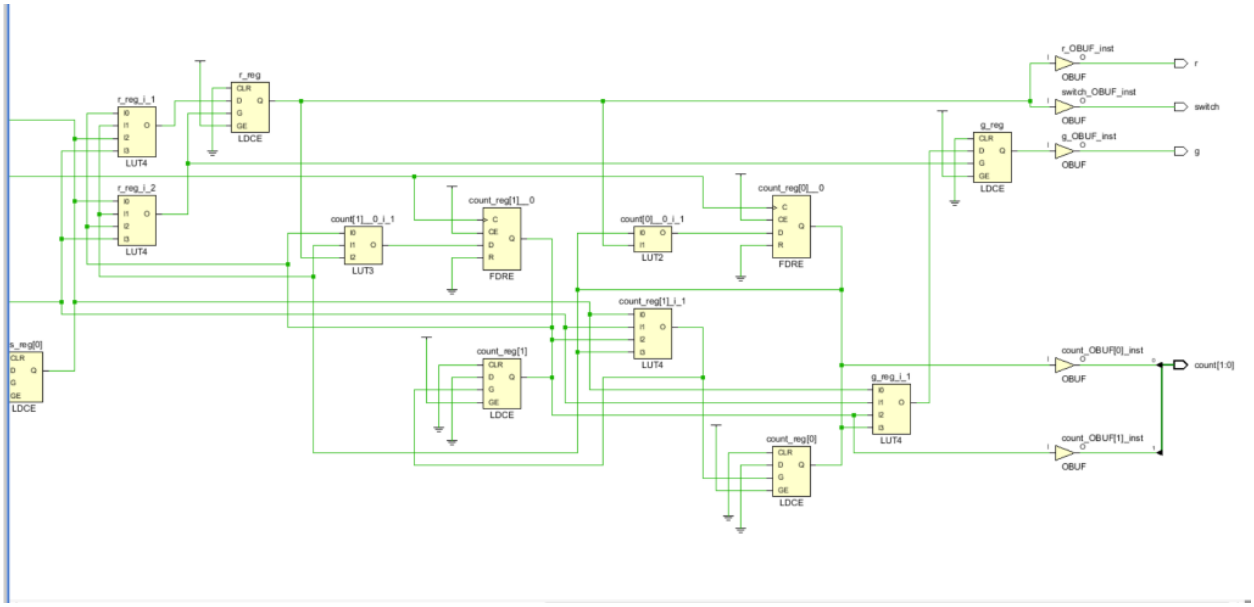

count_i
count_i__1
count_i__0
g_i
g_i__0
g_reg
g
RTL_LATCH
g_i__1
count_reg
g_i__3
RTL_LATCH
g_i__2
switch_i__2
switch_i__0
switch_i
switch_i__1
switch_reg
switch
RTL_LATCH
r_i
r_i__0
r_i__1
RTL_MUX



Synthesis Report:




clk
clk_IBUF_inst
IBUF
clk_IBUF_BUFG_inst
BUFG
reset
reset_IBUF_inst
IBUF
ps[0]_i_1
LUT2
ps_reg[0]
FDRE
ps[1]_i_1
LUT2
ps_reg[1]
FDRE
ns_reg[1]_i_1
LUT2
ns_reg[1]
LDCE
s1
s1_IBUF_inst
IBUF
s2
s2_IBUF_inst
IBUF
ns_reg[1]_i_2
LUT4
ns_reg[0]_i_1
LUT2
ns_reg[0]
LDCE
r_reg_i_1
LUT4
r_reg
LDCE
r_reg_i_2
LUT4


r_reg_i_1
LUT4
r_reg
LDCE
r_reg_i_2
LUT4
count[1]_0_i_1
LUT3
count_reg[1]_0
FDRE
count[0]_0_i_1
LUT2
count_reg[0]_0
FDRE
count_reg[1]_i_1
LUT4
s_reg[0]
LDCE
count_reg[1]
LDCE
count_reg[0]
LDCE
g_reg_i_1
LUT4
g_reg
LDCE
r_OBUF_inst
OBUF
r
switch_OBUF_inst
OBUF
switch
g_OBUF_inst
OBUF
g
count_OBUF[0]_inst
OBUF
count_OBUF[1]_inst
OBUF
count[1:0]