RISC_V-REPORT

Run file

#library creation

create_lib -technology ../../ref/tech/saed32nm_1p9m.tf -ref_libs \

{../../ref/CLIBs/saed32_1p9m_tech.ndm ../../ref/CLIBs/saed32_hvt.ndm \

../../ref/CLIBs/saed32_lvt.ndm ../../ref/CLIBs/saed32_rvt.ndm \

../../ref/CLIBs/saed32_sram_lp.ndm} risc_v1_extra

#reading netlist and SDC

read_verilog ../netlist/risc.v

read_sdc /home/BPD11/DNraKesh/Project/RISC_V_pn_2222/constraints/risc_sdc2.sdc

#floor plan

link_design

initialize_floorplan -side_ratio {2 4} -core_offset {1}

#parasitic reading

read_parasitic_tech -name {new_model} -tlup {../../ref/tech/saed32nm_1p9m_Cmin.lv.tluplus} -layermap \

{../../ref/tech/saed32nm_tf_itf_tluplus.map}

current_corner default

set_parasitic_parameters -early_spec new_model -late_spec new_model

set_process_number 0.99 -corners default

set_temperature 125 -corners default

set_voltage 0.75 -corners default

current_mode default

read_sdc ../constraints/risc_sdc2.sdc

```
set_scenario_status default -active true -setup true -hold true -max_transition true -max_capacitance true -min_capacitance true -leakage_power true  \
-dynamic_power true

#placement
place_pins -self
set_app_options -name place.coarse.fix_hard_macros -value false
set_app_options -name plan.place.auto_create_blockages -value auto
create_placement -timing_driven -congestion
legalize_placement

#clock route
set_app_options -name time.remove_clock_reconvergence_pessimism -value true
report_clock_settings
report_qor -summary
clock_opt

#routing
#set_routing_rule all -clear -default_rule -min_routing_layer 1 -max_routing_layer 9
route_auto -max_detail_route_iterations 30
route_opt
route_eco

#signoff_check_drc -auto_eco true
check_lvs
save_block
#script writing
write_script -force -format icc2 -output ../reports/router_spef
write_parasitics -output ../reports/spef_generation_1
```

write_sdf ../results/router_1.sdf

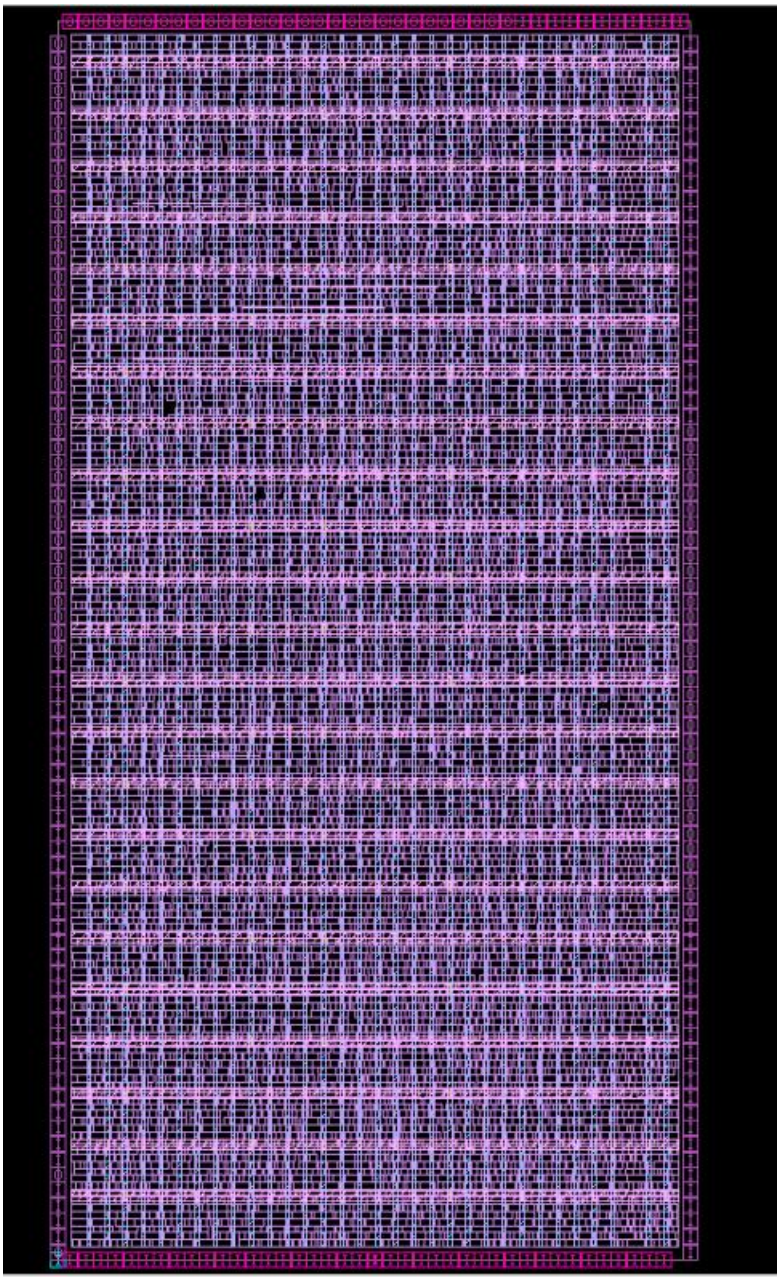
write_verilog ../results/router_1.v

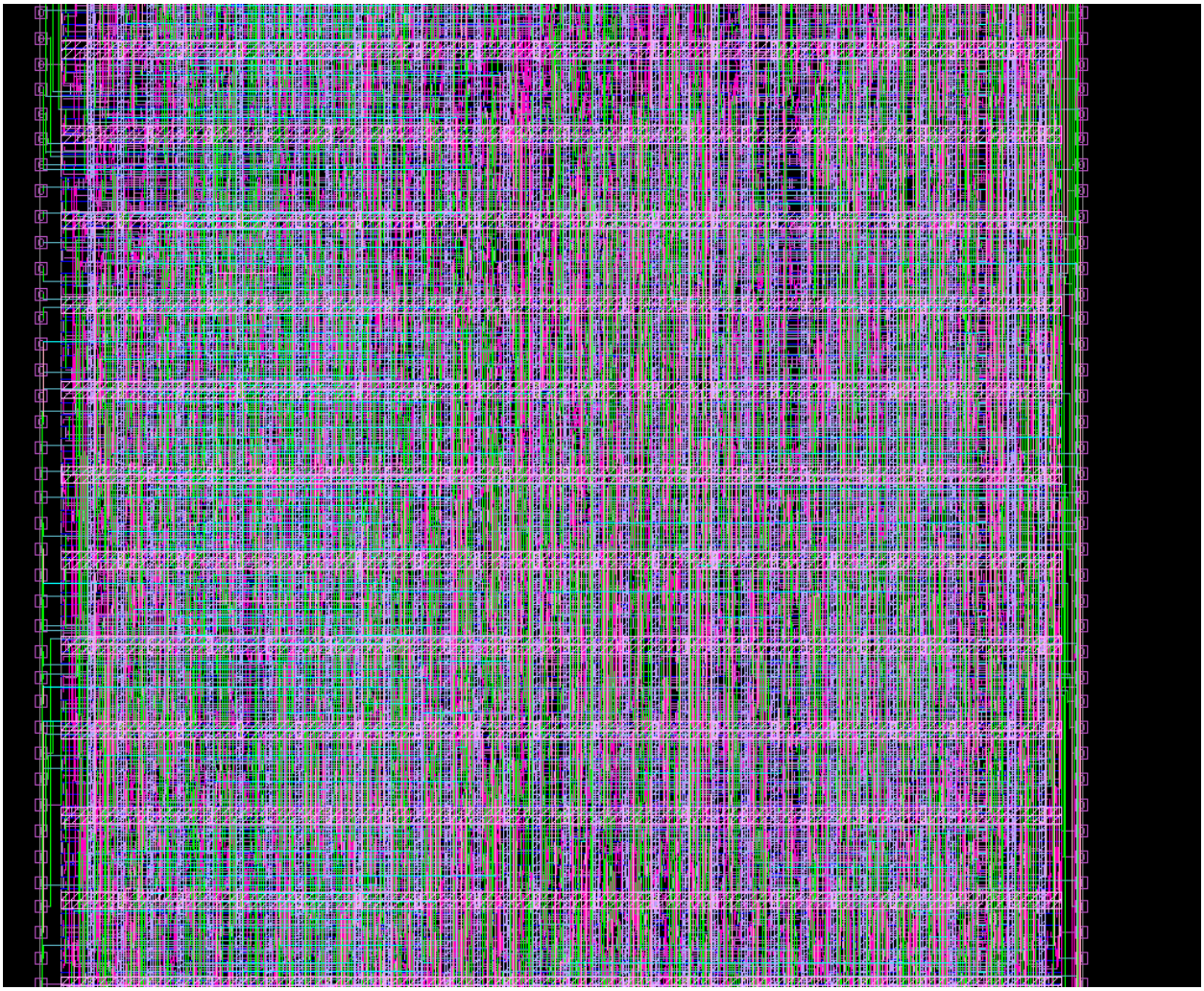
write_gds ../results/router_1.gds

write_sdc -output ../results/router_v.sdc

save_block

final stage image





Reports

Report_timing

```
1
icc2_shell> report_timing
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -report_by design
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Wed Dec 13 14:11:17 2023
****************************************
Information: Timer using 'CRPR'. (TIM-050)

  Startpoint: CSRF/MCAUSE_REG/int_or_exc_out_reg (rising edge-triggered flip-flop clocked by clk)
  Endpoint: REG1/pc_out_reg[31] (rising edge-triggered flip-flop clocked by clk)
  Mode: default
  Corner: default
  Scenario: default
  Path Group: clk
  Path Type: max

  Point                                          Incr      Path
  ---------------------------------------------------------------------------
  clock clk (rise edge)                          0.00      0.00
  clock network delay (propagated)               0.18      0.18

  CSRF/MCAUSE_REG/int_or_exc_out_reg/CLK (DFFX1_HVT)
                                                 0.00      0.18 r
  CSRF/MCAUSE_REG/int_or_exc_out_reg/Q (DFFX1_HVT)
                                                 2.30      2.48 f
  CSRF/MTVEC_REG/U3/Y (NAND4X0_RVT)              0.37      2.84 r
  CSRF/MTVEC_REG/U4/Y (INVX0_RVT)                0.13      2.97 f
  CSRF/MTVEC_REG/U8/CO (FADDX1_RVT)              0.26      3.23 f
  CSRF/MTVEC_REG/U10/CO (FADDX1_RVT)             0.21      3.44 f
  CSRF/MTVEC_REG/U11/CO (FADDX1_RVT)             0.17      3.61 f
  CSRF/MTVEC_REG/U12/Y (NBUFFX4_HVT)             0.15      3.76 f
  CSRF/MTVEC_REG/U13/Y (NAND4X0_RVT)             0.13      3.90 r
  CSRF/MTVEC_REG/U14/Y (INVX0_RVT)               0.10      4.00 f
  CSRF/MTVEC_REG/U15/Y (NAND2X0_RVT)             0.16      4.16 r
  CSRF/MTVEC_REG/U16/Y (INVX0_RVT)               0.10      4.26 f
  CSRF/MTVEC_REG/U17/Y (NAND2X0_RVT)             0.16      4.42 r
  CSRF/MTVEC_REG/U18/Y (INVX0_LVT)               0.03      4.45 f
  CSRF/MTVEC_REG/U19/Y (NAND2X0_RVT)             0.15      4.61 r
  CSRF/MTVEC_REG/U20/Y (INVX0_LVT)               0.02      4.63 f
  CSRF/MTVEC_REG/U21/Y (NAND2X0_RVT)             0.16      4.79 r
  CSRF/MTVEC_REG/U22/Y (INVX1_HVT)               0.38      5.17 f
  CSRF/MTVEC_REG/U23/Y (NAND2X0_RVT)             0.27      5.44 r
  CSRF/MTVEC_REG/U24/Y (INVX0_LVT)               0.03      5.47 f
  CSRF/MTVEC_REG/U25/Y (NAND2X0_RVT)             0.18      5.65 r
  CSRF/MTVEC_REG/U26/Y (INVX1_HVT)               0.34      5.99 f
  CSRF/MTVEC_REG/U27/Y (NAND2X0_RVT)             0.33      6.32 r
```

```
CSRF/MTVEC_REG/U27/Y (NAND2X0_RVT)                      0.33      6.32 f
CSRF/MTVEC_REG/U28/Y (INVX1_HVT)                        0.44      6.76 f
CSRF/MTVEC_REG/U29/Y (NAND2X0_RVT)                      0.28      7.04 r
CSRF/MTVEC_REG/U30/Y (INVX0_LVT)                        0.02      7.07 f
CSRF/MTVEC_REG/U31/Y (NAND2X0_RVT)                      0.14      7.20 r
CSRF/MTVEC_REG/U32/Y (INVX0_LVT)                        0.03      7.24 f
CSRF/MTVEC_REG/U33/Y (NAND2X0_RVT)                      0.14      7.38 r
CSRF/MTVEC_REG/U34/Y (INVX0_LVT)                        0.04      7.42 f
CSRF/MTVEC_REG/U35/Y (NAND2X0_RVT)                      0.15      7.57 r
CSRF/MTVEC_REG/U36/Y (INVX0_LVT)                        0.03      7.60 f
CSRF/MTVEC_REG/U37/Y (NAND2X0_RVT)                      0.14      7.74 r
CSRF/MTVEC_REG/U38/Y (INVX0_LVT)                        0.03      7.76 f
CSRF/MTVEC_REG/U39/Y (NAND2X0_RVT)                      0.14      7.90 r
CSRF/MTVEC_REG/U40/Y (INVX0_LVT)                        0.03      7.94 f
CSRF/MTVEC_REG/U41/Y (NAND2X0_RVT)                      0.15      8.08 r
CSRF/MTVEC_REG/U42/Y (INVX0_LVT)                        0.02      8.11 f
CSRF/MTVEC_REG/U43/Y (NAND2X0_RVT)                      0.14      8.25 r
CSRF/MTVEC_REG/U44/Y (INVX0_LVT)                        0.03      8.28 f
CSRF/MTVEC_REG/U45/Y (NAND2X0_RVT)                      0.14      8.42 r
CSRF/MTVEC_REG/U46/Y (INVX0_LVT)                        0.04      8.46 f
CSRF/MTVEC_REG/U47/Y (NAND2X0_RVT)                      0.16      8.62 r
CSRF/MTVEC_REG/U48/Y (INVX0_LVT)                        0.02      8.64 f
CSRF/MTVEC_REG/U49/Y (NAND2X0_RVT)                      0.14      8.78 r
CSRF/MTVEC_REG/U50/Y (INVX0_LVT)                        0.02      8.81 f
CSRF/MTVEC_REG/U51/Y (NAND2X0_RVT)                      0.14      8.95 r
CSRF/MTVEC_REG/U52/Y (INVX0_LVT)                        0.02      8.97 f
CSRF/MTVEC_REG/U53/Y (NAND2X0_RVT)                      0.14      9.12 r
CSRF/MTVEC_REG/U54/Y (INVX0_LVT)                        0.02      9.14 f
CSRF/MTVEC_REG/U55/Y (NAND2X0_RVT)                      0.14      9.29 r
CSRF/MTVEC_REG/U56/Y (INVX0_LVT)                        0.02      9.31 f
CSRF/MTVEC_REG/U57/Y (NAND2X0_RVT)                      0.15      9.46 r
CSRF/MTVEC_REG/U87/Y (INVX0_RVT)                        0.10      9.56 f
CSRF/MTVEC_REG/U88/SO (HADDX1_RVT)                      0.27      9.82 r
PC/U196/Y (AO22X1_RVT)                                  0.16      9.98 r
PC/U197/Y (OR2X1_RVT)                                   0.13     10.11 r
REG1/U38/Y (AND2X1_RVT)                                 0.11     10.22 r
REG1/pc_out_reg[31]/D (DFFX1_RVT)                       0.00     10.22 r
data arrival time                                                10.22

clock clk (rise edge)                                  10.00     10.00
clock network delay (propagated)                        0.32     10.32
clock reconvergence pessimism                           0.00     10.32
REG1/pc_out_reg[31]/CLK (DFFX1_RVT)                     0.00     10.32 r
library setup time                                     -0.10     10.22
data required time                                               10.22
--------------------------------------------------------------------------
data required time                                               10.22
data arrival time                                               -10.22
--------------------------------------------------------------------------
slack (MET)                                                      0.00
```

Report_constraints

```
icc2_shell> report_constraints
****************************************
Report : constraint
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Wed Dec 13 14:19:30 2023
****************************************

                                                 Weighted
    Group (min_delay/hold)       Cost     Weight     Cost     Scenario
    ------------------------------------------------------------------
    **default**                  0.00      1.00      0.00     default
    **async_default**            0.00      1.00      0.00     default
    **clock_gating_default**     0.00      1.00      0.00     default
    **in2reg_default**           0.00      0.10      0.00     default
    **reg2out_default**          0.00      0.10      0.00     default
    **in2out_default**           0.00      0.10      0.00     default
    clk                          0.00      1.00      0.00     default
    ------------------------------------------------------------------
    min_delay/hold                                   0.00

                                                 Weighted
    Group (max_delay/setup)      Cost     Weight     Cost     Scenario
    ------------------------------------------------------------------
    **default**                  0.00      1.00      0.00     default
    **async_default**            0.00      1.00      0.00     default
    **clock_gating_default**     0.00      1.00      0.00     default
    **in2reg_default**           0.00      0.10      0.00     default
    **reg2out_default**          0.00      0.10      0.00     default
    **in2out_default**           0.00      0.10      0.00     default
    clk                          0.00      1.00      0.00     default
    ------------------------------------------------------------------
    max_delay/setup                                  0.00

    Constraint                                       Cost
    ---------------------------------------------------
    min_delay/hold                                   0.00  (MET)
    max_delay/setup                                  0.00  (MET)
    max_transition                                   0.00  (VIOLATED)
    max_capacitance                                  3.84  (VIOLATED)
    min_capacitance                                  0.00  (MET)
1
icc2_shell>
```

Report_utilization

```
icc2_shell> report_utilization
****************************************
Report : report_utilization
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Wed Dec 13 14:23:11 2023
****************************************
Utilization Ratio:                      0.7439
Utilization options:
 - Area calculation based on:           site_row of block msrv32_top
 - Categories of objects excluded:      hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area:                             39943.8125
Total Capacity Area:                    39943.8125
Total Area of cells:                    29713.4999
Area of excluded objects:
 - hard_macros         :                0.0000
 - macro_keepouts      :                0.0000
 - soft_macros         :                0.0000
 - io_cells            :                0.0000
 - hard_blockages      :                0.0000

Utilization of site-rows with:
 - Site 'unit':                         0.7439

0.7439
icc2 shell>
```

Report_congestion

```
icc2_shell> report_congestion
Information: The command 'report_congestion' cleared the undo history. (U
****************************************
Report : congestion
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Wed Dec 13 14:22:27 2023
****************************************

Layer      |    overflow     |               # GRCs has
Name       |  total   |  max   | overflow (%)       | max overflow
-----------------------------------------------------------------
Both Dirs  |    1953  |     8  |    1571  ( 5.16%)  |       1
H routing  |    1161  |     4  |     991  ( 6.51%)  |       1
V routing  |     792  |     8  |     580  ( 3.81%)  |       1

1
```

Check_lvs

```
icc2_shell> check_lvs
Information: Using 1 threads for LVS
[Check Short] Stage 1   Elapsed =    0:00:00, CPU =    0:00:00
[Check Short] Stage 1-2 Elapsed =    0:00:01, CPU =    0:00:00
[Check Short] Stage 2   Elapsed =    0:00:01, CPU =    0:00:00
[Check Short] Stage 2-2 Elapsed =    0:00:08, CPU =    0:00:07
[Check Short] Stage 3   Elapsed =    0:00:08, CPU =    0:00:07
[Check Short] End       Elapsed =    0:00:08, CPU =    0:00:07
[Check Net] Init        Elapsed =    0:00:08, CPU =    0:00:07
Warning: Port VSS have no valid pin shapes. Skip this port. (RT-203)
Warning: Port VDD have no valid pin shapes. Skip this port. (RT-203)
[Check Net] 10%         Elapsed =    0:00:12, CPU =    0:00:10
[Check Net] 20%         Elapsed =    0:00:12, CPU =    0:00:11
[Check Net] 30%         Elapsed =    0:00:13, CPU =    0:00:11
[Check Net] 40%         Elapsed =    0:00:13, CPU =    0:00:12
[Check Net] 50%         Elapsed =    0:00:14, CPU =    0:00:12
[Check Net] 60%         Elapsed =    0:00:14, CPU =    0:00:12
[Check Net] 70%         Elapsed =    0:00:14, CPU =    0:00:13
[Check Net] 80%         Elapsed =    0:00:14, CPU =    0:00:13
[Check Net] 90%         Elapsed =    0:00:15, CPU =    0:00:14
[Check Net] All nets are submitted.
[Check Net] 100%        Elapsed =    0:00:15, CPU =    0:00:14

************************************************************
    Maximum number of violations is set to 20
    Abort checking when more than 20 violations are found
    All violations might not be found.
************************************************************
Total number of input nets is 9469.
Total number of short violations is 0.
Total number of open nets is 0.
Total number of floating route violations is 0.

Elapsed =    0:00:15, CPU =    0:00:14
1
```

Check_routes

```
Verify Summary:

Total number of nets = 9451, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = no antenna rules defined
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked


icc2_shell>
```

Check_design

```
1
icc2_shell> report_design
****************************************
Report : design
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Wed Dec 13 14:26:24 2023
****************************************

Total number of std cells in library : 1025
Total number of dont_use lib cells   : 80
Total number of dont_touch lib cells : 80
Total number of buffers              : 69
Total number of inverters            : 45
Total number of flip-flops           : 318
Total number of latches              : 36
Total number of ICGs                 : 36

Cell Instance Type  Count         Area
-------------------------------------
TOTAL LEAF CELLS     9154    29713.500
Standard cells       9154    29713.500
Hard macro cells        0        0.000
Soft macro cells        0        0.000
Always on cells         0        0.000
Physical only           0        0.000
Fixed cells             0        0.000
Moveable cells       9154    29713.500
Sequential           1613    11190.469
Buffer/inverter      1406     2907.153
ICG cells               0        0.000

Logic Hierarchies                    : 27
Design Masters count                 : 144
Total Flat nets count                : 9469
Total FloatingNets count             : 18
Total no of Ports                    : 241
Number of Master Clocks in design    : 1
Number of Generated Clocks in design : 0
Number of Path Groups in design      : 7 (1 of them Non Default)
Number of Scan Chains in design      : 0
List of Modes                        : default
List of Corners                      : default
List of Scenarios                    : default

Core Area                            : 39943.812
Chip Area                            : 42523.380
Total Site Row Area                  : 39943.812
Number of Blockages                  : 0
Total area of Blockages              : 0.000
Number of Power Domains              : 1
Number of Voltage Areas              : 1
Number of Group Bounds               : 0
Number of Exclusive MoveBounds       : 0
```

```
Number of Voltage Areas               : 1
Number of Group Bounds                : 0
Number of Exclusive MoveBounds        : 0
Number of Hard or Soft MoveBounds     : 0
Number of Multibit Registers          : 0
Number of Multibit LS/ISO Cells       : 0
Number of Top Level RP Groups         : 0
Number of Tech Layers                 : 71 (61 of them have unknown routing dir.)

Total wire length                     : 265579.55 micron
Total number of wires                 : 108142
Total number of contacts              : 112150
1
icc2_shell> ■
```

Report_qor

```
0.7439
icc2_shell> report_qor
****************************************
Report : qor
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Wed Dec 13 14:24:34 2023
****************************************
Information: Timer using 'CRPR'. (TIM-050)


Scenario           'default'
Timing Path Group  'clk'
-----------------------------------------
Levels of Logic:                     56
Critical Path Length:             10.04
Critical Path Slack:               0.00
Critical Path Clk Period:         10.00
Total Negative Slack:              0.00
No. of Violating Paths:               0
Worst Hold Violation:              0.00
Total Hold Violation:              0.00
No. of Hold Violations:               0
-----------------------------------------


Cell Count
-----------------------------------------
Hierarchical Cell Count:             27
Hierarchical Port Count:           4101
Leaf Cell Count:                   9154
Buf/Inv Cell Count:                1406
Buf Cell Count:                     499
Inv Cell Count:                     907
CT Buf/Inv Cell Count:                0
Combinational Cell Count:          7541
   Single-bit Isolation Cell Count:                      0
   Multi-bit Isolation Cell Count:                       0
   Isolation Cell Banking Ratio:                         0.00%
   Single-bit Level Shifter Cell Count:                  0
   Multi-bit Level Shifter Cell Count:                   0
   Level Shifter Cell Banking Ratio:                     0.00%
   Single-bit ELS Cell Count:                            0
   Multi-bit ELS Cell Count:                             0
   ELS Cell Banking Ratio:                               0.00%
Sequential Cell Count:             1613
   Integrated Clock-Gating Cell Count:                   0
   Sequential Macro Cell Count:                          0
   Single-bit Sequential Cell Count:                     1613
   Multi-bit Sequential Cell Count:                      0
   Sequential Cell Banking Ratio:                        0.00%
   BitsPerflop:                                          1.00
Macro Count:                          0
-----------------------------------------
```

```
Macro Count:                          0
----------------------------------------


Area
----------------------------------------
Combinational Area:           18523.03
Noncombinational Area:        11190.47
Buf/Inv Area:                  2907.15
Total Buffer Area:             1481.66
Total Inverter Area:           1425.49
Macro/Black Box Area:             0.00
Net Area:                            0
Net XLength:                  129386.40
Net YLength:                  205847.70
----------------------------------------
Cell Area (netlist):                        29713.50
Cell Area (netlist and physical only):      29713.50
Net Length:                   335234.10


Design Rules
----------------------------------------
Total Number of Nets:             9469
Nets with Violations:                9
Max Trans Violations:                1
Max Cap Violations:                  8
----------------------------------------

1
```