Field effect transistor

FET:

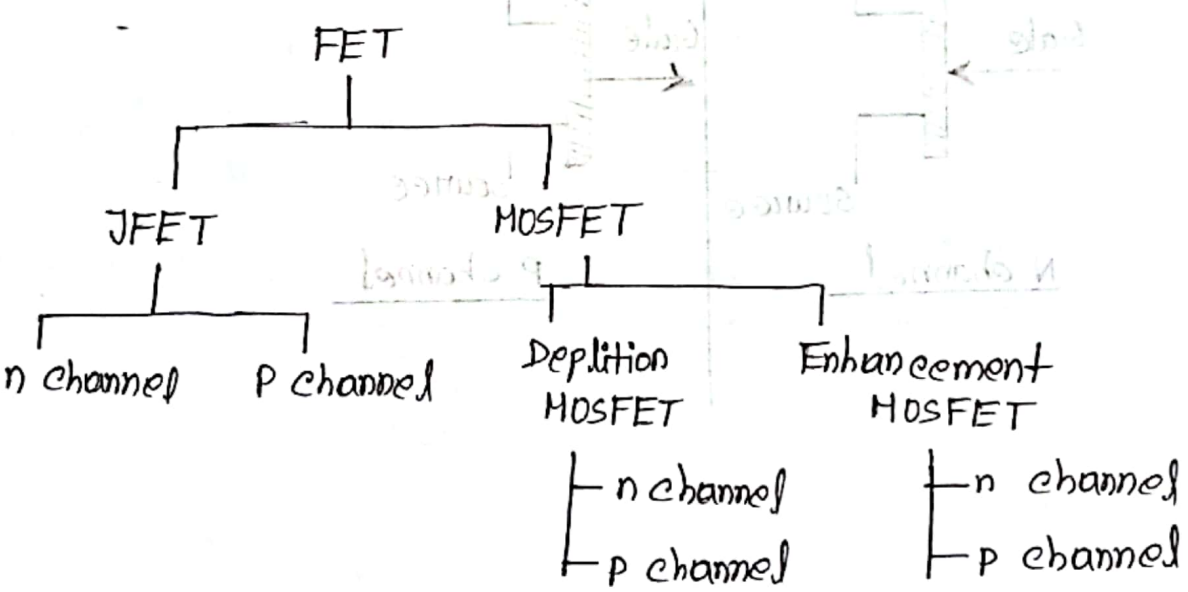
Definition: The FET or field effect transistor is a three terminal device that uses an electric field to control the current flowing through the device.

Types of FET:

There are two types of FET. They are

① JFET (Junction type field Effect transistor)

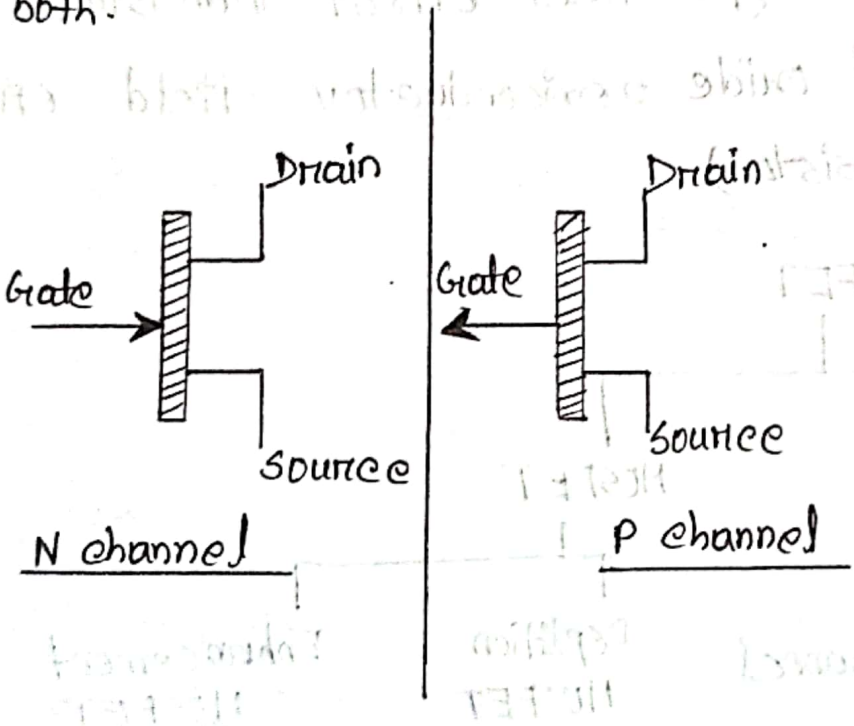
② MOSFET (Metal oxide semiconductor field effect Transistor)



The field effect transistor (FET) is a type of transistor that uses an electric field to control the flow of current in a semiconductor. FETs (JFETs or MOSFETs) are devices with ~~the~~ three terminals: source, Gate and Drain.

FET control the flow of current by the application of a voltage to the gate, which in turn alters the conductivity between the drain and source. FET are also known as unipolar transistors. since they involve single-carrier-type operation.

That is FET use either electrons (n-channel) or holes (P-channel) as charge carries in their operation. but not both.



JFET: (Junction field effect transistor)

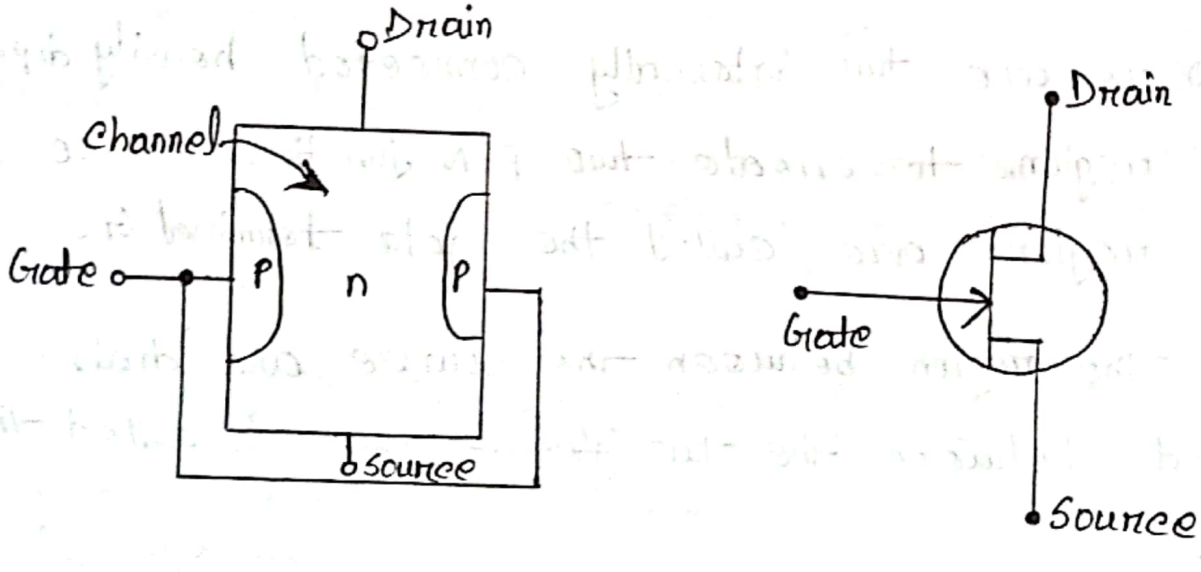
It is a three terminal semiconductor device in which current conducted by one type of carrier by electron or hole.

It is one of the simplest types of field transistor.

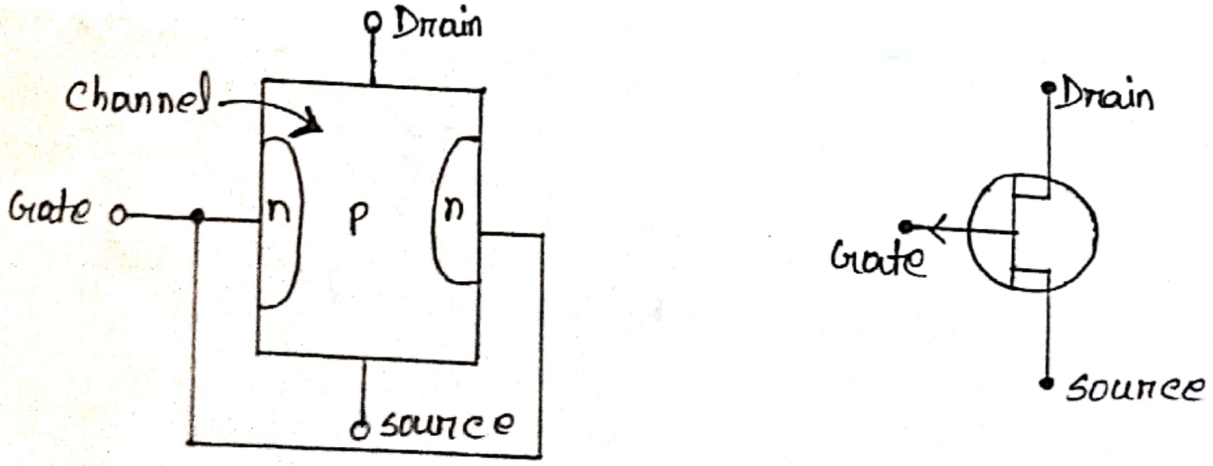
Types of JFET: n channel JFET
P channel JFET

Three terminals are: ① Drain (D)
② Grate (G)
③ Source (S)

Symbol of JFET:

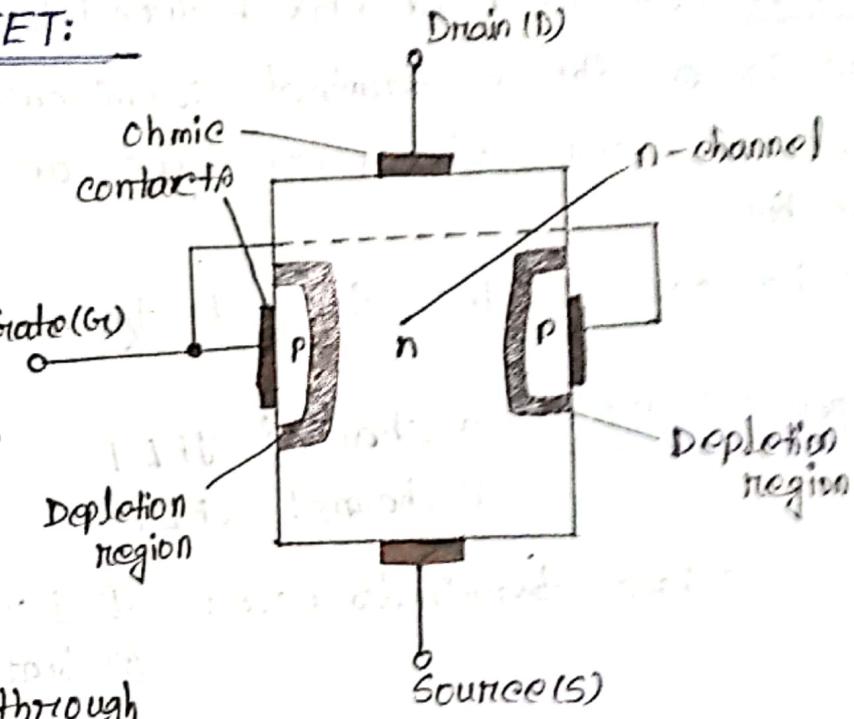


n-Channel JFET



P-Channel JFET

Construction of JFET:



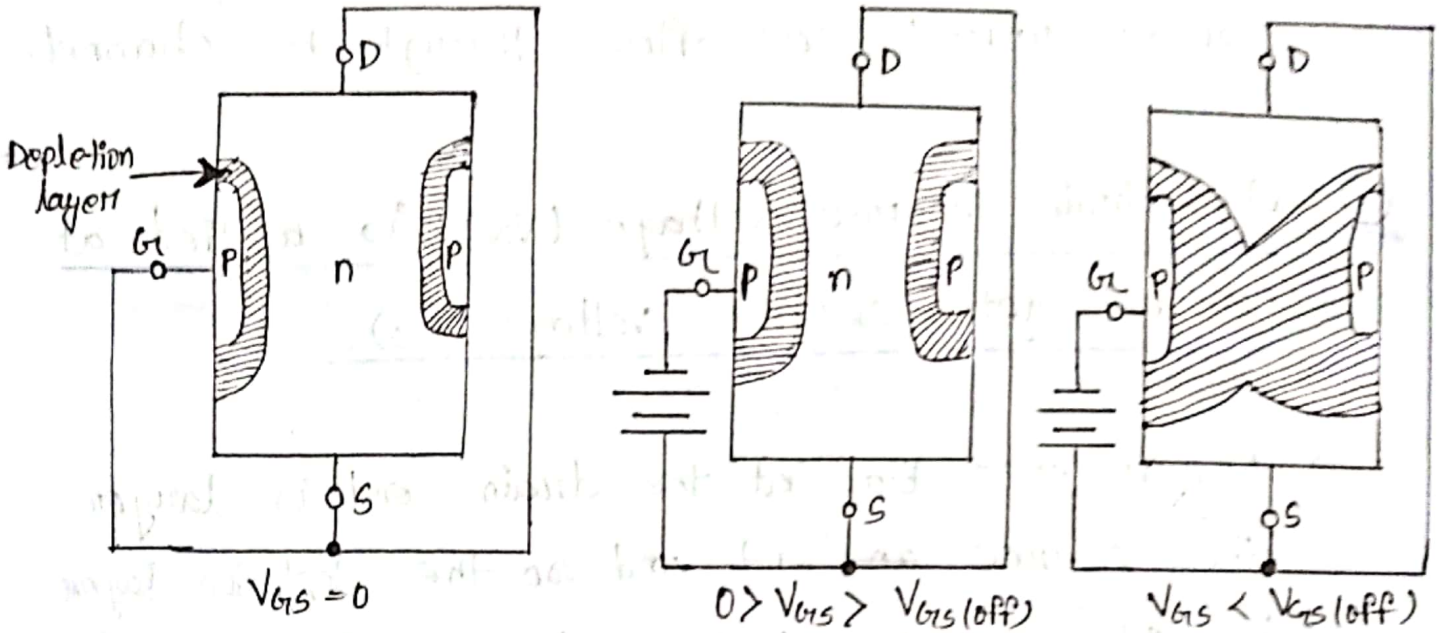
Source: The terminal through which the majority carriers enter into the channel, is called the source terminal (S).

Drain: The terminal, through which the majority carriers leave from the channel, is called the drain terminal D.

Gate: There are two internally connected heavily doped impurity regions to create two P-N junctions. These impurity regions are called the gate terminal G.

Channel: The region between the source and drain, sandwiched between the two ~~glasses~~ gates is called the channel.

operation of JFET:



$V_{GS} = 0$ | $0 > V_{GS} > V_{GS(off)}$ | $V_{GS} < V_{GS(off)}$

(a) Bias is zero and depletion layer is thin hence channel resistance is low.

(b) V_{GS} is applied hence depletion layer is increased so, less charge can be flow through the channel.

(c) V_{GS} is greater than cut off voltage hence no conductive path exist.

(i) when gate source voltage (V_{GS}) is applied and drain-source voltage (V_{DS}) is zero,

i.e, $V_{DS} = 0V$.

⇒ when $V_{GS} = 0V$, two depletion layer and channel are formed normally.

⇒ when V_{GS} increase negativity i.e, $0V > V_{GS} > V_{GS(off)}$ depletion layers are also increased and channel will be decrease.

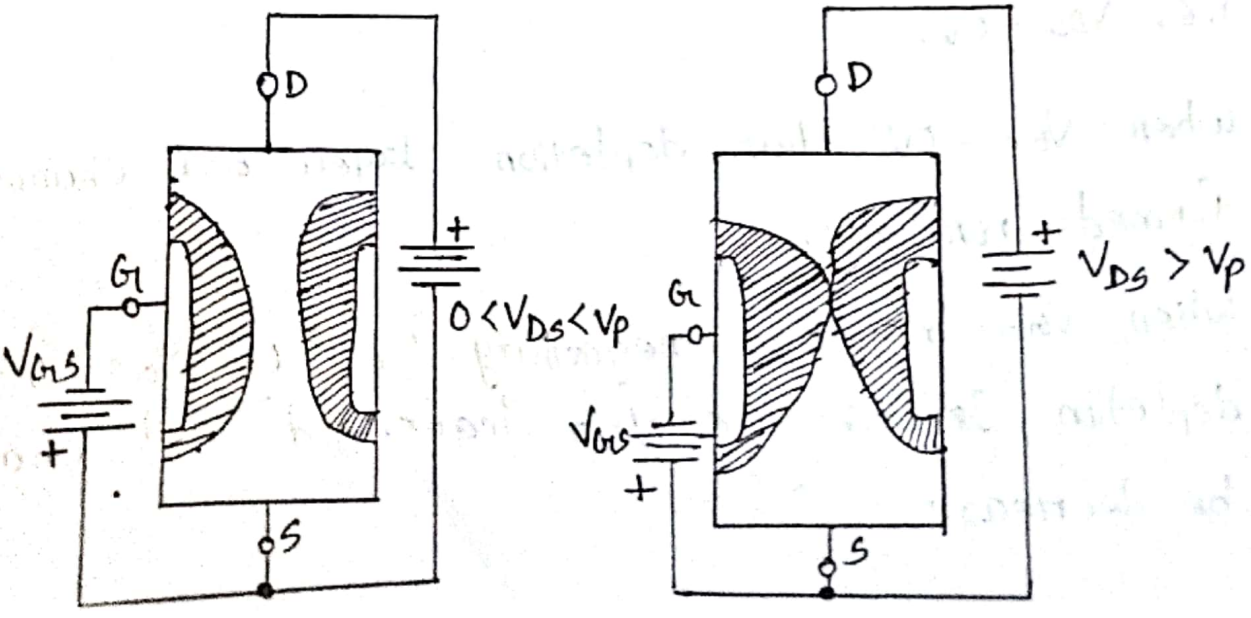
⇒ When $V_{GS} = V_{GS(off)}$ depletion layer will be touch each other and channel will totally removed. So, no current can flow through the channel.

(ii) When drain source voltage (V_{DS}) is applied at constant gate – source voltage (V_{GS}).

⇒ Now reverse bias at the drain end is larger than source ~~end~~ end and so the depletion layer is wider at the drain end than source end.

⇒ When V_{DS} increases i.e $0V < V_{DS} < V_p$ depletion layer at drain end is gradually increased and drain current also increased.

⇒ When $V_{DS} = V_p$ the channel is effectively closed at drain end and it does not allow further increase of drain current. So the drain current will become constant.

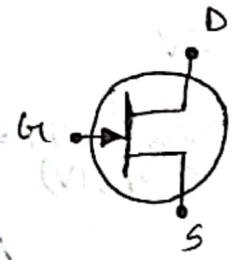


(a) channel becomes narrower as V_{DS} is increased.

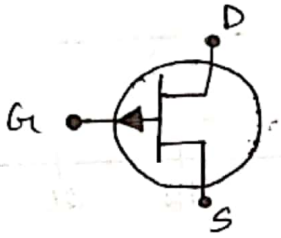
(b) Current is confined to a very narrow strip for $V_{DS} > V_p$

JFET (Depletion mode) →

N-channel



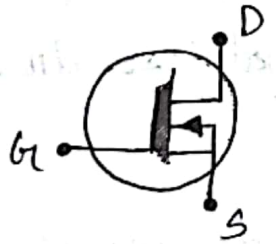
P-channel



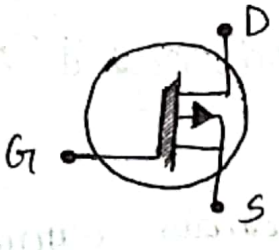
MOSFET:

(Depletion-Mode)

(i) N-channel

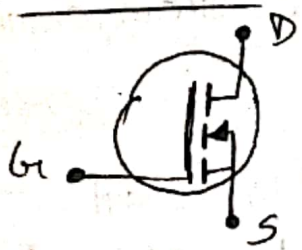


(ii) P-channel

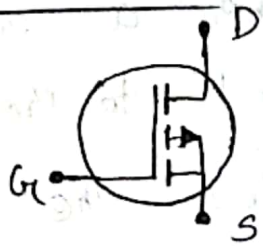


(Enhancement mode)

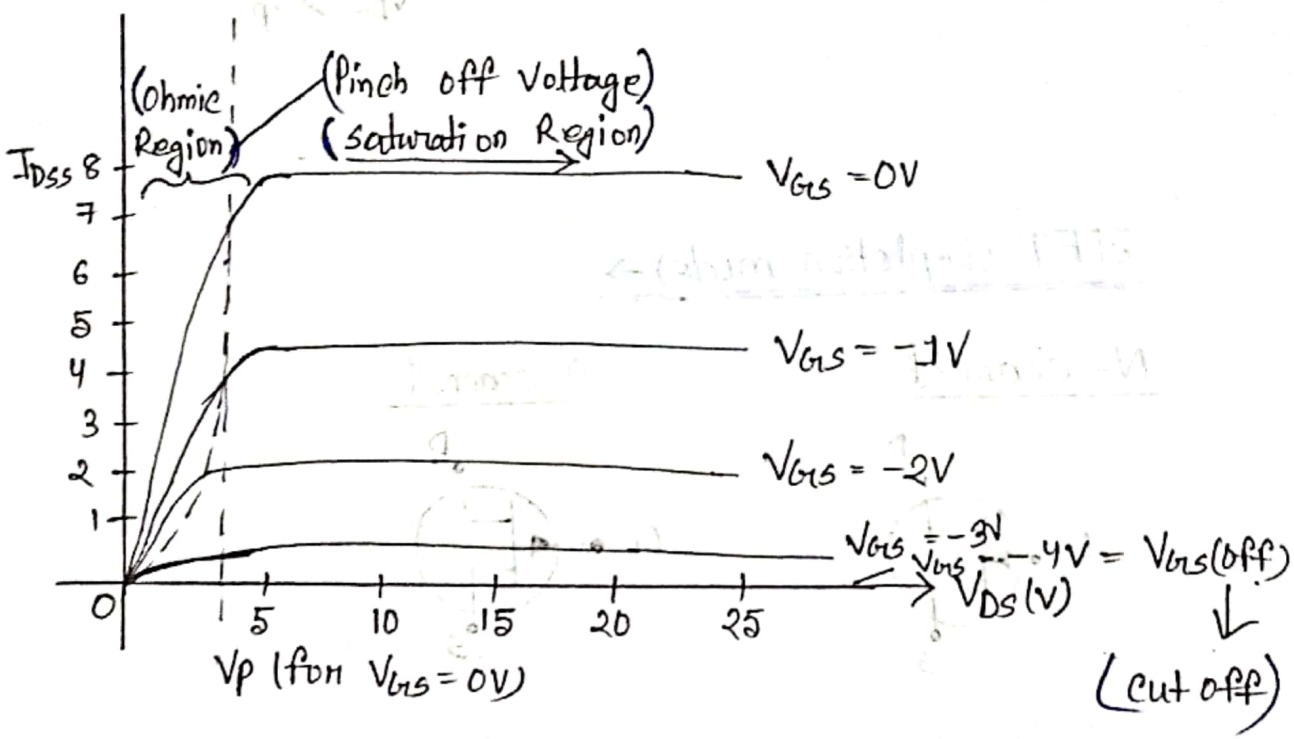
(i) N-channel



(ii) P-channel



I-V characteristic curve:

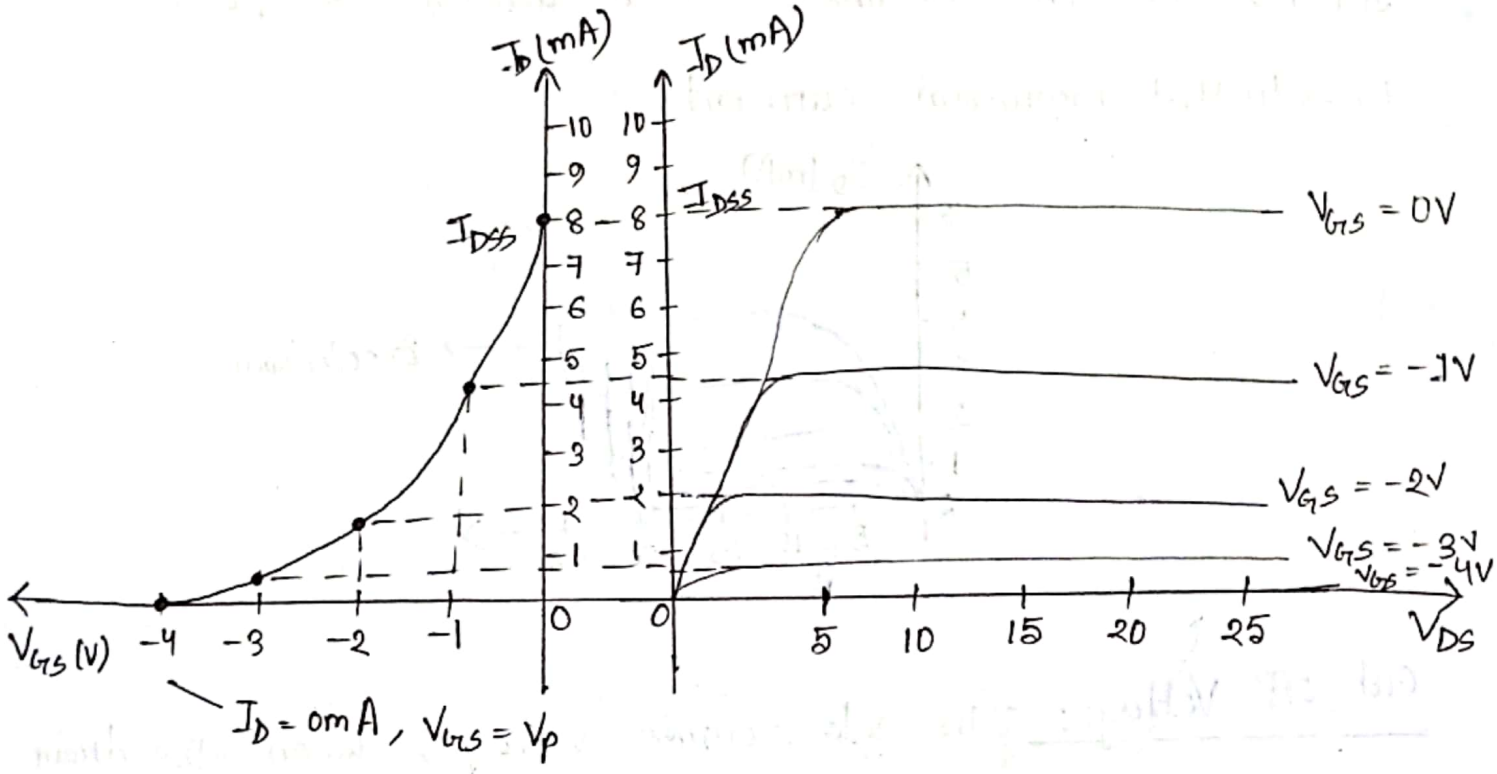


It is the curve between drain current (I_D) and drain source voltage (V_{DS}) for different gate source voltage (V_{GS}). It can be characterized as:

1. For $V_{GS} = 0V$ the drain current is maximum. It is denoted as I_{DSS} and called shorted gate ~~go~~ drain current.
2. If V_{GS} increases drain current I_D decreases ($I_D < I_{DSS}$) even through V_{DS} is increased.
3. When V_{GS} reaches a certain value, the drain current will be decreased to zero.
4. For different V_{GS}, the I_D will become constant after pinch off voltage (V_P) though V_{DS} is increased.

Transfer characteristic curve:

This curve shows the value of I_D for a given value of V_{GS}.

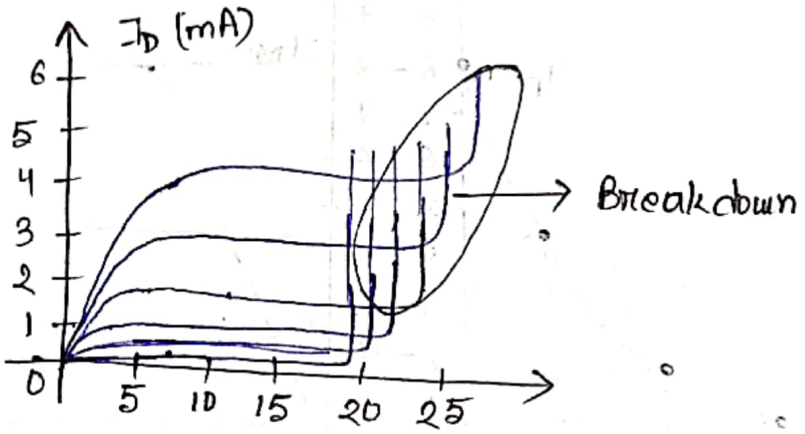


Pinch of voltage: It is the minimum drain source voltage at which the drain current essentially become constant.

Saturation level: After pinch off voltage the drain current become constant, this constant level is known as saturation level.

Ohmic region: The region behind the pinch off voltage where the drain current increase rapidly is known as ohmic region.

Break down Voltage: It is the region when the drain source voltage (V_{DS}) is high enough to cause the JFET's resistive channel to breakdown and pass uncontrolled maximum current.



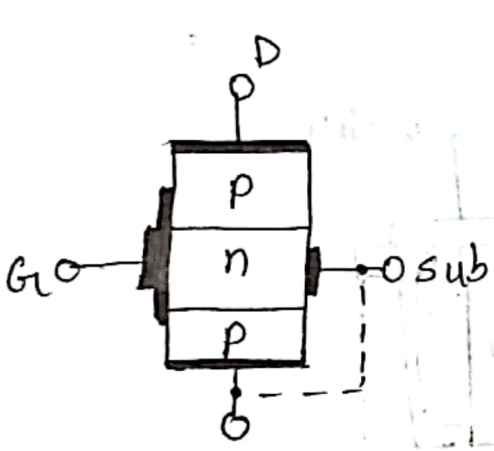
Cut off Voltage: The gate source voltage, when the drain current become zero is called ~~as~~ cut-off voltage. which is usually denoted as $V_{GS(off)}$.

MOSFET:

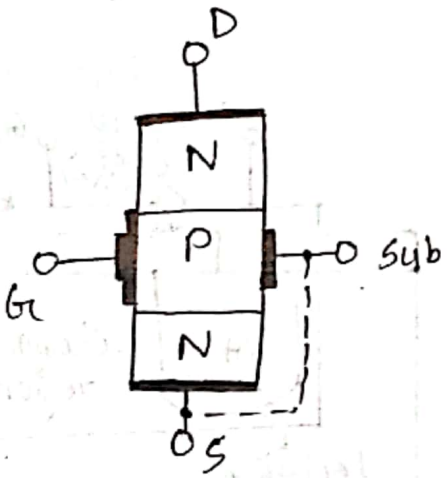
The MOSFET (Metal oxide semiconductor field effect transistor) transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices.

Terminal of Mosfet: source(s), gate(G), drain(D) and body (B)

Mosfet channel construction:

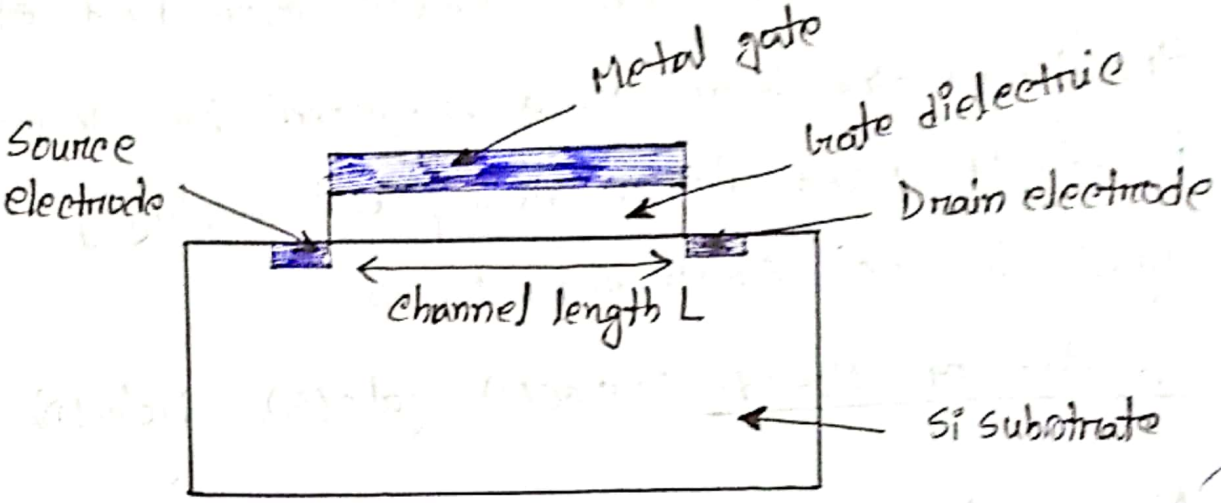


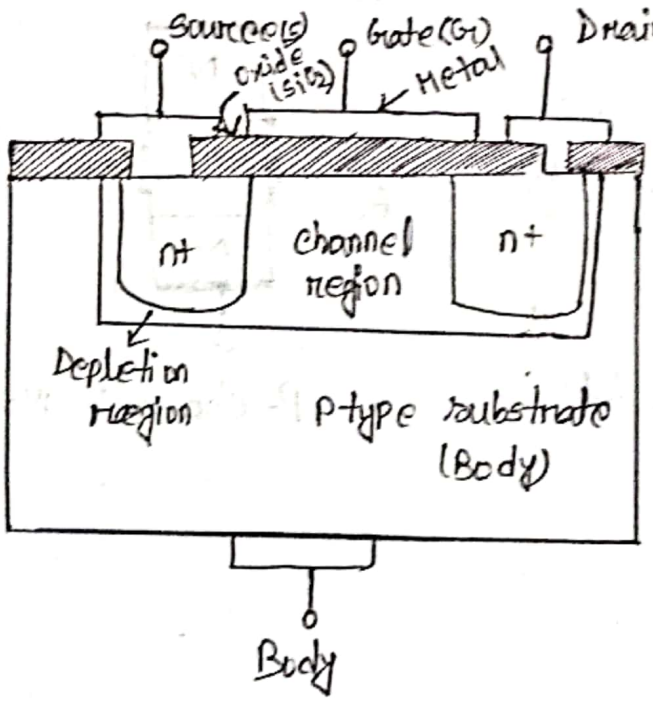
n channel Mosfet



P-channel Mosfet

Schematic structure of Mosfet:

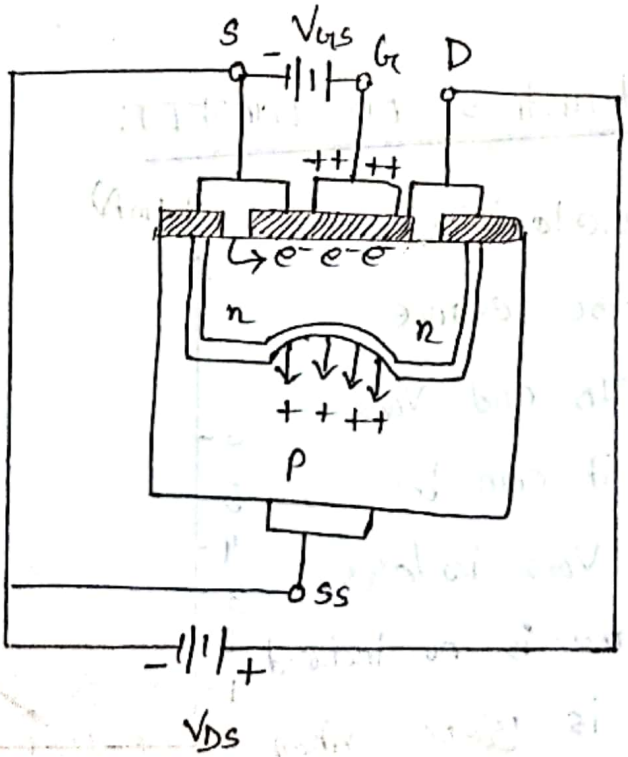




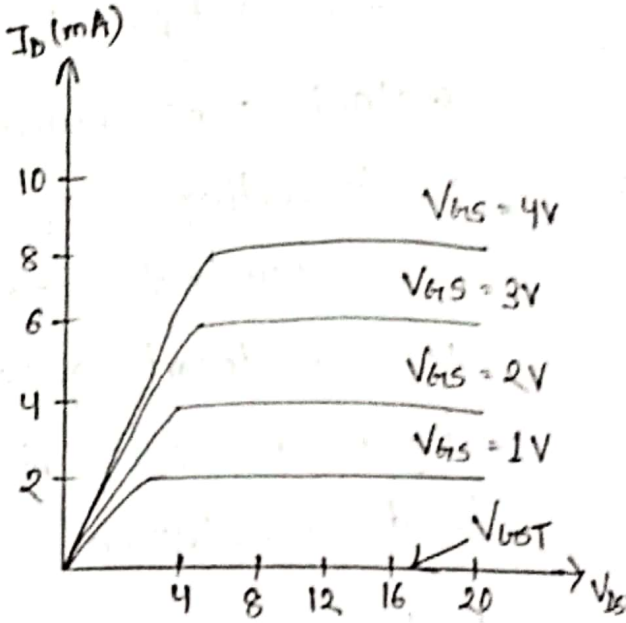
Two highly doped n-type regions are diffused in a lightly doped substrate of p-type silicon substrate. The substrate is sometimes connected to the source. Otherwise it is brought out as the fourth terminal.

The drain and source terminals are connected to the n-type doped regions through the metallic contact. The channel is absent in this type. The insulating SiO_2 layer is still present which isolates gate terminal from the substrate. This device is called the insulated gate FET because of the insulating layer of SiO_2. This layer gives an extremely high input resistance.

Working Principle of a n-channel EMOSFET:

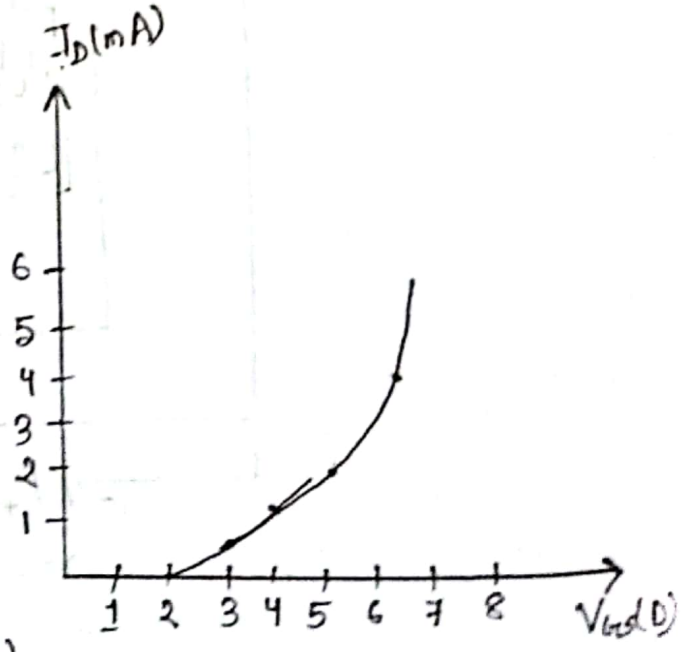


Drain characteristics of Enhancement Mosfet:



The amount of current flow is dependent on the positive amount of the potential applied at the terminal gate. If the application of the potential is below the threshold then no current flow is evident through the terminal drain. If the voltage exceeds the threshold the device gets turned ON.

Transfer characteristics of EMOSFET:



The transfer characteristics of EMOSFET is the curve plotted between I_D and V_{GS}. From the curve, it can be seen that, when V_{GS} is less than $V_{GS(th)}$. there is no induced channel and I_D is zero. When V_{GS} is made equal to $V_{GS(th)}$ the EMOSFET is turned ON and the induced channel conducts from source to drain. The further

increase in the value of V_{GS}. increases the width of induced channel and hence, the drain current.