Laboratory Manual

For

Course Code:EEE-1222
Course Title: Electronics Lab

Dept. of Computer Science & Engineering
IIUC

Contents

LIST OF EXPERIMENTS

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Instructions for Students

Introduction

EEE is an experimental science. Advancements in EEE throughout its history have come about mainly driven by experiments. For you, the EEE lab will be an opportunity to have some fun with some hands-on experience with EEE theories. Moreover, it will be an opportunity for you to develop and enhance your skills in experimental observation, data analysis, and proper scientific documentation which are always important in a career in science and engineering. So please look forward to using your laboratory time for a gainful purpose.

This manual will provide the basic theoretical backgrounds and detailed procedures of various experiments that you will perform in the lab. Before that, here are some specific instructions for you to follow while carrying out the experiments. It also outlines the approach that will be undertaken in conducting the lab. Please read carefully the following.

Specific Instructions

1. You are expected to complete one experiment in each class. For that to happen, you will have to come to the laboratory with certain initial preparation. The initial preparation will involve a prior study of the basic theory of the experiment you are going to take up as well as the procedure to perform it to have a rough idea of what to do. In addition, it will also involve a partial preparation of the lab report in advance as mentioned later in this section.
2. You must bring with you the following materials to the lab: This instruction manual, A4 size papers for writing the lab report, graph sheets if necessary, pen, pencil, measuring scale, calculator and any other stationary items required. On the very first day of your lab class, bring also a file cover/folder with your name, roll no., branch name etc. written on it clearly and submit it to the instructor. The folder will be used to store your laboratory reports regularly at the end of the classes. The folder with your reports will be kept in the laboratory and will be returned to you only after the course instructions are over.

3. The format of a lab report shall be as follows:
    a. The first sheet will contain your name, branch name, roll number, date and title of the experiment. The subsequent sheets will contain the followings in that order.
    b. The objective of the experiment, apparatus needed, and a brief theory with working formulas and figures or diagrams whenever necessary.
    c. Experimental observations. Data from experimental observations should be recorded in proper tabular format with well-documented headings for the columns. The datatables should be preceded by the least counts of the instruments used to take thedata and the numerical value of any constant, if any, used in the table.
    d. Graphs whenever applicable.
    e. Relevant calculations, and error analyses.
    f. Final results along with error estimates.
    g. Remarks if any.
    h. Please DO NOT write the procedure of the experiment anywhere.
4. As part of the initial preparation mentioned earlier, you are required to come to the lab ready with items 3.a. and 3.b. above already written in your report sheets. This will save valuable lab time and help you to complete the rest of the experiment within the allotted time.
5. After the completion of your data recording, switch off any power supply etc. used andput back the components of the apparatus in their proper places. Complete the rest ofthe relevant calculations and hand over the final report sheets to the instructor beforeleaving the lab.
6. Last but not least - please handle the instruments with care and maintain the utmost discipline and decorum in the lab.

• References

This manual was prepared with help from several books, the documentation provided by the equipment vendors, and from several documents shared by others on the website. Though it is not possible to mention all the individual sources, cited below is a list of books which students may also find helpful for further reading.

Text Books:

1. R.L. Boylestad, Louis Nashelsky, Electronic device and circuit theory, Sedra Smith, Microelectronics Circuits
2. Robert F. Coughlin, Frederick F. Driscoll, Prentice Hall, Operational Amplifier and Linear Integrated Circuits

Reference Books:

1. V.K. Mehta, Principles of Electronics
2. J. Millman, C. C. Halkias, Electronic device and circuit
3. B.L. Thereja, Basic Electronics- Solid State

EXPERIMENT NO: 01
EXPERIMENT NAME: Calibration of an Oscilloscope

Theory: An oscilloscope is a type of electronic test instrument that allows users to visualize and analyze electrical signals. It displays the signal in a graphical format, typically as a voltage versus time graph, and can be used to measure a wide range of signal characteristics such as amplitude, frequency, and phase.Calibrating an oscilloscope is to adjust the amplitude and time-based settings. The amplitude setting controls the vertical scale of the oscilloscope display, and the time-based setting controls the horizontal scale. These settings are typically adjusted using knobs or buttons on the front panel of the oscilloscope.The probe is the device that connects the oscilloscope to the signal being measured. The probe has several settings, such as attenuation and compensation, that need to be adjusted to match the characteristics of the signal being measured. This is done using a calibration signal generator and a probe calibration set.Once the amplitude and time-based settings are adjusted, and the probe is calibrated, the oscilloscope is ready to measure signals. To verify that the oscilloscope is measuring accurately, a calibration signal generator is used to generate test signals with known characteristics. The oscilloscope's measurements are then compared to the known characteristics of the test signals to verify the accuracy of the measurements.

Fig 1: Analog Oscilloscope.

Apparatus:
1. Oscilloscope.
2. Probe.

Procedure:

1.At first,if we are using channel 1, then we will adjust the mode to channel 1. There will be a little adjustment where there is a knob called AC-GND-DC. We will set it to GND.

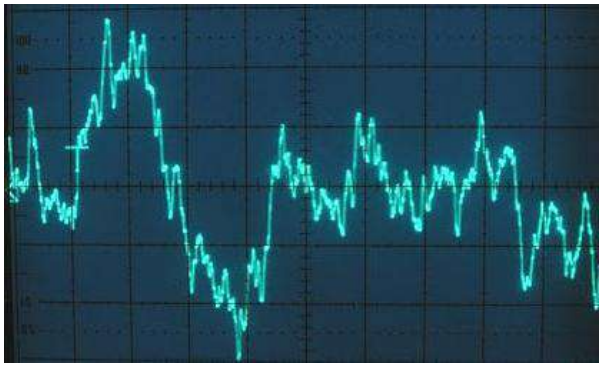


Fig 2: Noise signal.

3. When we attach the probe to the oscilloscope, we will hopefully see a horizontal line along the screen.If we don't see it, then we should adjust the intensity or focus.Even if we don't see it, maybe the line is up at the top or down at the bottom.Then we will make the line appear by adjusting the position upwardsor downwards.

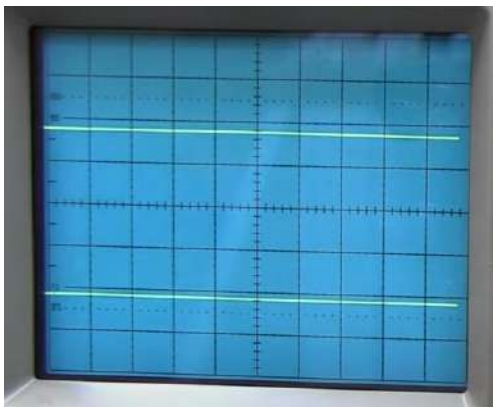


Fig 3: Low intensity.

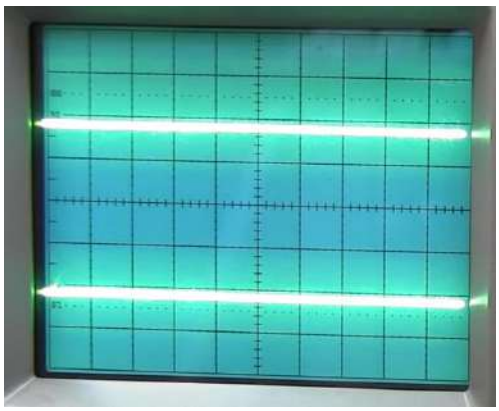


Fig 4: High intensity.

3.If there is no straight line but some slices of the line slowly moving horizontally or moving fast enough to see those slices, we have to adjust the time/div knob. By changing the knob to a higher frequency, the waveform gives a straight line. What happens is that the trace will move so fast that it will display a rock-solid line.

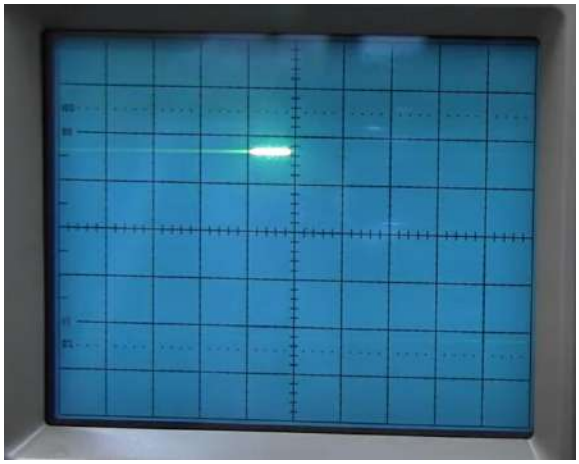


Fig 5: Waveform at a lower frequency.

4. Even after that if we don't get a straight line, we can use the level knob from the trigger section to stable the line.

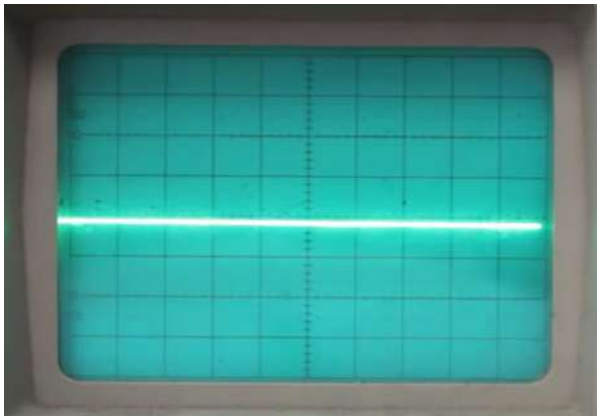


Fig 6: Straight line.

5. We will hook the prob's other end to the calibration terminal down at the left corner.It will send a square wave signal which we will use to calibrate the oscilloscope.

6. But to receive the signal on the screen we need to make some adjustments.At first, we will turn that knob from the first step to AC from GND because square waves are alternating currents.So,we will tell the oscilloscope that it will receive an AC signal.

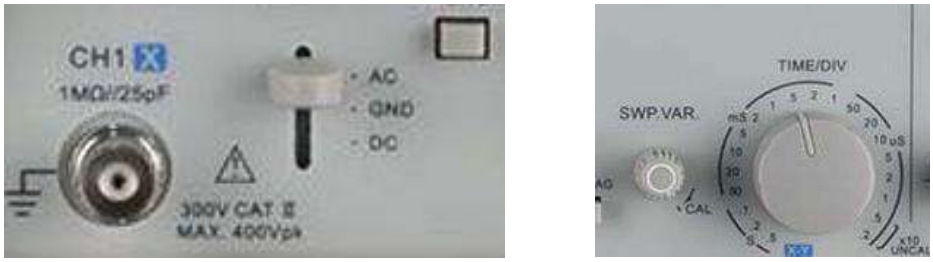


Fig 7: AC-GND-DC & TIME/DIV probe.

7. In this oscilloscope we can see it says 2-volt peak to peak. So, we will set the volts/divprob to 1 volt. This is the amplitude for our square wave.It will show one square for every 1 volt vertically.

Fig 8: VOLTS/DIV probe.

8. Then we will set the waveform on the middle line, and adjust it horizontally and vertically until we get a 2-volt peak-to-peak square wave.

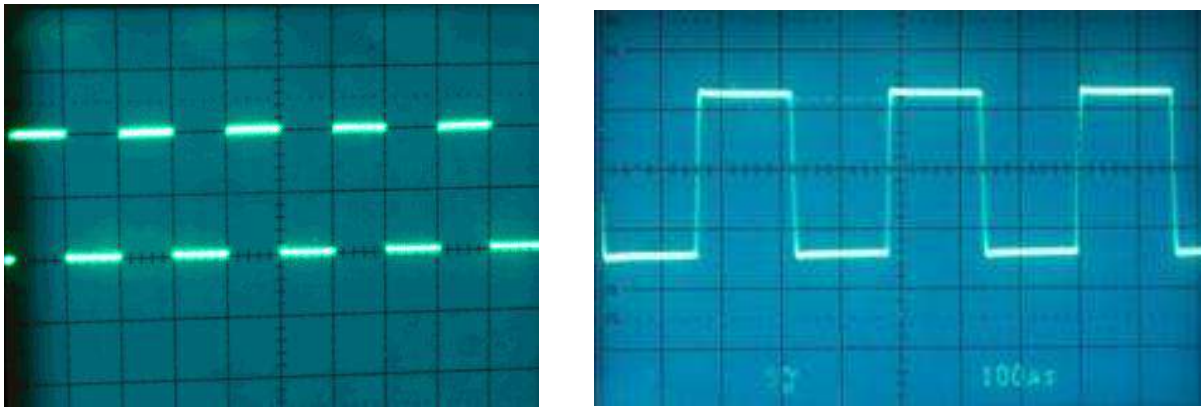


Fig 9: Square Waveforms.

Discussion: Calibration of an oscilloscope involves adjusting the instrument to ensure that it is measuring signals accurately and consistently. For the analogue oscilloscope, calibration is needed to get a stable waveform from the function generator as an output. It is important to calibrate an oscilloscope regularly to ensure that the instrument is providing accurate measurements, as the instrument's performance can drift over time due to ageing or environmental factors. Also, different types of oscilloscopes need a different types of calibration procedures.

EXPERIMENT NO: 02
EXPERIMENT NAME: To study of V-l Characteristics curve of P-N junction diode.

Objective:

1. To plot Volt-Ampere Characteristics of Silicon P-N Junction Diode.
2. To find cut-in Voltage for Silicon P-N Junction diode.
3. To find static and dynamic resistances in both forward and reverse-biased conditions for the P-N Junction diode

Hardware Requirement:

S.NO	Apparatus	Type	Range	Quantity
01	PN Junction Diode	IN4001		1
02	Resistance		1k ohm	1
03	Regulated power supply		(0 – 30V)	1
04	Ammeter	mC	(0-30)mA,(0-500)μA	1
05	Voltmeter	mC	(0 – 1)V, (0 – 30)V	1
06	Breadboard and connecting wires			

Introduction:

Donor impurities (pentavalent) are introduced into one side and acceptor impurities into the other side of a single crystal of an intrinsic semiconductor to form a p-n diode with a junction called depletion region (this region is depleted of the charge carriers). This region gives rise to a potential barrier Vγ called **Cut-in Voltage**. This is the voltage across the diode at which it starts conducting. The P-N junction can conduct beyond this Potential.

The P-N junction supports uni-directional current flow. If the +ve terminal of the input supply is connected to the anode (P-side) and the –ve terminal of the input supply is connected to the cathode (N- side), then the diode is said to be forward-biased. In this condition, the height of the potential barrier at the junction is lowered by an amount equal to the given forward biasing voltage. Both the holes from the p-side and electrons from the n-side cross the junction simultaneously and constitute a forward current **(injected minority current** – due to holes crossing the junction and entering the N-side of the diode**),** due to electrons crossing the junction and entering the P-side of the diode). Assuming the current flowing through the diode to be very large, the diode can be approximated as short-connected to the anode (p-side) and the +ve terminal of the input supply is connected to the cathode (n-side) then the diode is said to be reverse biased. In this condition, an amount equal to the reverse biasing voltage increases the height of the potential barrier at the junction. Both the holes on the p-side and electrons on the n-side tend to move away from the junction thereby increasing the depleted region. However, the process cannot continue indefinitely, thus a small current called **reverse saturation current** continues to flow in the diode. This small current is due to thermally generated carriers. Assuming the current flowing through the diode to be negligible, the diode can be approximated as an open-circuited switch.

The volt-ampere characteristics of a diode are explained by the following equation:

$\mathbf{I = I_o e^{\frac{V}{\eta V_T}}}$

I=current flowing in the diode

I_o=reverse saturation current

V=voltage applied to the diode

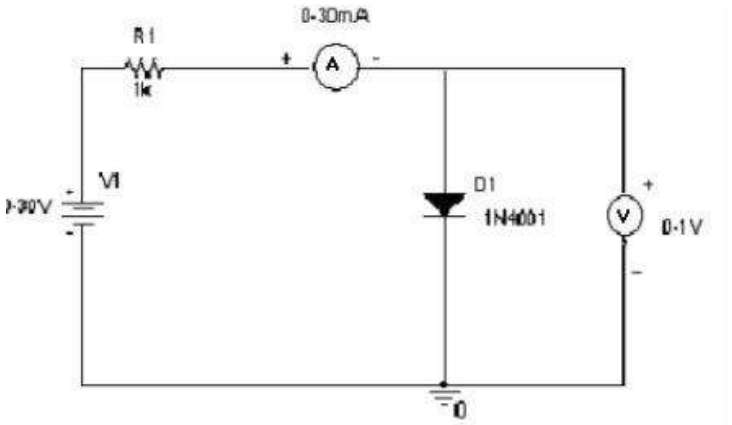
V_T=volt-equivalent of temperature=$\frac{kT}{q}$=$\frac{T}{11,600}$=26mV(at room temp).

η=1 (for Ge) and 2 (for Si)

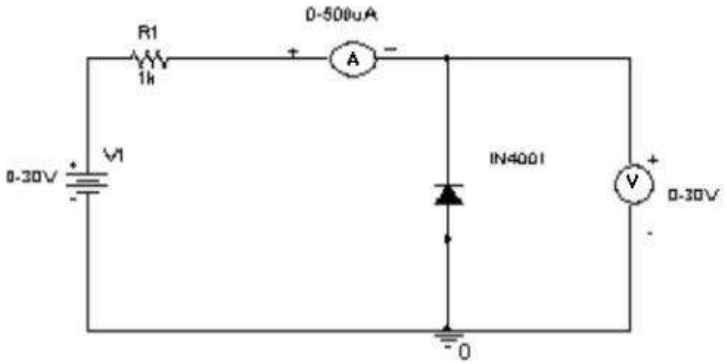
It is observed that the Ge diode has a smaller cut-in-voltage when compared to the Si diode. The reverse saturation current in the Ge diode is larger in magnitude when compared to the silicon diode.

Circuit Diagram:

Forward Bias:



Reverse Bias:



Precautions:

1. While experimenting, do not exceed the ratings of the diode. This may lead to damage to the diode.
2. Connect the voltmeter and Ammeter in the correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

Experiment:

Forward Biased Condition:

1. Connect the PN Junction diode in forward bias i.e; Anode is connected to the positive of the power supply and the cathode is connected to the negative of the power supply.
2. Use a Regulated power supply of range (0-30)V and a series resistance of 1kΩ.
3. For various values of forward voltage (V_r) note down the corresponding values of forward current (I_f).

Reverse biased condition:

1. Connect the PN Junction diode in Reverse bias i.e; the anode is connected to the negative of the power supply and the cathode is connected to the positive of the power supply.
2. For various values of reverse voltage (V_r) note down the corresponding values of reverse current (I_r).

Tabular Column:

Forward Bias:

S.No	V_f (volts)	I_f (mA)
01		
02		
03		
04		
05		
06		

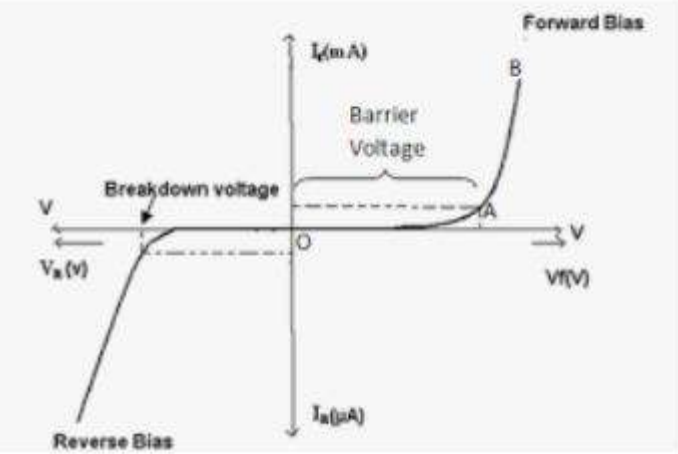
Reverse Bias:

S. No	V_r(volts)	I_r (µA)
01		
02		
03		
04		
05		

Graph (instructions):

1. Take a graph sheet and divide it into 4 equal parts. Mark the origin at the centre of the graph sheet.
2. Now mark +ve x-axis as V_f
   -ve x-axis as V_r
   +ve y-axis as I_f
   -ve y-axis as I_r.
3. Mark the readings tabulated for the diode forward biased condition in the firstQuadrant and the diode reverse the biased condition in the Third Quadrant.

Graph:



Calculations from Graph:

Static forward Resistance $R_{dc}= \frac{V_f}{I_f}$ Ω

Dynamic forward Resistance $r_{ac}= \frac{\Delta V_f}{\Delta I_f}$ Ω

Static Reverse Resistance $R_{dc} = \frac{V_r}{I_r}$ Ω

Dynamic Reverse Resistance $r_{ac}= \frac{\Delta V_r}{\Delta I_r}$ Ω

Result:

Thus, the VI characteristics of the P-N junction diode are verified.

1. Cut in voltage = …… V
2. Static forward resistance = ……. Ω
3. Dynamic forward resistance = ……. Ω

Conclusion:

EXPERIMENT NO: 03

EXPERIMENT NAME: To study of V-l Characteristics curve of a Zener diode.

Objective:

1. To plot Volt-Ampere characteristics of the Zener diode.
2. To find Zener break down the voltage in reverse biased condition.

Hardware Required:

S.No	Apparatus	Type	Range	Quant ity
01	Zener Diode	IZ6.2		1
02	Resistance		1k ohm	1
03	Regulated power supply		(0 – 30V)	1
04	Ammeter	mC	(0-30)mA, (0-500)µA	1
05	Voltmeter	mC	(0 – 1)V, (0 –30)V	1
06	Breadboard and connecting wires			

Introduction:

An ideal P-N Junction diode does not conduct in reverse-biased conditions. A **Zener diode** conducts excellently even in reverse-biased conditions. These diodes operate at a precise value of voltage called the breakdown voltage. A **Zener diode** when forward biased behaves like an ordinary P-N junction diode.

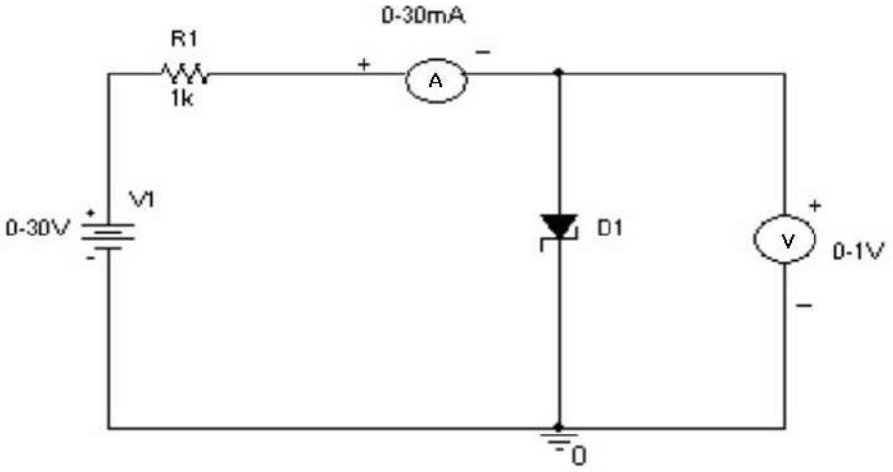
A **Zener diode** when reverse biased can either undergo **avalanche breakdown** or **Zener breakdown**.

Avalanche breakdown: If both p-the side and n-side the diode is lightly doped, and the depletion region at the junction widens. Application of a very large electric field at the junction may rupture covalent bonding between electrons. Such rupture leads to the generation of a large number of charge carriers resulting in avalanche multiplication.

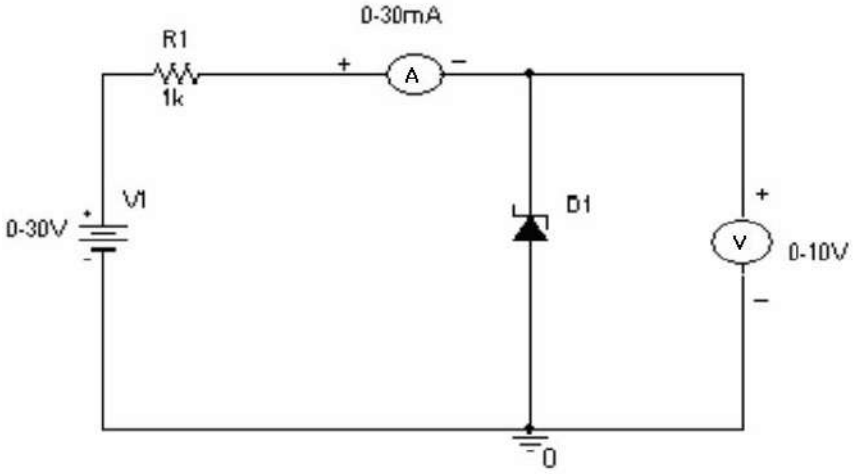
Zener breakdown:If both the p-side and n-side of the diode are heavily doped, the depletion region at the junction reduces. The application of even a small voltage at the junction ruptures covalent bonding and generates a large number of charge carriers.

Such a sudden increase in the number of charge carriers results in a **Zener mechanism**.

Circuit Diagram:
Forward Bias:



Reverse Bias:



Precautions:

1. While experimenting, do not exceed the ratings of the diode. This may lead to damage to the diode.
2. Connect the voltmeter and Ammeter in the correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

Experiment:
Forward Biased Condition:

1. Connect the Zener diode in forward bias i.e; the anode is connected to the positive of the power supply and the cathode is connected to the negative of the power supply as in the circuit.
2. Use a Regulated power supply of range (0-30)V and a series resistance of 1kΩ.
3. For various values of forward voltage (V_f) note down the corresponding values of forward current(I_f).

Reverse Biased condition:

1. Connect the Zener diode in Reverse bias i.e; the anode is connected to the negative of the power supply and the cathode is connected to the positive of the power supply as in the circuit.
2. For various values of reverse voltage(V_r) note down the corresponding values of reverse current (I_r).

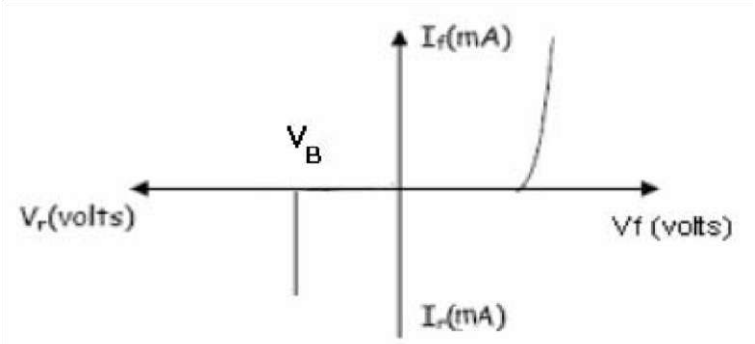
Tabular Column:
Forward Bias:

S.No	Vf(volts)	If(µA)

Reverse Bias:

S.No	Vr(volts)	Ir(µA)

MODEL GRAPH



Calculations from Graph:

Cut in voltage = ---------- (v)
Break down voltage = ----------(v)

Result:
The Zener diode characteristics have been plotted.

1. Cut in voltage = …… V
2. Break down voltage = ----------(v)

Conclusion:

EXPERIMENT NO: 04
EXPERIMENT NAME: To study of Half-Wave Rectification circuit.

Objective:

1. To plot the Output waveform of the Half Wave Rectifier.
2. To find the ripple factor for Half Wave Rectifier using the formulae.
3. To find the efficiency, V_p(rect), V_{dc} for Half Wave Rectifier.

Hardware Required:

S. No	Apparatus	Type	Range	Quantity
01	Transformer		6-0-6 V	1
02	Resistance		470Ω	1
03	Capacitor		470µF	1
04	Diode	IN4001		1
05	Bread Board and Connecting wires			

Introduction:

A device that is capable of converting a sinusoidal input waveform into a unidirectional waveform with a non-zero average component is called a rectifier.

A practical half-wave rectifier with a resistive load is shown in the circuit diagram. During the positive half cycle of the input, the diode conducts and all the input voltage is dropped across RL. During the negative half cycle, the diode is reverse biased and is in an OFF state and so the output voltage is zero.

The filter is simply a capacitor connected from the rectifier output to the ground. The capacitor quickly charges at the beginning of a cycle and slowly discharges through RL after the positive peak of the input voltage. The variation in the capacitor voltage due to charging and discharging is called ripple voltage. Generally, ripple is undesirable, thus the smaller the ripple, the better the filtering action.

The ripple factor is an indication of the effectiveness of the filter and is defined as $R=V_r(pp)/V_{dc}$

Where $V_r(pp)$ = Ripple voltage

V_{dc}= Peak rectified voltage.

The ripple factor can be lowered by increasing the value of the filter capacitor or increasing the load capacitance.

MATHEMATICAL ANALYSIS (Neglecting R_f and R_s)

Let Vac = $V_m \sin\omega t$ is the input AC signal, the current I_{ac} flows only for one-half cycle i.e from ωt

= 0 to $\omega t = \pi$,whereas it is zero for the duration $\pi \leq \omega t \leq 2\pi$

Therefore, I_{ac} = = $I_m \sin\omega t$ $0 \leq \omega t \leq 2\pi$

= 0 $\pi \leq \omega t \leq 2\pi$

Where,

I_m = maximum value of current

V_m = maximum value of voltage

AVERAGE OR DC VALUE OF CURRENT

$V_{dc} = \frac{Vm}{\pi}$

The RMS VALUE OF CURRENT

$V_{rms} = \frac{Vm}{2}$

RECTIFICATION FACTOR:

The ratio of output DC power to the input AC power is defined as the efficiency

Output power = $I_{2dc}R$

Input power = $I_{2rms}(R+R_f)$

Where R_f - forward resistance of the diode

$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{2dc}R}{I_{2rms}\ (R+R_f)}$

PERCENTAGE OF REGULATION:

It is a measure of the variation of AC output voltage as a function of DCoutput Voltage

Percentage of regulation

V_{NL} = Voltage across load resistance, When minimum current flows through it.

V_{FL} = Voltage across load resistance, When maximum current flows through. For an ideal half-wave rectifier, the percentage regulation is 0%. For a practical half wave

$$\frac{V_{NL} - V_{FL}}{V_{FL}} * 100\%$$

$$V_{NL} = \frac{V_m}{\pi}$$

$$V_{FL} = \frac{Vm}{\pi} - I_{dc}(R + R_f)$$

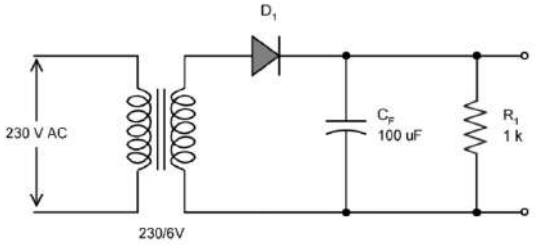
Peak - inverse - voltage PIV:

It is the maximum voltage that has to be withstood by a diode when it is reverse biased

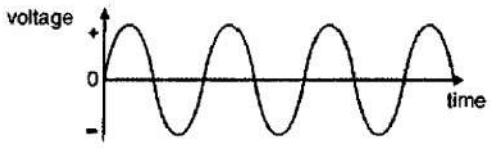
PIV = V_m

CIRCUIT DIAGRAM OF HALF-WAVE RECTIFIER WITH FILTER:

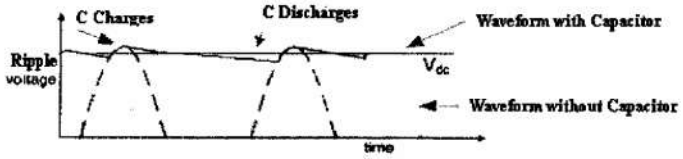
Half wave rectifier with filter:



MODEL GRAPH:



Input Waveform



Resultant Output Waveform

Precautions:

1. While experimenting do not exceed the ratings of the diode. This may lead to damage to the diode.
2. Connect CRO using probes properly as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

Experiment:

1. Connections are given as per the circuit diagram without a capacitor
2. Apply AC main voltage to the primary of the transformer. Feed the rectified output voltage to the CRO and measure the time period and amplitude of the waveform.
3. Now connect the capacitor in parallel with the load resistor and note down the amplitude and timeperiod of the waveform.
4. Measure the amplitude and timeperiod of the transformer secondary(input waveform) by connecting CRO.
5. Plot the input, and output without filter and with filter waveform on a graph sheet.
6. Calculate the ripple factor.

Graph (instructions):

1. Take a graph sheet and divide it into 2 equal parts. Mark the origin at the centre ofthe graph sheet.
2. Now mark the x-axis as Time, the y-axis as Voltage
3. Mark the readings tabulated for Amplitude as Voltage and Time in the graphsheet.

Formula:

Peak to Peak Ripple Voltage, $V_r(pp)=(1/fR_{LC})Vp(rect)$
$V_p(rect)$ = Unfiltered Peak Rectified Voltage
$V_{dc}=(1-1/(2fRLC))V_p(rect)$
Ripple Factor = $V_{r(pp)}/V_{dc}$

Observations:

	Input Waveform	Output Waveform	Ripple Voltage
Amplitude			
Time Period			
Frequency			

Result:

The Rectified output Voltage of Half Wave Rectifier Circuit is observed and the calculated value of the ripple factor is _____

Conclusion:

EXPERIMENT NO: 05
EXPERIMENT NAME: To study of Full-Wave Rectification circuit (Center-tapped)

Objective:

1. To plot the Output waveform of the Full Wave Rectifier.
2. To find ripple factor for Full Wave Rectifier using the formulae.
3. To find the efficiency, V_p(rect), V_{dc} for Full Wave Rectifier.

Hardware Required:

S. No	Apparatus	Type	Range	Quantity
01	Transformer		6-0-6 V	1
02	Resistance		470 ohm	1
03	Capacitor		470μF	1
04	Diode	IN4001		2
05	Breadboard and connecting wires			

Introduction:

A device capable of converting a sinusoidal input waveform into a unidirectional waveform with a non-zero average component is called a rectifier.

A practical half-wave rectifier with a resistive load is shown in the circuit diagram. It consists of two half-wave rectifiers connected to a common load. One rectifies during the positive half cycle of the input and the other rectifies the negative half cycle. The transformer supplies the two diodes (D1 and D2) with sinusoidal input voltages that are equal in magnitude but opposite in phase. During the input positive half cycle, diode D1 is ON and diode D2 is OFF. During the negative half cycle, D1 is OFF and diode D2 is ON. Generally, ripple is undesirable, thus the smaller the ripple, the better thefiltering action.

The ripple factor is an indication of the effectiveness of the filter and is defined as

$R=V_{r(pp)}/V_{dc}$

Where, $V_{r(pp)}$ = Ripple voltage

V_{dc}= Peak rectified voltage.

The ripple factor can be lowered by increasing the value of the filter capacitor or increasing the load capacitance.

MATHEMATICAL ANALYSIS (Neglecting R_f and R_s)

The current through the load during both half cycles is in the same direction and hence it is the sum of the individual currents and is unidirectional Therefore, I = Id1 + Id2 The individual currents and voltages are combined in the load and therefore their average values are double that obtained in a half wave rectifier circuit.

AVERAGE OR DC VALUE OF CURRENT I_{dc}

$$I_{dc} = 1/2\pi \left[\int_0^{\pi} I_m(sin\omega t)d\omega t - \int_{\pi}^{2\pi} I_m(sin\omega t)d\omega t\right] = 2\, I_m/\pi$$

Similarly,

$$V_{dc} = 2V_m/\pi$$

The RMS VALUE OF CURRENT

$= \sqrt{\pi \int_0^{2\pi} \quad {I_m}^2 \, sin \quad ^2\omega t \, d\omega t}$

$= \frac{I_m}{\sqrt{2\pi}}$

Similarly, $V_{rms} = \frac{V_m}{\sqrt{2\pi}}$

RECTIFICATION FACTOR

The ratio of output DC power to the input AC power is defined as the efficiency

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{V_{dc} * I_{dc}}{V_{rms}\sqrt{{I_{ac}}^2 + {I_{dc}}^2}} * 100$$

η= 81% (if R >>Rf . then Rf can be neglected)

PERCENTAGE OF REGULATION

It is a measure of the variation of AC output voltage as a function of DC output Voltage.

$$\frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

For an ideal Full-wave rectifier. The percentage regulation is 0%.
Peak - Inverse - Voltage (PIV)
It is the maximum voltage that has to be withstood by a diode when it is reverse biased
PIV = 2Vm

Advantages of Full wave Rectifier

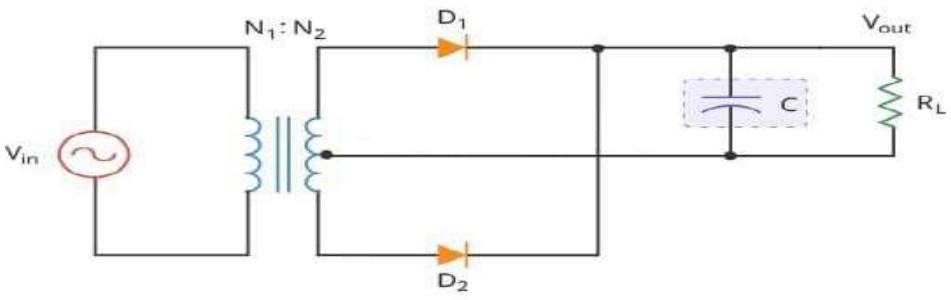
1.γ is reduced
2.η is improved

Disadvantages of Full wave Rectifier

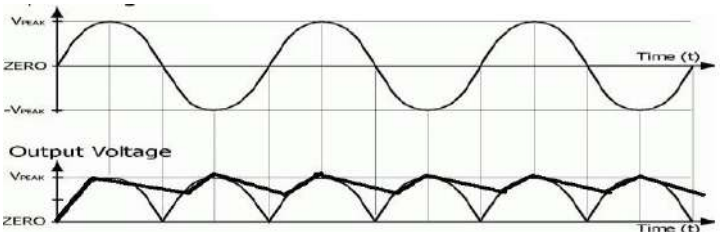
1. Output voltage is half the secondary voltage
2. Diodes with high PIV ratings are used

Manufacturing centre-tapped transformer is quite expensive and so Full wave rectifier with

CIRCUIT DIAGRAM ON FULL-WAVE RECTIFIER WITH FILTER:



MODEL GRAPH:



Precautions:

1. While experimenting, do not exceed the ratings of the diode. This maylead to damage to the diode.
2. Connect CRO using probes properly as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuitconnections as per the circuit diagram.

Experiment:

1. Connections are given as per the circuit diagram without a capacitor.
2. Apply AC main voltage to the primary of the transformer. Feed the rectified output voltage to the CRO and measure the time period and amplitude of the waveform.
3. Now connect the capacitor in parallel with the load resistor and note down theamplitude and time period of the waveform.
4. Measure the amplitude and time period of the transformer secondary (inputwaveform) by connecting CRO.
5. Plot the input, and output without filter and with filter waveform on a graph sheet.
6. Calculate the ripple factor.

GRAPH (Instructions):

1. Take a graph sheet and divide it into 2 equal parts. Mark the origin at the centre of the graph sheet.
2. Now mark the x-axis as Time, the y-axis as Voltage
3. Mark the readings tabulated for Amplitude as Voltage and Time in the graphsheet.

Formula:

Peak to Peak Ripple Voltage, $V_r(pp) = ½fR_{LC}V_p(rect)$

$V_p(rect)$ = Unfiltered Peak Rectified Voltage

$V_{dc} = (1-\frac{1}{4}fR_{LC})V_p(rect)$

Ripple Factor = $\frac{Vr(pp)}{Vdc}$

Observations:

	Input Waveform	**Output Waveform**	**Ripple Voltage**
Amplitude			
Time Period			
Frequency			

Result:
The Rectified output Voltage of the Full Wave Rectifier Circuit is observed and the calculated value of the ripple factor is _____

Conclusion:

EXPERIMENT NO: 06
EXPERIMENT NAME: To study of Full-Wave Rectification circuit (Bridge)

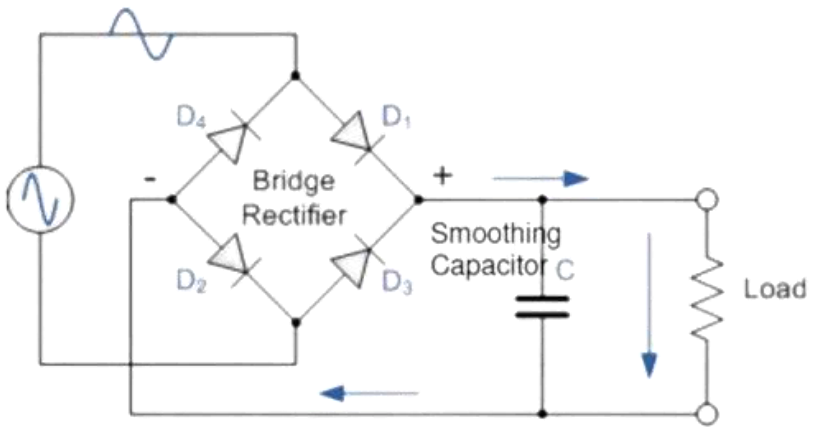
Objective:
1. To plot the Output waveform of the Full Wave Bridge Rectifier.
2. To find the ripple factor for the Full Wave Bridge Rectifier using the formulae.
3. To find the efficiency, Vp(rect), Vdc for Full Wave Bridge Rectifier.

Hardware Required:

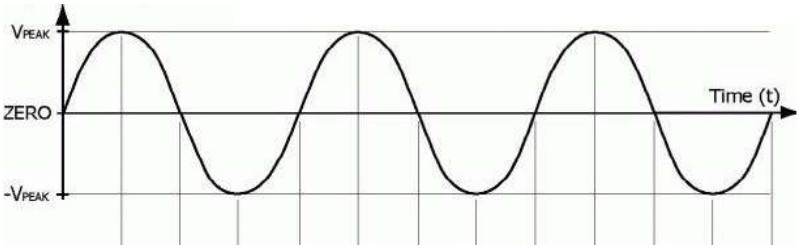
S.No	Apparatus	Type	Range	Quantity
01	Transformer		6-0-6 V	1
02	Resistance		470 ohm	1
03	Capacitor		470µF	1
04	Diode	IN4001		4
05	Breadboard and Connecting wires			

Introduction:
A device that is capable of converting a sinusoidal input waveform into a unidirectional waveform with non-zero average components is called a rectifier. The Bridge rectifier is a circuit, which converts an ac voltage to a dc voltage using both half cycles of the input ac voltage. The Bridge rectifier has four diodes connected to form a Bridge. The load resistance is connected between the other two ends of the bridge. For the positive half cycle of the input ac voltage, diode D1 and D3 conducts whereas diodes D2 and D4 remain in the OFF state. The conducting diodes will be in series with the load resistance RL and hence the load current flows through RL. For the negative half cycle of the input ac voltage, diodes D2 and D4 conduct whereas diodes D1 and D3 remain in the OFF state. The conducting diodes will be in series with the load resistance RL and hence the load current flows through RL in the same direction as in the previous half cycle. Thus, a bidirectional wave is converted into a unidirectional wave.
The ripple factor is an indication of the effectiveness of the filter and is defined as
$R=V_r(pp)/V_{dc}$
Where, $V_r(pp)$ = Ripple voltage
V_{dc}= Peak rectified voltage.
The ripple factor can be lowered by increasing the value of the filter capacitor or increasing the load capacitance.

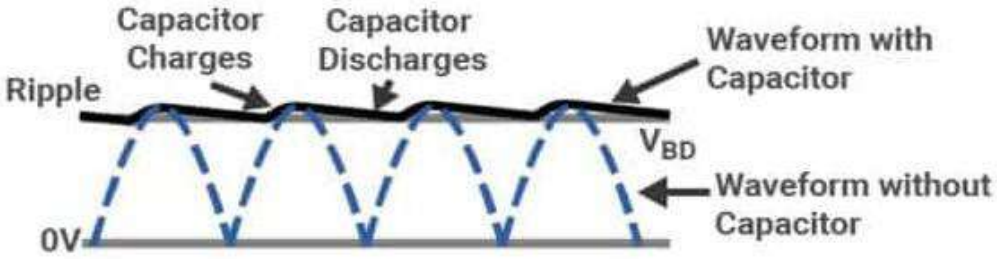
CIRCUIT DIAGRAM OF FULL WAVE BRIDGE RECTIFIER WITH FILTER:



MODEL GRAPH:



Input waveform



Output waveform

Precautions:

1. While experimenting, do not exceed the ratings of the diode. This may lead to damage to the diode.
2. Connect CRO using probes properly as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

Experiment:

1. Connections are given as per the circuit diagram without a capacitor.
2. Apply AC main voltage to the primary of the transformer. Feed the rectified outputvoltage to the CRO and measure the time period and amplitude of the waveform.
3. Now connect the capacitor in parallel with the load resistor and note down the amplitudeand time period of the waveform.
4. Measure the amplitude and time period of the transformer secondary (input waveform) by connecting CRO.
5. Plot the input, the output without filter and with filter waveform on a graph sheet.
6. Calculate the ripple factor.

Graph:

1. Take a graph sheet and divide it into 2 equal parts. Mark the origin at the centre of the graph sheet.
2. Now mark the x-axis as Time, the y-axis as Voltage
3. Mark the readings tabulated for Amplitude as Voltage and Time in the graph sheet.

Formula:

Peak to Peak Ripple Voltage, $V_r(pp)=(1/2fR_{LC})V_p(rect)$

$V_{p(rect)}$ = Unfiltered Peak Rectified Voltage

$V_{dc}=(1-1/(4fRLC))V_p(rect)$

Ripple Factor = $V_{r(pp)}/V_{dc}$

Observations:

	Input Waveform	**Output Waveform**	**Ripple Voltage**
Amplitude			
Time Period			
Frequency			

Result:

The Rectified output Voltage of the Full Wave Rectifier Circuit is observed and the calculated value of the ripple factor is _____

Conclusion:

EXPERIMENT NO: 07

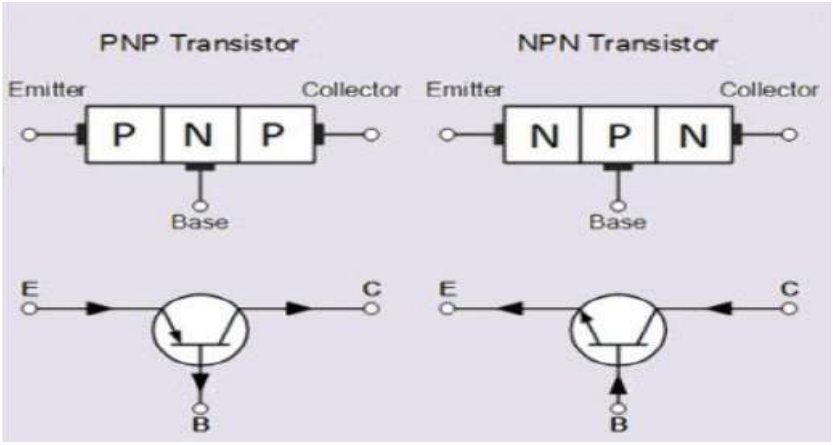
EXPERIMENT NAME: To familiar with NPN and PNP Transistors.

Objective:

To become familiar with the theory of operation of bipolar junction transistors (BJT) and its applications.

Introduction

A transistor is a semiconductor device used to amplify and switch electronic signals and electrical power. It is composed of semiconductor material with at least three terminals for connection to an external circuit. A voltage or current applied to one pair of the transistor's terminals changes the current through another pair of terminals. Because the controlled (output) power can be higher than the controlling (input) power, a transistor can amplify a signal.



Transistors types

1. Bipolar Transistor Example: Bipolar junction transistor
2. Unipolar Transistor Example: Field effect transistor, Uni junction transistor

Bipolar junction transistor:

The Bipolar junction transistor is a solid-state device and in the BJTs the current flow into two terminals, they are the emitter and collector, and the amount of current is controlled by the third terminal i.e. base terminal. It is different from the other type of transistor i.e. Field-effect transistor which is the output current controlled by the input voltage.

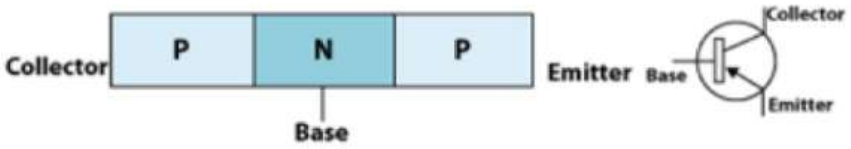
Types of Bipolar Junction Transistors:

- PNP junction transistors
- NPN junction transistors

PNP Junction Transistor:

In the PNP transistors, the emitter is more positive with the base and also with respect to the collector. The PNP transistor is a three-terminal device that is made from semiconductor material. The three terminals are the collector, base, and emitter and the transistor is used for switching and amplifying applications. The operation of the PNP transistor is shown below.

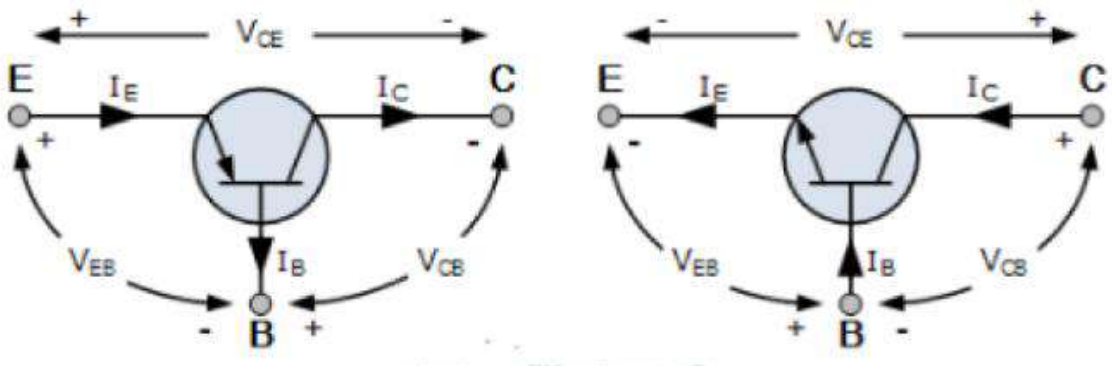
Generally, the collector terminal is connected to the positive terminal and the emitter to a negative supply with a resistor either the emitter or collector circuit. To the base terminal, the voltage is applied and it operates the transistor in an ON/OFF state. The transistor is in the OFF state when the base voltage is the same as the emitter voltage. The transistor mode is in an ON state when the base voltage decreases with respect to the emitter. By using this property the transistor can act on both applications like switch and amplifier. The basic diagram of the PNP transistor is shown below.



NPN Junction Transistor:

The NPN transistor is exactly opposite to the PNP transistor. The NPN transistor contains three terminals which are the same as the PNP transistor which is the emitter, collector, and base. Generally, the positive supply is given to the collector terminal, and the negative supply is to the emitter terminal with a resistor either the emitter or collector or emitter circuit. To the base terminal, the voltage is applied and it operated as an ONN/OFF state of a transistor. The transistor is in an OFF state when the base voltage is the same as the emitter. If the base voltage is increased with respect to the emitter then the transistor mode is in the ON state. By using this condition the transistor can act like both applications which are amplifier and switch. The basic symbol and the NPN configuration diagram as shown below.

Working Principle of BJT



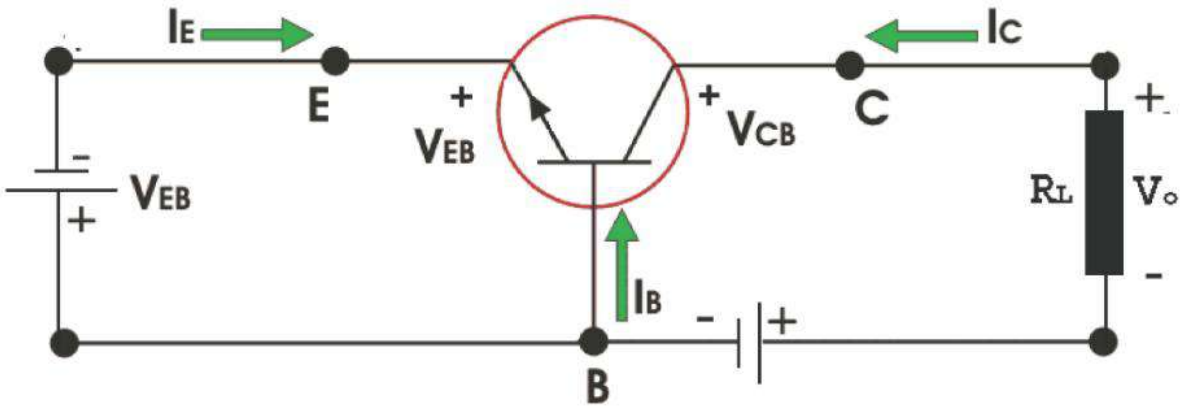
The BE junction is forward bias and the CB is a reverse bias junction. The width of the depletion region of the CB junction is higher than the BE junction. The forward bias at the BE junction decreases the barrier potential and produces electrons to flow from the emitter to the base is thin and lightly doped it has very few holes and less amount of electrons from the emitter about 2% it recombines in the base region with holes and from the base terminal it will flow out. This initiates the base current flow due to the combination of

electrons and holes. The leftover large number of electrons will pass the reverse bias collector junction to initiate the collector current. By using KCL we can observe the mathematical equation,

$$I_E = I_B + I_C$$

The base current is very less as compared to emitter and collector current

Here the operation of the PNP transistor is the same as the NPN transistor the only difference is only holes instead of electrons. The below diagram shows the PNP transistor of the active mode region.



Advantages of BJT:

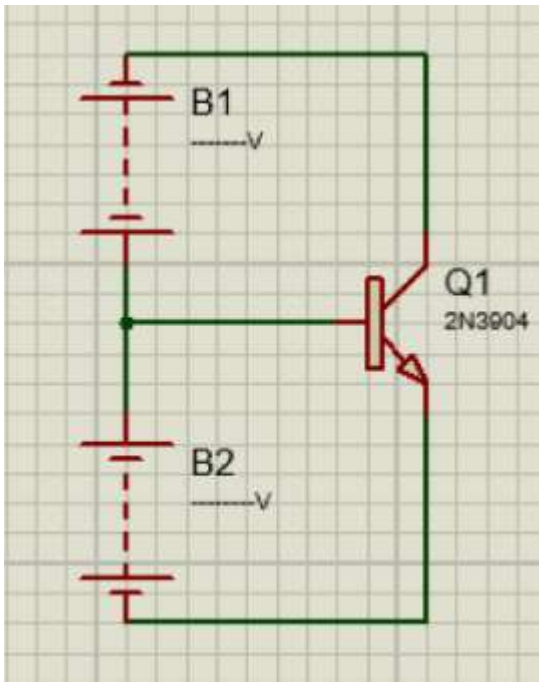
1. High driving capability
2. High-frequency operation
3. An emitter-coupled logic used in BJTs as a digital switch

Applications of BJT:

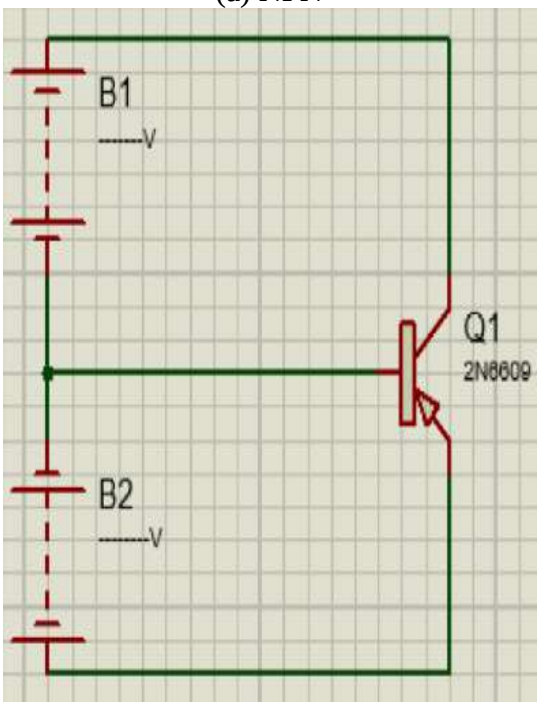
Following are the two different types of applications in BJT they are

1. Switching
2. Amplification

Circuit Diagrams:



(a) NPN



(b) PNP

Practical Work:

Equipment:

1. DMM
2. Breadboard
3. Transistor

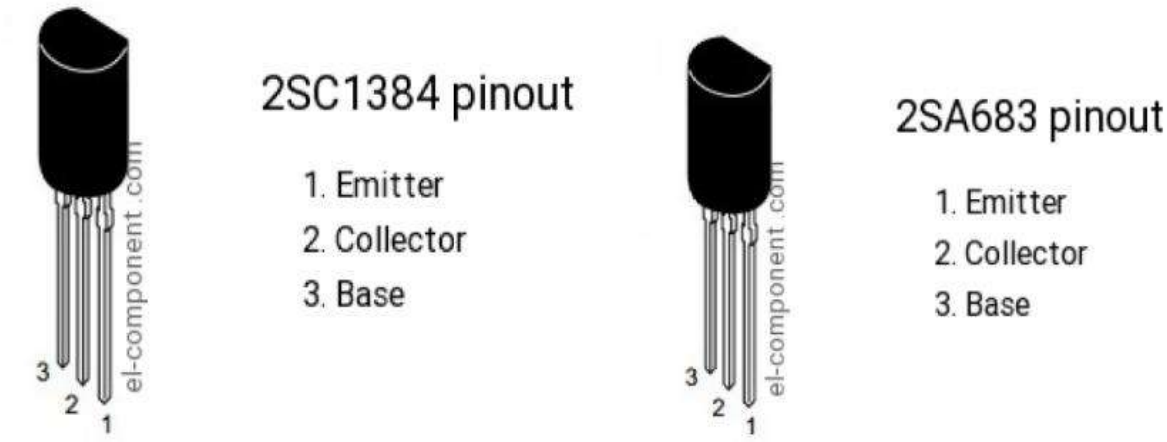
2SC1384 ----------NPN

A683 ---------- PNP

Procedure:

Verify the transistor type for each unit by checking the polarity of the base-emitter junction. Use a Fluke DMM in diode-test mode. Tabulate your measured data.

For the given transistor (c1384 & 2SA683), measure the forward and reverse bias resistance between Base and Emitter, Base and Collector, and Collector and Emitter. Use a Fluke DMM in diode-test mode. The lead connection of this transistor is shown in Fig.



Results:

(a) NPN		(b) PNP
VEC = 0 V	VEC =	0 V
VCE = 0 V	VCE =	0 V
VEB = 0 V	VEB =	0.699 V
VBE = 0.688 V	VBE =	0 V
VCB = 0 V	VCB =	0.695 V
VBC = 0.687 V	VBC =	0 V

Discussion:

- Bipolar transistors are so named because the controlled current must go through two types of semiconductor material: P and N. The current consists of both electron and hole flow, in different parts of the transistor.
- Bipolar transistors consist of either a P-N-P or an N-P-N semiconductor "sandwich" structure.
- The three leads of a bipolar transistor are called the Emitter, Base, and Collector.
- Transistors function as current regulators by allowing a small current to control a larger current. The amount of current allowed between the collector and emitter is primarily determined by the amount of current moving between the base and the emitter.

- In order for a transistor to properly function as a current regulator, the controlling (base) current and the controlled (collector) currents must be going in the proper directions: meshing additively at the emitter and going in the direction of the emitter arrow symbol.

Conclusion:

A single NPN BJT was used to drive this differential amplifier. The collector current entering the NPN BJT will be the current source driving the differential amplifier. The transistor is a good component to get an amplified current using a very small current. Dc current gain increases as Voltage increases. But Dc current gain for the same voltage with the different base current is the same. Each part has a different base current but if DC current gain is found for the same voltage on different curves it will come out to be about the same.

EXPERIMENT NO: 08
EXPERIMENT NAME: To study of Full-Wave filter circuit.

Objective:

1. To study the operation of a Full wave rectifier with filters
2. To find its:
    a. Ripple Factor
    b. Percentage Regulation

Hardware Required:

S.No	Apparatus	Type	Range	Quantity
01	Diodes	1N4007(Si)		2
02	Resistance		1 K ohm	1
03	Capacitor		100μF	2
04	Inductor		35 mH	1
05	CRO		(0-20) MHz	1
06	CRO Probes			2
07	Digital Ammeter, Voltmeter		(0-200μA/200mA), (0-20 V)	1
08	Transformer		200 V/9 V, 50 Hz	1
09	Connecting wires			

Introduction:

A rectifier is a circuit that converts a pure AC signal into a pulsating DC signal or asignal that is a combination of AC and DC components. In DC supplies, a rectifier is oftenfollowed by a filter circuit which converts the pulsating DC signal into a pure DC signalbyremoving the AC component. An L-section filter consists of an inductor and a capacitor
connected in the form of an inverted L. A π- section filter consists of two capacitors andoneinduction in the form symbol pi.

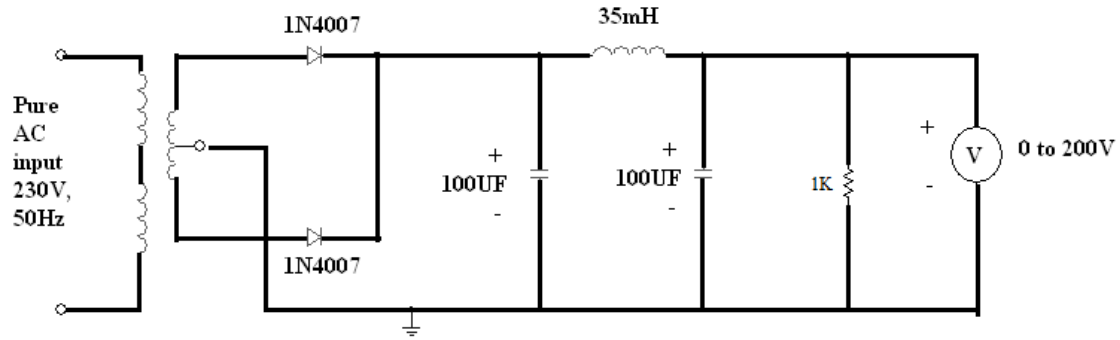
Ripple Factor:

The ripple factor is defined as the ratio of the effective value of AC components to theaverage DC value. It is denoted by the symbol 'γ'.

$\gamma_{LWRL\pi-section} = \frac{V_{AC}}{V_{DC}} = \sqrt{2}\frac{X_{C1}X_{C2}}{R\,X_L}$, where $X_L = 2\omega L$, $X_c = \frac{1}{2\omega C}$

Circuit Diagram:

Full Wave Rectifier (with π-section filter):



Procedure:

1. Connect the circuit as shown in the figure.
2. Repeat the above steps 2-6
3. Plot different graphs for waveforms and calculate the ripple factor.

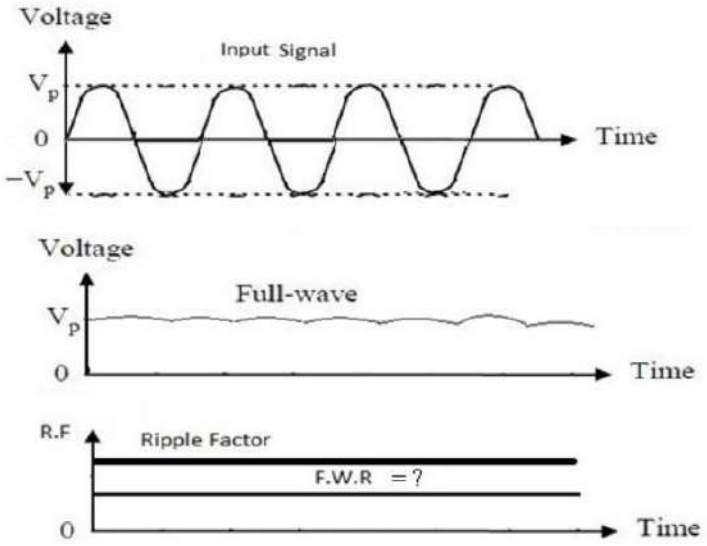
Observations:

Load Resistance (R_L)	V_{AC}(V)	V_{DC}(V)	Ripple Factor $\gamma=\frac{Vac}{Vdc}$	Input Signal		Output Signal	
				Vm p-p(v)	Frequency (Hz)	Vm p-p(v)	Frequency (Hz)

Calculations:

1. Ripple factor: $FWR\pi\text{–}Section=\frac{V_{AC}}{V_{DC}}$
2. Percentage Regulation: $\frac{V_{DCNL}-V_{DCFL}}{V_{DCFL}}\times$ 100%

Expected Waveforms:



Results:

Full Wave rectifier characteristics are studied.

1. Ripple factor of Half wave with L-section filter = ----------
2. Ripple factor of Full wave with π-section filter = ----------
3. Regulation of Half wave with L-section filter = ----------
4. Regulation of Half wave with π -section filter = ----------

EXPERIMENT NO: 9
EXPERIMENT NAME: To study Common Emitter (CE) Transistor Amplifier circuits.

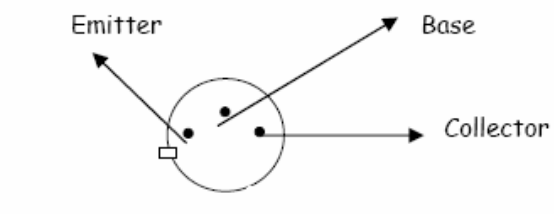
Objective:
To study the input and output characteristics of a bipolar junction transistor in a common emitter configuration.

Hardware Required:

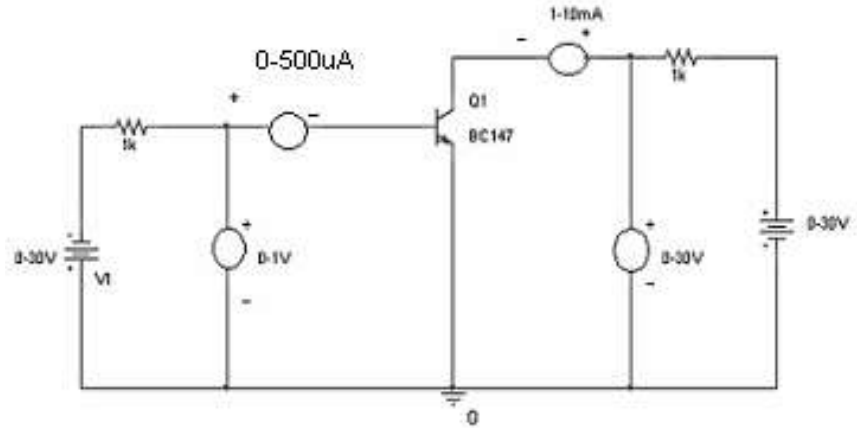
S. No	Apparatus	Type	Range	Quantity
01	Transistor	BC147		1
02	Resistance		1K ohm	2
03	Regulated power supply		0-30 V	2
04	Ammeter	mC	(1-10)mA, (0-500)mA	1
05	Voltmeter	mC	(0-1)V, (0-30)V	1
06	Breadboard and connecting wires			

Introduction:
A bipolar junction transistor (BJT) is a 3-terminal (emitter, base, collector) semiconductor device. There are two types of transistors namely NPN and PNP. It consists of two P-N junctions namely the emitter junction and the collector junction. In Common Emitter configuration the input is applied between the base and emitter and the output is taken from the collector and emitter. Here emitter is common to both input and output and hence the name common emitter configuration. Input characteristics are obtained between the input current and input voltage taking output voltage as the parameter. It is plotted between VBE and IB at constant VCE in CE configuration. Output characteristics are obtained between the output voltage and output current taking the input current as the parameter. It is plotted between VCE and IC at constant IB in CE configuration.

Pin assignment:



Circuit Diagram:



Precautions:

1. While doing the experiment do not exceed the ratings of the transistor. This may lead to damage to the transistor.
2. Connect the voltmeter and Ammeter in the correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base, and collector terminals of the transistor.

Experiment:

Input Characteristics

1. Connect the transistor in CE configuration as per the circuit diagram
2. Keep output voltage V_{CE} = 0V by varying V_{CC}.
3. Varying V_{BB} gradually, note down both base current I_B andbase–emitter voltage (V_{BE}).
4. Repeat the above procedure (step 3) for various values of V_{CE}

Output Characteristics

1. Make the connections as per the circuit diagram.
2. By varying V_{BB} keep the base current I_B = 20μA.
3. Varying V_{CC} gradually, note down the readings of collector-current (I_C) and collector-emitter voltage (V_{CE}).
4. Repeat the above procedure (step 3) for different values of I_E

Tabular Column:

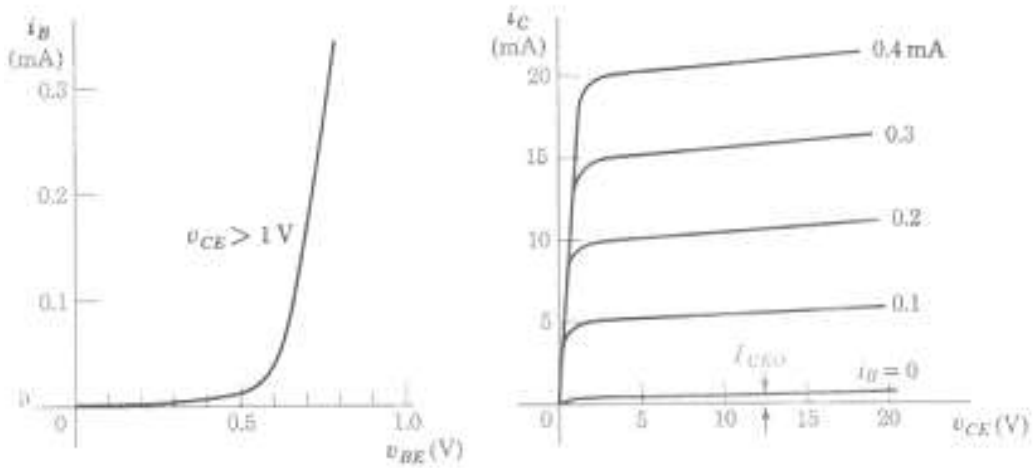
Input characteristics:

V_{CE} = 0 V		V_{CE} = 4V	
V_{BE} (volts)	I_B (mA)	V_{BE} (volts)	I_B (mA)

Output characteristics:

I_B = 30 µA		I_B = 60 µA	
V_{CE} (volts)	Ic (mA)	V_{CE} (volts)	Ic (mA)

Graphs:



Input characteristics **Output characteristics**

1. Plot the input characteristics by taking V_{BE} on Y-axis and IB on X-axis at constant V_{CE}.
2. Plot the output characteristics by taking V_{CE} on the x-axis and I_C on the y-axis by taking I_B as a constant parameter.

Calculations from graph:

1. Input resistance:

To obtain input resistance find ΔV_{BE} and ΔI_B at constant V_{CE} on one of the input characteristics.

Then $R_i = \frac{\Delta V_{BE}}{\Delta I_B}$ (V_{CE} constant)

2. Output resistance:

To obtain output resistance, find ΔI_C and ΔV_{CE} at constant I_B.

$R_o = \frac{\Delta V_{CE}}{\Delta I_C}$ (I_B constant)

Calculations from graph:

a) Input impedance(hic)= $\frac{\Delta V_{BE}}{\Delta I_B}$, V_{CE} constant.

b) Forward current gain(hfc)= $\frac{\Delta I_C}{\Delta I_B}$, V_{CE} constant

c) Output admittance(hoe)= $\frac{\Delta I_{\square}}{\Delta V_{\square\square}}$, I_B constant

d) Reverse voltage gain(hrc)= $\frac{\Delta V_{\square\square}}{\Delta V_{\square\square}}$, I_B constant

Inference:

1. Medium Input and Output resistances.
2. Smaller value of V_{CE} becomes earlier cut-in-voltage.
3. Increase in the value of I_B causes saturation of the transistor at an earlier voltage.

Result:

Thus the input and output characteristics of C_E configuration are plotted.

1. Input Resistance (R_i) = …….Ω
2. Output Resistance (R_o) = …….Ω

Conclusion:

EXPERIMENT NO: 10
EXPERIMENT NAME: To study of Clipping circuit.

Objective:
To study the clipping circuits for the following reference voltages and to verify the responses.

Hardware Required:

S. No	Apparatus	Type	Range
01	Diode		
02	Resistance		1K ohm
03	Power supply		0-30 V
04	CRO		
05	Function generator		
06	Breadboard and connecting wires		

Introduction:
The non-linear semiconductor diode in combination with the resistor can function as a clipper circuit. Energy storage circuit components are not required in the basic process of clipping. These circuits will select part of an arbitrary waveform that lies above or below some particular reference voltage level and that selected part of the waveform is used for transmission. So they are referred to as voltage limiters, current limiters, amplitude selectors, or slicers. There are three different types of clipping circuits.
1) Positive Clipping circuit.
2) Negative Clipping.
3) Positive and Negative Clipping (slicer).
In the positive clipping circuit positive cycle of the Sinusoidal signal is clipped and the negative portion of the sinusoidal signal is obtained in the output of reference voltage is added, instead of a complete positive cycle that portion of the positive cycle which is above the reference voltage value is clipped.
In the negative clipping circuit instead of the positive portion of the sinusoidal signal, the negative portion is clipped.
In the slicer, both positive and negative portions of the sinusoidal signal are clipped

1. Positive Clipping:

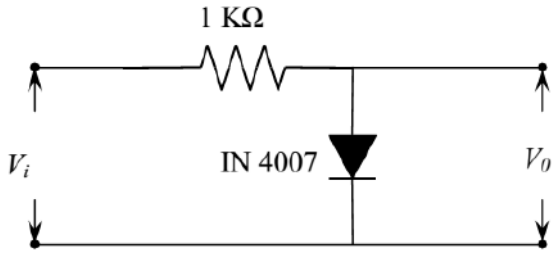


Figure:1

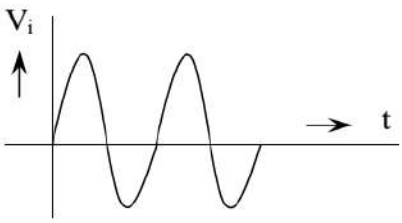


Figure: 2(a). Input waveform

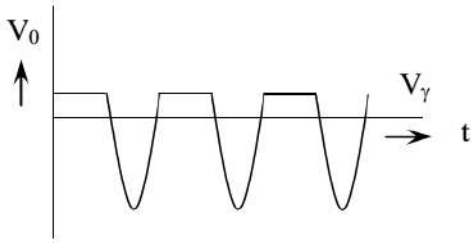


Figure: 2(b)Output waveform.

V_i is an input sinusoidal signal as shown in figure 2(a). For the positive portion of the sinusoidal, the diode gets forward-biased. The output voltages in the voltage across the diode under forward biased which are cut-in-voltage of the diode. Therefore the positive portion above the cut-in-voltage is clipped or not observed in the output (V_0) as shown in figure 2(b).

2. Positive clipping with positive reference voltage:

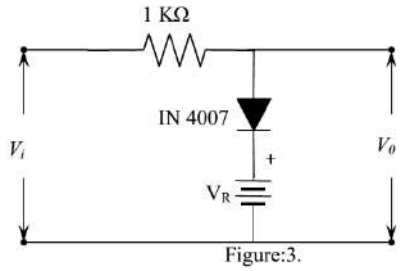


Figure:3.

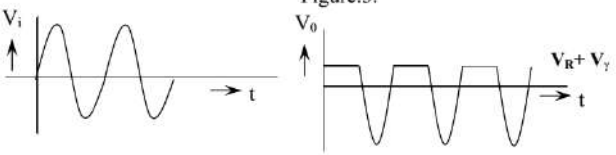


Figure:4(a). Input waveform

Figure:4(b). Output waveform.

The input sinusoidal signal (V_i) in figure 4(a) can make the diode conduct when its instantaneous value is greater than V_R. Up to that voltage (V_R), the diode is open-circuited and the output voltage is the same as the input voltage. After that voltage (V_R) the output voltage is V_R plus the cut-in-voltage (V_γ) of the diode as shown in figure 4(b).

3. Positive clipping with negative reference voltage:

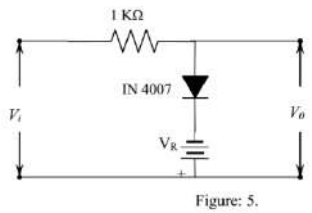


Figure: 5.

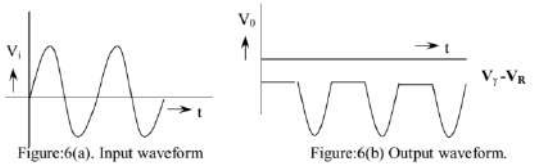


Figure:6(a). Input waveform

Figure:6(b) Output waveform.

In this circuit, the diode conducts the output voltage the same as the input voltage. The diode
conducts at a voltage less by V_R from cut-in-voltage called V_γ. For voltage less than V_γ, the diode is open-circuited and the output is the same as the input voltage.

4. Negative Clipping Circuit:

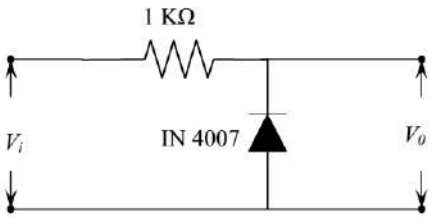


Figure:7.

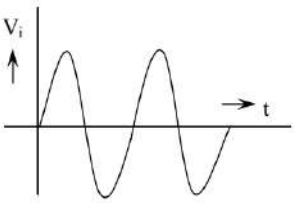


Figure:8 (a). Input waveform

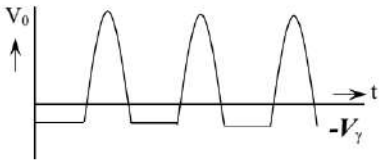


Figure:8 (b). Output waveform.

For this portion of the input sinusoidal signal (V_i), the diode gets reverse biased and it is open. Then the output voltage is the same as the input voltage. For the negative portion of the signal the diode gets forward biased and the output voltage is the cut-in-voltage (-Vγ)of the diode. Then the input sinusoidal variation is not seen in the output. Therefore the negative portion of the input sinusoidal signal (V_i)is clipped in the output signal (V_0)

5. Negative Clipping with Negative Reference Voltage:

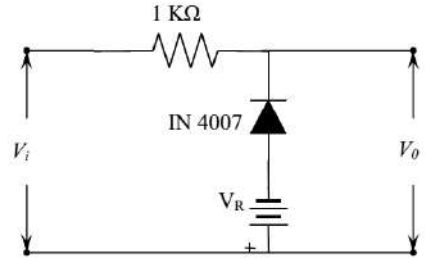


Figure:9

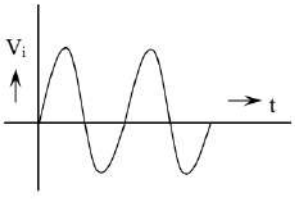


Figure:10(a). Input waveform.

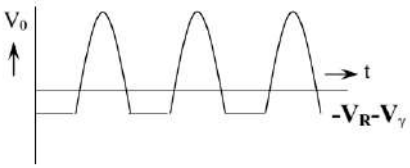


Figure:10(b) Output waveform.

In this circuit, the diode gets forward biased for the input sinusoidal voltage is less than ($-V_R$). For input voltage greater than ($-V_R$), the diode is non-conducting and it is open. Then the output voltage is the same as the input voltage.

6. Negative Clipping with Positive Reference Voltage:

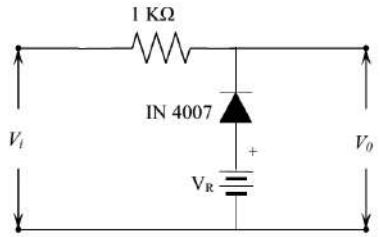


Figure:11.

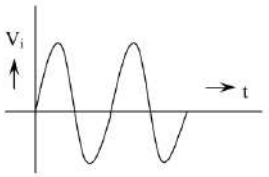


Figure:12(a) Input waveform

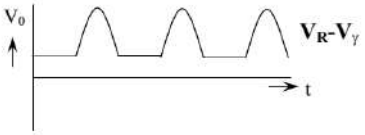


Figure:12(b) Output waveform.

For input sinusoidal signal voltage less than V_R, the diode is shorted and the output voltage is fixed at V_R. For input sinusoidal voltage greater than V_R the diode is reverse-biased and open-circuited. Then the output voltage is the same as the input voltage.

7. Slicer:

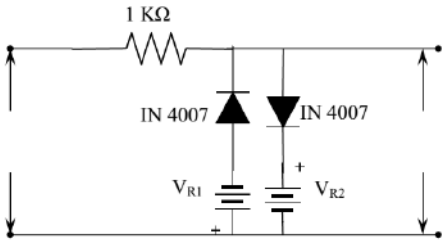
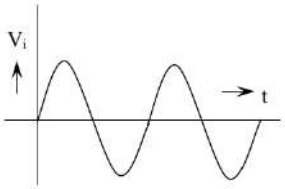


Figure:13.



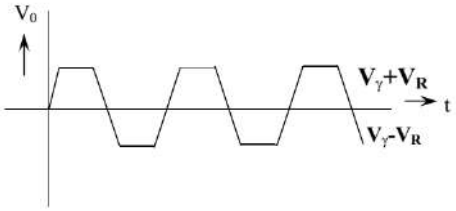


Figure:14(a). Input waveform

Figure14(b). Output waveform.

DESIGN:

1. For positive clipping at 'V' volts reference select V_R = V.
2. For negative clipping at 'V' volts reference select V_R= V.

3. For clipping at two independent levels at V1 & V2 reference voltages select $V_{R1}= V_1$, $V_{R2}= V_2$ and $V_{R2}> V_{R1}$

.

PROCEDURE:

1. Connect the circuit as shown in figure 1.
2. Connect the function generator at the input terminals and CRO at the output terminals of the circuit.
3. Apply a sine wave signal of frequency 1KHz at the input and observe the output waveforms of the circuits.
4. Repeat the procedure for figures 3, 5, 7, 9, 11 and 13.

RESULT:

$V\gamma=$

Clipping circuits for different reference voltages are studied.

EXPERIMENT NO: 11
EXPERIMENT NAME: To study of Clamping circuit.

Objective:
To get positive and negative clamping for sinusoidal and Square wave inputs.

Hardware Required:

S. No	Apparatus	Type	Range
01	Diode		
02	Resistance		1K ohm
03	Capacitor		10 mF
04	Power supply		0-30 V
05	CRO		
06	Function generator		
07	Breadboard and connecting wires		

Introduction:
Clamping Circuit "A clamping circuit is one that takes an input waveform and provides an output that is a faithful replica of its shape but has one edge tightly clamped to the zero voltage reference point".

There are various types of Clamping circuits, which are mentioned below:

1. Positive Clamping Circuit.
2. Negative Clamping Circuit.
3. Positive Clamping with the positive reference voltage.
4. Negative Clamping with the positive reference voltage.
5. Positive Clamping with the negative reference voltage.
6. Negative Clamping with the negative reference voltage.

Negative Clamping Circuit:

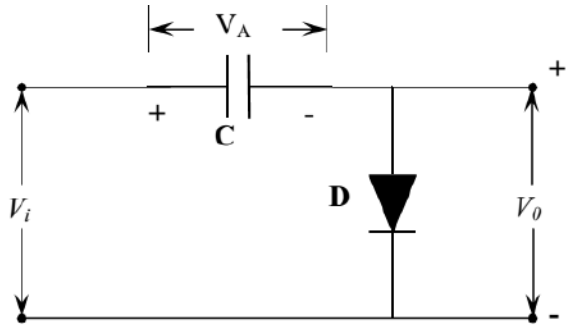


Figure:1

The input signal is sinusoidal which begins at t=0. The capacitor C is charged at t = 0. The waveform across the diode at various instants is studied. During the first quarter cycle, the

input signal rises from zero to the maximum value of V_m. The diode being ideal, no forward voltage may appear across it. During this first quarter cycle the capacitor voltage $V_A = V_i$. The voltage across C rises sinusoidally, and the capacitor is charged through the series combination of the signal source and the diode. Throughout this first quarter cycle the output V_0 has remained zero. At the end of this quarter cycle, there exists across the capacitor a voltage $V_A = V_m$.

After the first quarter cycle, the peak has been passed and the input signal begins to fall, the voltage V_A across the capacitor is no longer able to follow the input voltage. For in order to do so, it would be required that the capacitor-discharge, and because of the diode, such a discharge is not possible. The capacitor remains charged to the voltage $V_A = V_m$, and, after the first quarter cycle, the output is $V_0 = V_i - V_m$. During succeeding cycles, the positive excursion of the signal just barely reaches zero. The diode need never again conduct, and the positive extremity of the signal has been clamped to zero. The average value of the signal is $-V_m$.

Positive Clamping circuit:

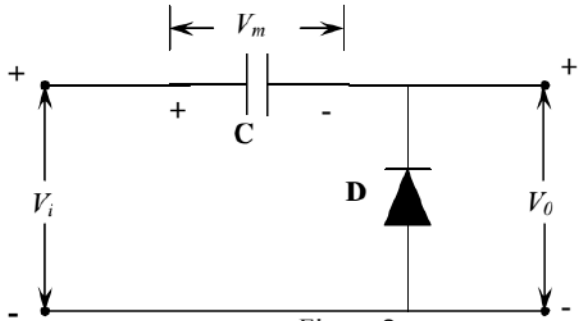


Figure:2

It is also called a negative peak clamper because this circuit clamps at the negative peaks of a signal.

Let the input signal be $V_i = V_m \sin\omega t$. When V_i goes negative, the diode gets forward-biased and conducts. The capacitor charges to voltage V_m, with polarity as shown. Under steady-state conditions, the positive clamping circuit is given as,

$$V_0 = V_i - (-V_m)$$

$$V_0 = V_i + V_m$$

During the negative half cycle of V_i, the diode conducts and C charges to $-V_m$ volts, i.e., the negative peak value. The capacitor cannot discharge since the diode cannot conduct in the reverse direction. Thus the capacitor acts as a battery of $-V_m$ volts and the output voltage is given by equation.1 above. It is seen in figure 2, that the negative peaks of the

input signal are clamped to zero level. The peak-to-peak amplitude of the output voltage $2V_m$, which is the same as that of the input signal.

Negative Clamping with Positive Reference Voltage:

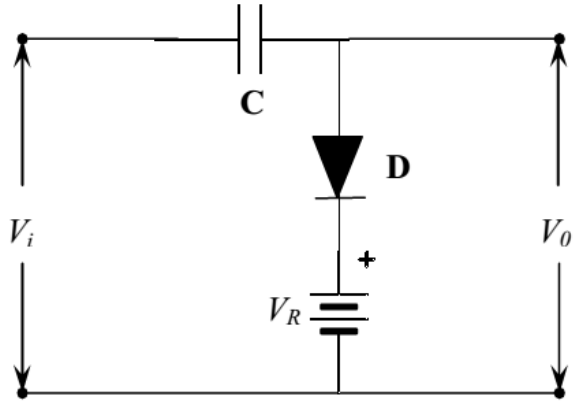


Figure:2

Since V_R is in series with the output of the negative clamping circuit, now the average value of the output becomes $(-V_m + V_R)$.

Similarly, the average of

i) Negative clamping with negative reference voltage is$(-V_m + V_R)$.

ii) Positive clamping is $+V_m$.

iii) Positive clamping with positive reference voltage is $V_m + V_R$.

iv) Positive clamping with negative reference voltage is $V_m - V_R$.

Negative Clamping:

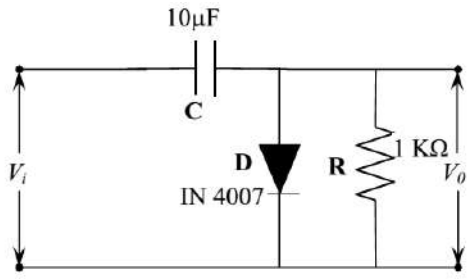


Figure:3

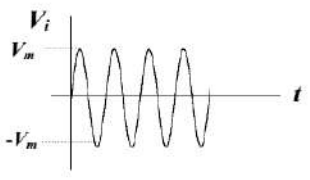


Figure:4 (a).Input waveform

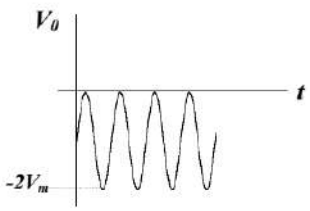


Figure:4 (b) Output waveform.

Negative Clamping with the positive reference voltage:

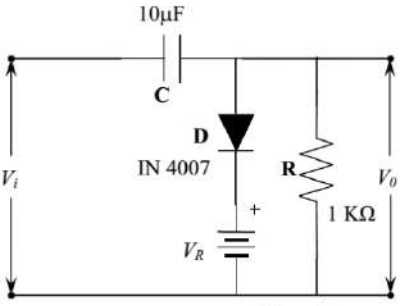


Figure:5

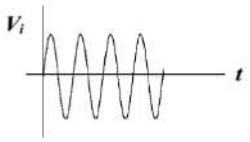


Figure:6 (a).Input waveform

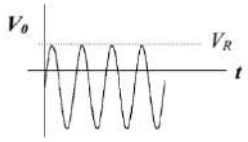


Figure:6 (b) Output waveform.

Negative Clamping with the negative reference voltage:

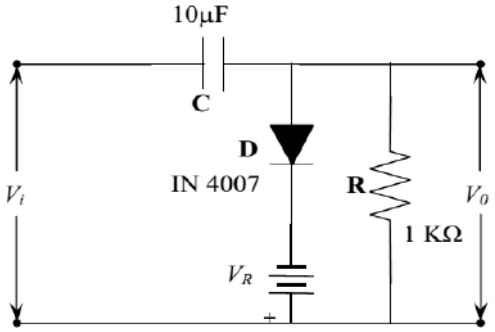


Figure:7

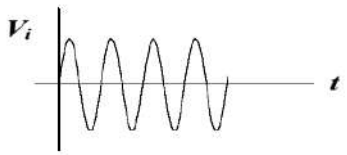


Figure:8 (a).Input waveform

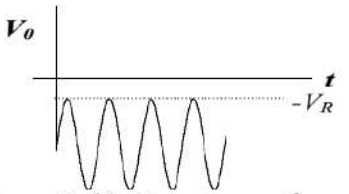


Figure:8 (b) Output waveform.

Positive Clamping:

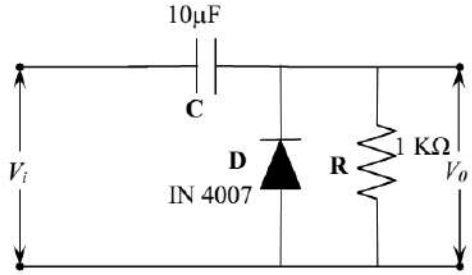


figure:9

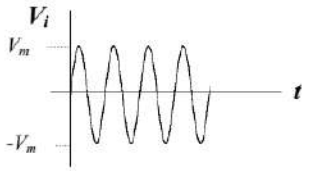


Figure:10 (a).Input waveform

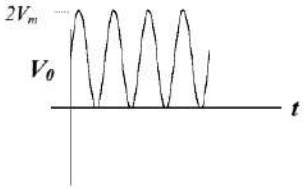


Figure:10 (b) Output waveform.

Positive Clamping with Negative Reference Voltage:

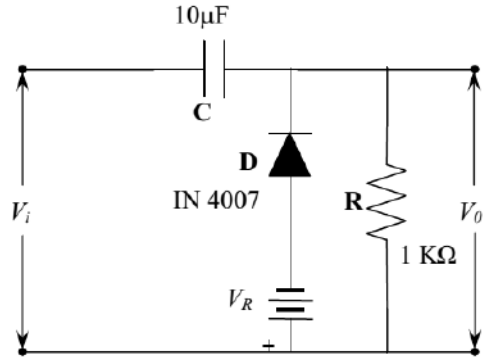


Figure: 11

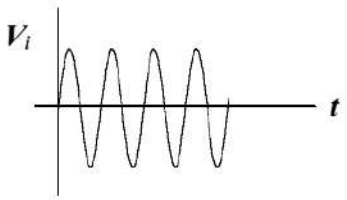


Figure:12 (a).Input waveform

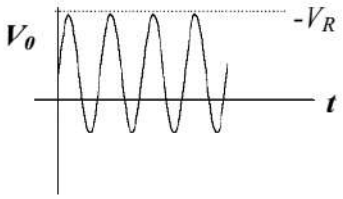


Figure:12 (b) Output waveform.

Positive Clamping with Positive reference Voltage:

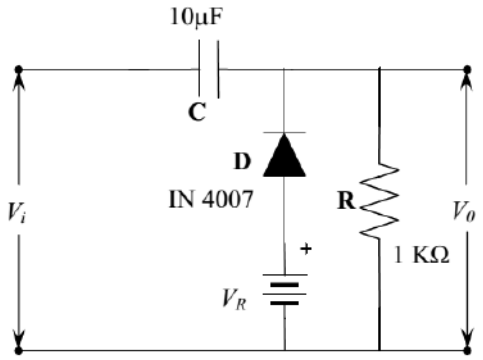


Figure:13

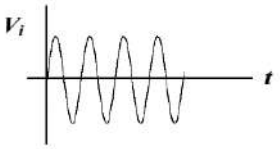


Figure:14 (a).Input waveform

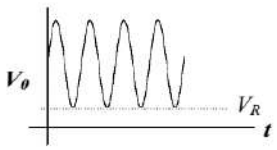


Figure:14 (b) Output waveform.

PROCEDURE:

1. Connect the circuit as shown in figure 3.
2. Connect the function generator at the input terminals and CRO at the output terminals of the circuit.
3. Apply a sine wave and square wave signal of frequency 1kHz at the input and observe the output waveforms of the circuits in CRO.
4. Repeat the above procedure for the different circuit diagrams as shown in figures 5, 7, 9, 11 and 13.

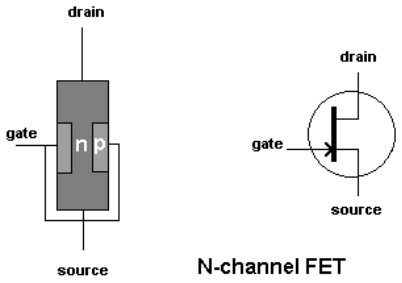
RESULT: The clamping voltages for positive and negative clamping circuits are noted.

EXPERIMENT NO: 12
EXPERIMENT NAME: To study of output characteristics of a FET.
Objective:
a) To study the Drain Characteristics of a FET.
b) To study the Transfer Characteristics of a FET.

Hardware Required:

S.No	Apparatus	Type	Range	Quantity
01	JFET	BFW11		1
02	Resistance		1K ohm	1
03	Regulated power supply		0-30 V	1
04	Ammeter	mC	(0-30)mA, (0-500)mA	1
05	Voltmeter	mC	(0 – 1)V, (0 – 30)	1
06	Breadboard and connecting wires			

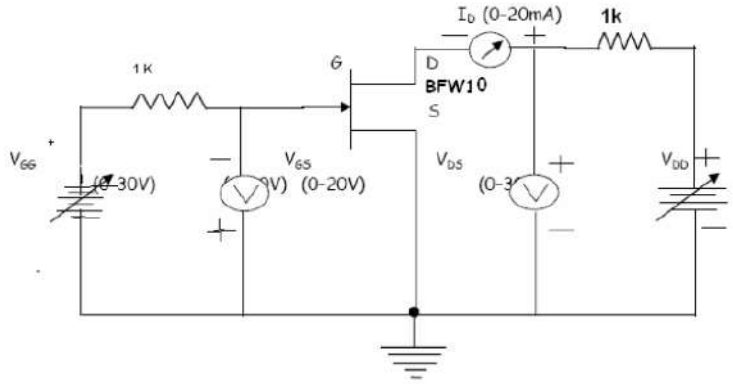
Introduction:



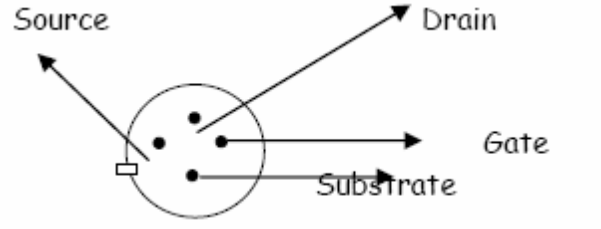
N-channel FET

The field effect transistor (FET) is made of a bar of N-type material called the SUBSTRATE with a P-type junction (the gate) diffused into it. With a positive voltage on the drain, with respect to the source, electron current flows from source to drain through the CHANNEL.
f the gate is made negative with respect to the source, an electrostatic field is created, which squeezes the channel and reduces the current. If the gate voltage is high enough the channel will be "pinched off" and the current will be zero. The FET 21 is voltage controlled, unlike the transistor which is current controlled. This device is sometimes called the junction FET or IGFET or JFET. If the FET is accidentally forward biased, gate current will flow and the FET will be destroyed. To avoid this, an extremely thin insulating layer of silicon oxide is placed between the gate and the channel. The device is then known as an insulated gate FET, IGFET or metal oxide semiconductor FET (MOSFET) Drain characteristics are obtained between the drain-to-source voltage (VDS) and drain current (ID) taking gate-to-source voltage (VGS) as the parameter. Transfer characteristics are obtained between the gate to source voltage (VGS) and Drain current (ID) taking drain to source voltage (VDS) as the parameter.

Circuit diagram:



Pin assignment of FET:



Precautions:

1. While experimenting, do not exceed the ratings of the FET. This may lead to damage to the FET.
2. Connect the voltmeter and Ammeter in the correct polarities as shown in the Circuit diagram.
3. Do not switch ON the power supply unless you have checked the Circuit connections as per the circuit diagram.
4. Make sure while selecting the Source, Drain and Gate terminals of the FET.

Experiment:

DRAIN CHARACTERISTICS:

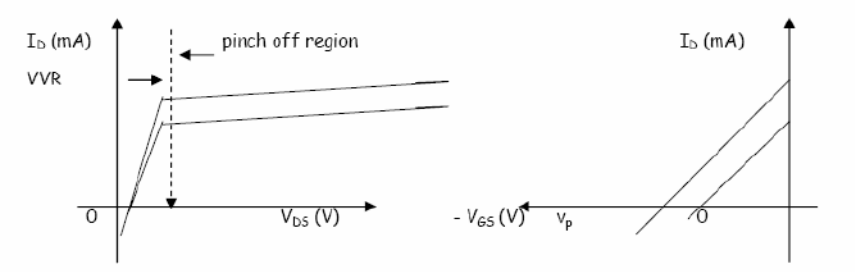
Determine the drain characteristics of FET by keeping V_{GS} = 0v. Plot its characteristics with respect to V_{DS} versus $I_{D.}$

TRANSFER CHARACTERISTICS:

Determine the transfer characteristics of FET for the constant value of V_{DS}. Plot its characteristics with respect to V_{GS} versus $I_{D.}$

Graph (Instructions):

1. Plot the drain characteristics by taking V_{DS} on X-axis and I_D on Y-axis at constant V_{GS}.
2. Plot the Transfer characteristics by taking V_{GS} on X-axis and I_D on Y-axis at constant V_{DS}.



DRAIN CHARACTERISTICS TRANSFER CHARACTERISTICS

Calculations from Graph:

Drain Resistance (rd) :

It is given by the ratio of a small change in the drain-to-source voltage (ΔV_{DS}) to the corresponding change in Drain current (ΔI_D) for a constant gate-to-source voltage (V_{GS}) when the JFET is operating in pinch-off or saturation region.

Trans-Conductance (gm) :

The ratio of a small change in drain current (ΔI_D) to the corresponding change in the gate to source voltage (ΔV_{GS}) for a constant V_{DS}. $gm = \Delta I_D / \Delta V_{GS}$ at constant V_{DS} (from transfer characteristics) The value of gm is expressed in mho's or siemens (s).

Amplification Factor (μ) :

It is given by the ratio of a small change in the drain-to-source voltage (ΔV_{DS}) to the corresponding change in the gate-to-source voltage (ΔV_{GS}) for a constant drain current.

$\mu = \Delta V_{DS} / \Delta V_{GS}$.

$\mu = (\Delta V_{DS} / \Delta I_D) \text{ X } (\Delta I_D / \Delta V_{GS})$

$\mu = rd \text{ X } gm$.

Inference:

1. As the gate-to-source voltage (VGS) is increased above zero, pinch-off voltage is increased at a smaller value of drain current as compared to that when VGS =0 V
2. The value of drain to source voltage (VDS) is decreased as compared to that when VGS= 0V.

Result:

1. Drain Resistance (rd) = …….
2. Transconductance (gm) = …….
3. Amplification factor (μ) = ……

Conclusion:

EXPERIMENT NO: 13
EXPERIMENT NAME: To study of output characteristics of a JFET.

Objective:
1. To study Drain Characteristics and Transfer Characteristics of a Junction Field Effect Transistor (JFET).

2. To measure drain resistance, trans-conductance and amplification factor.

Hardware Required:

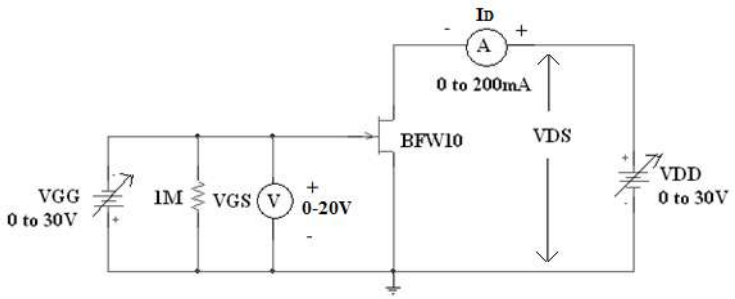
S.No	Apparatus	Type	Range	Quantity
01	JFET	BFW11		1
02	Resistance		1M ohm	1
03	Regulated power supply		0-30 V	1
04	Digital Ammeter	mC	(0-200)mA	1
05	Digital Voltmeter	mC	(0-20)V	2
06	Breadboard and connecting wires			

Introduction:
A JFET is called a Junction Field effect transistor. It is a unipolar device because the flow of current through it is due to one type of carrier i.e., the majority carriers whereas a BJT is a Bi-Polar device, It has 3 terminals Gate, Source and Drain. A JFET can be used in any of the three configurations viz, Common Source, Common Gate and Common Drain. The input gate to the source junction should always be operated in reverse bias, hence input resistance Ri = ∞, IG ≈ 0. Pinch-off voltage VP is defined as the gate to source reverse bias voltage at which the output drain current becomes zero.
In CS configuration Gate is used as the input node and the Drain as the output node. A JFET in CS configuration is used widely as an amplifier. A JFET amplifier is preferred over a BJT amplifier when the demand is for smaller gain, high input resistance and low output resistance. Any FET operation is governed by the following equation.
The drain current equation and trans-conductance are given as

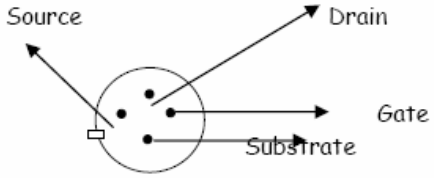
$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)$, $g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2}{V_p}\sqrt{I_D I_{DSS}}$

Where $I_{DSS}$is called as Drain to Source Saturation current & V_P is called the Pinch off voltage.

Circuit diagram:



Pin assignment of FET:



Procedure:

Transfer Characteristics:

1) Connect the circuit as shown. All the knobs of the power supply must be at the minimum position before the supply is switched on.
2) Adjust the output voltage V_{DS} to 4V by adjusting the supply V_{DD}.
3) Vary the supply voltage V_{GG} so that the voltage V_{GS} varies in steps of -0.25 V from 0 V onwards. In each step note the drain current I_D. This should be continued till I_D becomes zero.
4) Repeat above step for V_{DS} = 8V.
5) Plot a graph between the input voltage V_{GS} and output current I_D for output voltage V_{DS} in the second quadrant. This curve is called the transfer characteristics.

Drain Characteristics:

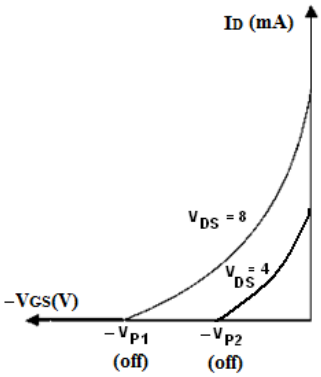
1) Connect the circuit as shown in the figure. Adjust all the knobs of the power supply to their
minimum positions before switching the supply on.
2) Adjust the input voltage V_{GS} to 0 V by adjusting the supply V_{GG}.
3) Vary the supply voltage V_{DD} so that V_{DS} varies in steps of 0.5 V from 0 to 4 V and then in steps of 1 V from 4 to 10 V. In each step note the value of drain current I_D.
4) Adjust V_{GS} to -1 and -2 V and repeat step-3 for each value of V_{GS}.
5) Plot a graph between V_{DS} and I_D for different values of V_{GS}. These curves are called drain
characteristics.
6) Mark the various regions in the drain characteristics graph and calculate the drain resistance.

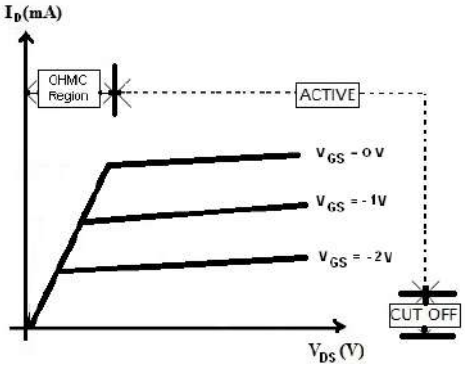
Observations:

Transfer Characteristics			
V_{DS} = 4V		V_{DS} = 6V	
V_{GS}(V)	I_D(mA)	V_{GS}(V)	I_D(mA)

Drain Characteristics					
V_{GS} = 0V		V_{GS} = -1V		V_{GS} = -2V	
V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)

Graph:





Transfer Characteristics **Drain Characteristics**

1. Plot the drain characteristics by taking V_{DS} on X-axis and I_D on Y-axis at a constant V_{GS}.
2. Plot the transfer characteristics by taking V_{GS} on X-axis and taking I_D on Y-axis at constant V_{DS}.

Calculations from Graph:

1. **Drain Resistance (r_d):** It is given by the relation of a small change in drain to source voltage (ΔV_{DS}) to the corresponding change in Drain Current (ΔI_D) for a constant gate to source voltage (ΔV_{GS}) when the JFET is operating in pinch-off region.
2. **Trans Conductance (gm):** Ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant V_{DS}.
gm= $\frac{\Delta \square_{\square}}{\Delta \square_{\square\square}}$ at constant V_{DS} (from transfer characteristics).
The value of **gm** is expressed in mho's (ʊ) or Siemens (**s**).
3. **Amplification factor (μ):** It is given by the ratio of small change in drain to source voltage (V_{DS}) to the corresponding change in gate to source voltage (V_{GS}) for a constant drain current (I_D).

Precautions:

1. While performing the experiment do not exceed the ratings of the FET. This may lead todamage to the FET.
2. Connect the voltmeter and ammeter in the correct polarities as shown in the circuitdiagram.
3. Do not switch ON the power supply unless you have checked the circuit connections asper the circuit diagram.
4. Make sure while selecting the Source, Drain and Gate terminals of the transistor.

Results:

1. Drain Characteristics and Transfer Characteristics of a Field Effect (FET) Transistor are studied.
2. Drain resistance, trans-conductance and amplification factor are measured.