CSE_2323

Sequential Logic
Flip Flop

Digital Logic Design

Course code: CSE-2323
Credit Hour: 3

Md. Mujibur Rahman Maruf

Adjunct Lecturer,

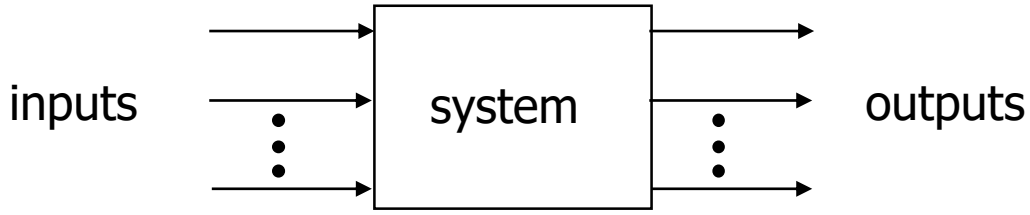
Dept. of CSE, IIUC

Mujiburmaruf.cuet17@gmail.com

International Islamic University Chittagong(IIUC)

Combinational vs. sequential systems

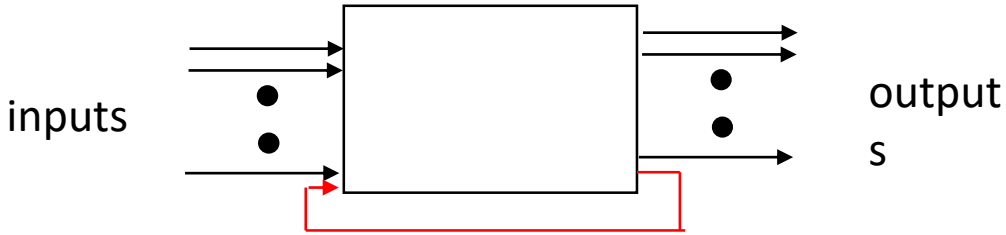
A simple model of a digital system is a unit with inputs and outputs:



Combinational systems are "memory-less" The outputs depend only on the present inputs

Sequential systems have memory

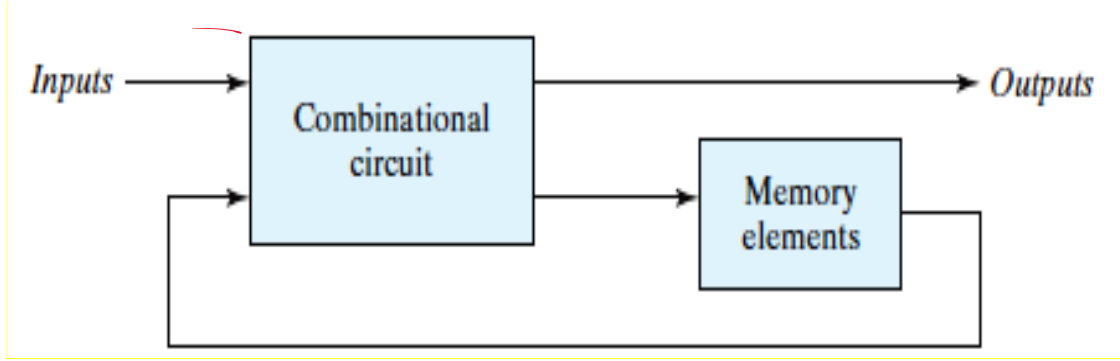
The output values depend on the input values and previous input values



Sequential Logic

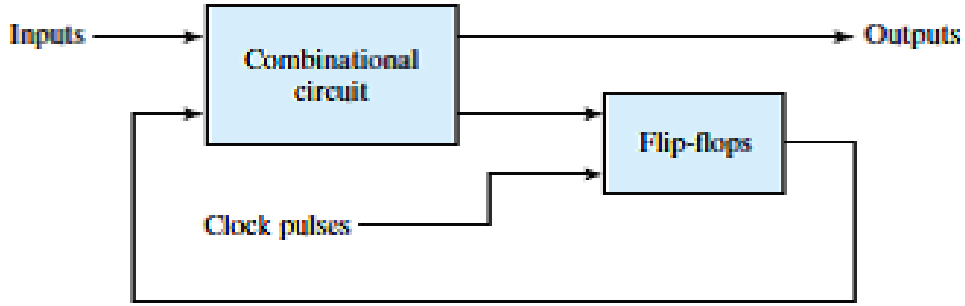
There are **TWO** main types of sequential circuits:

- **Asynchronous sequential circuit:** Sequential circuits that don't use a clock signal to determine the timing of their operations

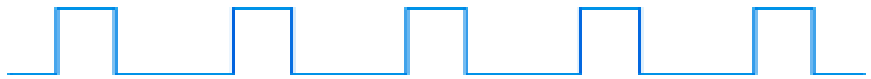


Synchronous sequential circuit:

outputs and internal states are changed synchronously following a clock signal.

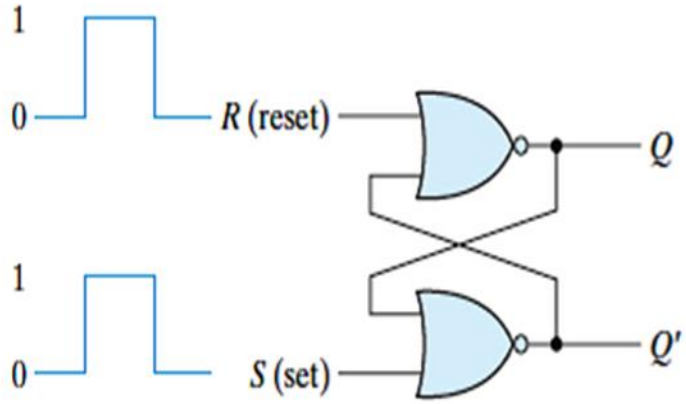


(a) Block diagram



(b) Timing diagram of clock pulses

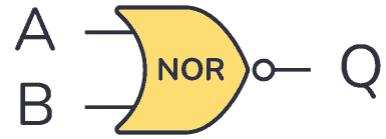
S R Latch: NOR Gate



(a) Logic diagram

S	R	Q	Q′	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

(b) Function table



A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

NOR gate truth table

Case:1

- When S=0 and R=1, the latch is reset into a state where Q=0 and Q'=1

When R= S=0 the circuit remains in its current state (Q=1 and Q'=0)

Case:2

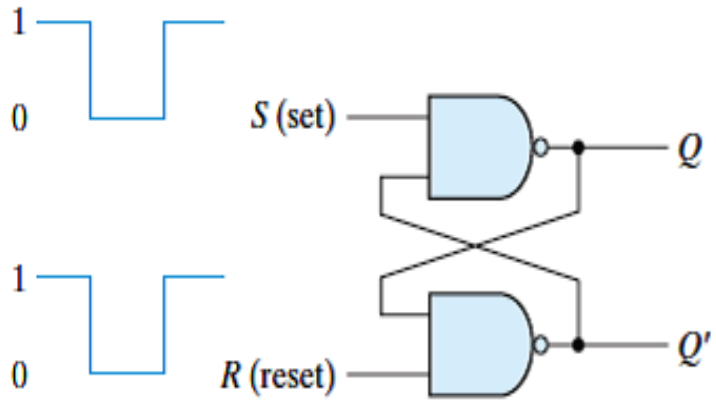
- When S=1 and R=0, the latch is set into a state where Q=1 and Q'=0

When R= S=0 the circuit remains in its current state (Q=1 and Q'=0)

Case 3:

Where S=1 and R=1, Q_2=Q=0 (there are actually problems with this state as we will see)

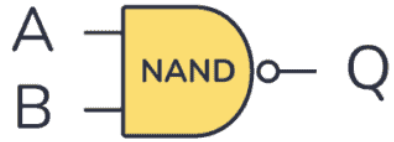
S R Latch: NAND Gate



(a) Logic diagram

S	R	Q	Q′	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

(b) Function table



A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

NOR gate truth table

Case:1

• When S=0 and R=1, the latch is reset into a state where Q=1 and Q'=0

When R= S=1 the circuit remains in its current state (Q=1 and Q'=0)

Case:2

• When S=1 and R=0, the latch is set into a state where Q=0 and Q'=1

When R= S=0 the circuit remains in its current state (Q=0 and Q'=1)

Case 3:

Where S=0 and R=0, Q_2=Q=1 (there are actually problems with this state as we will see)

Flip flop

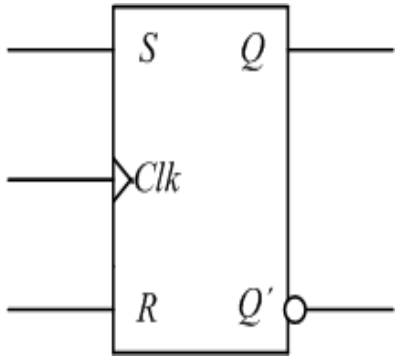
A device that stores either a 0 or 1.

Flip-flop :is a clocked device, in which only the clock edge determines when a new bit is entered.

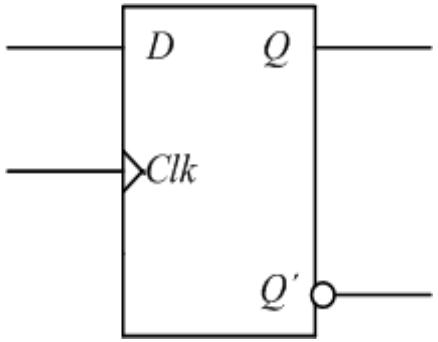
Stored value can be changed only at certain times determined by a clock input.

New value depend on the current state and it's control inputs

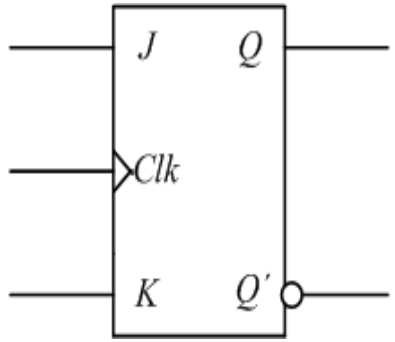
A digital circuit that contains flip-flops is called a sequential circuit



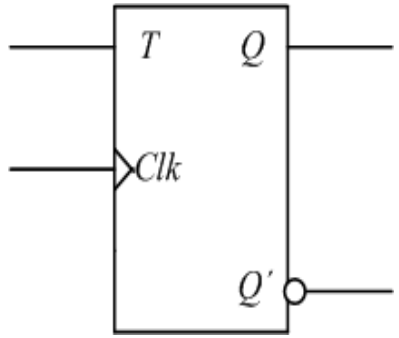
S-R flip-flops



D flip-flop



J-K flip-flops

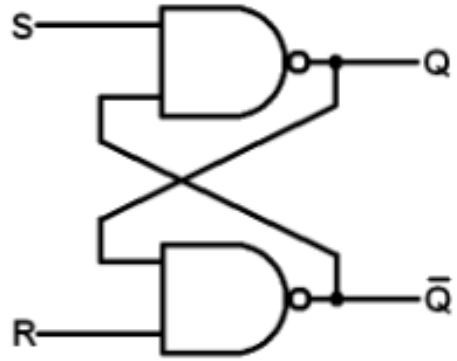


T flip-flop

Difference between Latch and Flip Flop

- The circuit an change accidentally.
- Not suitable for use
- Add control input so that we can decide

When S R input will be change



S R Latch

Level triggered

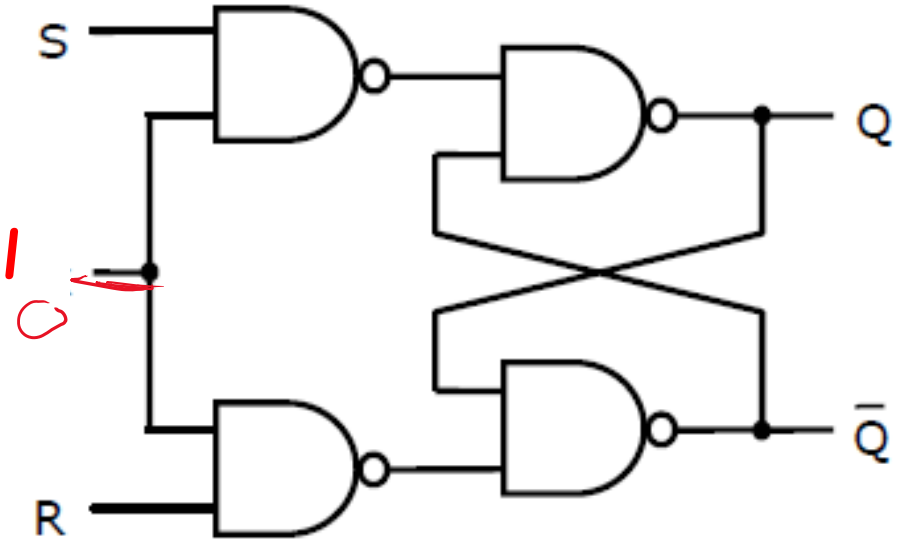
Enable

Clk

Edge triggered

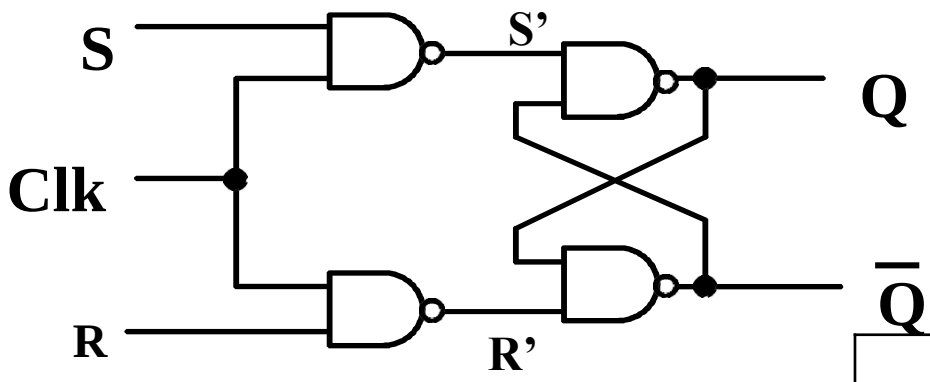
Flip flop

Control input



S - R Flip Flop

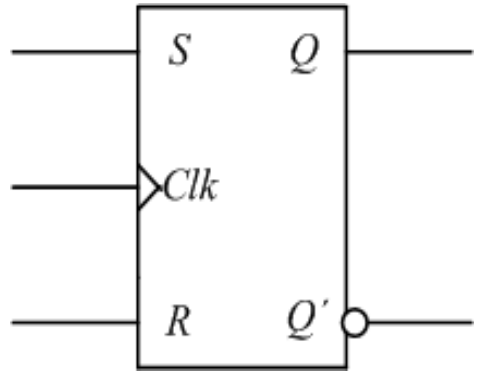
- Adding two NAND gates to the basic S - R NAND latch gives the clocked S'-R' Latch



S'	R'	Q	Q'
0	0	Not used	
0	1	1	0
1	0	0	1
1	1	Memory	

Truth Table			
clk	S	R	Q_{t+1}
0	x	x	Q_t (Memory)
1	0	0	Q_t (Memory)
1	0	1	0
1	1	0	1
1	1	1	Invalid

characteristics Table				
Q(t)	**S**	**R**	**Q(t+1)**	**Comment**
0	**0**	**0**	**0**	**No change**
0	**0**	**1**	**0**	**Clear Q**
0	**1**	**0**	**1**	**Set Q**
0	**1**	**1**	**X**	**Indeterminate**
1	**0**	**0**	**1**	**No change**
1	**0**	**1**	**0**	**Clear Q**
1	**1**	**0**	**1**	**Set Q**
1	**1**	**1**	**x**	**Indeterminate**



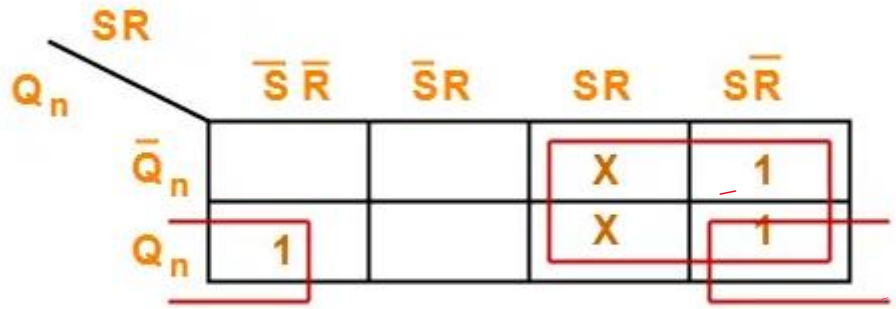
S - R Flip Flop

characteristics Table				
Q(t)	S	R	Q(t+1)	Comment
0	0	0	0	No change
0	0	1	0	Clear Q
0	1	0	1	Set Q
0	1	1	X	Indeterminate
1	0	0	1	No change
1	0	1	0	Clear Q
1	1	0	1	Set Q
1	1	1	x	Indeterminate

Excitation Table

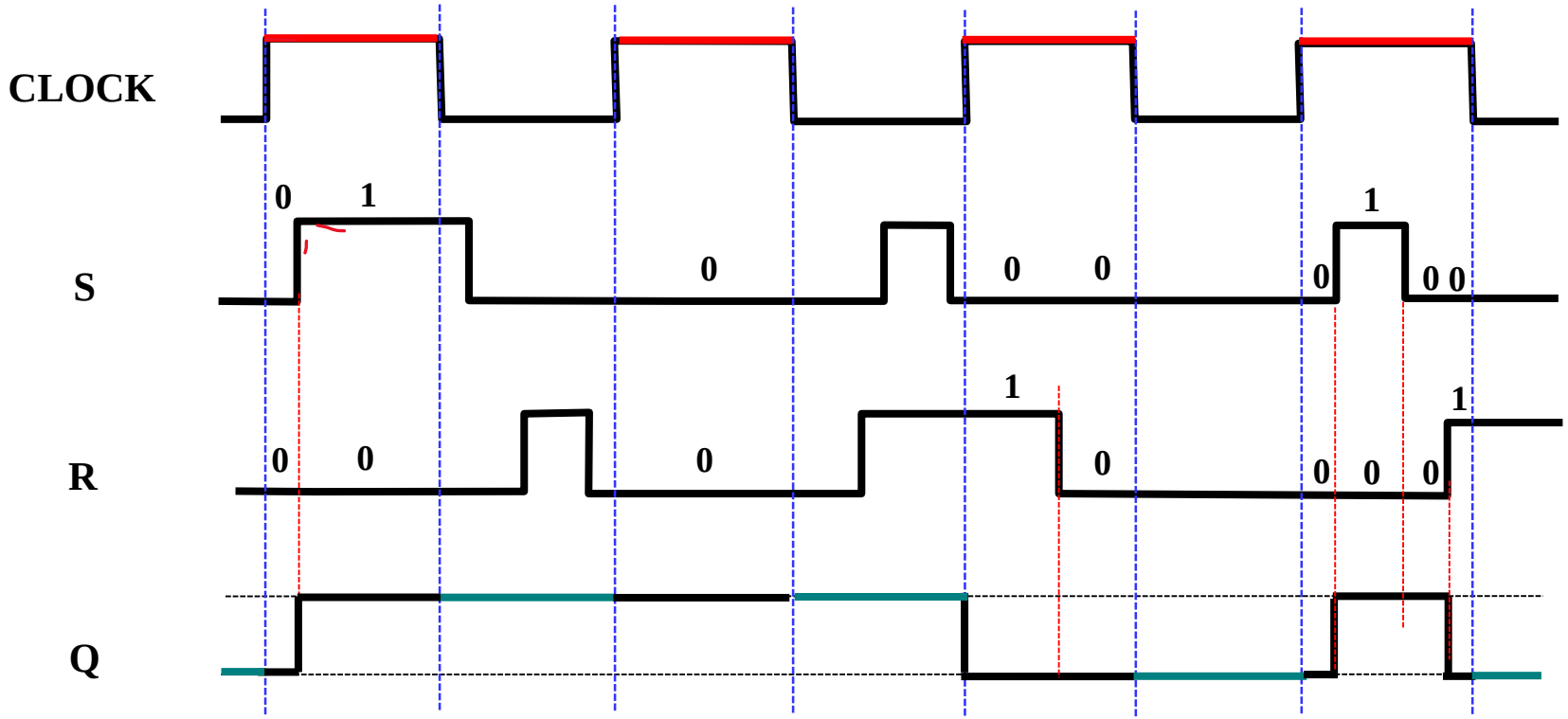
SR Flip-flop			
Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

$Q_{t+1} = S + Q_t R'$



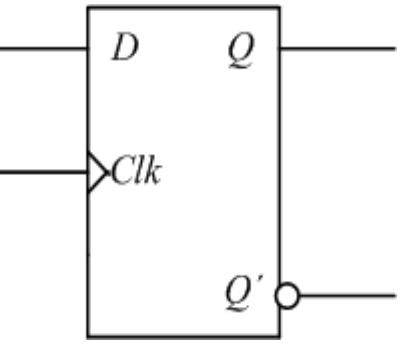
K Map

Example- S - R Flip Flop

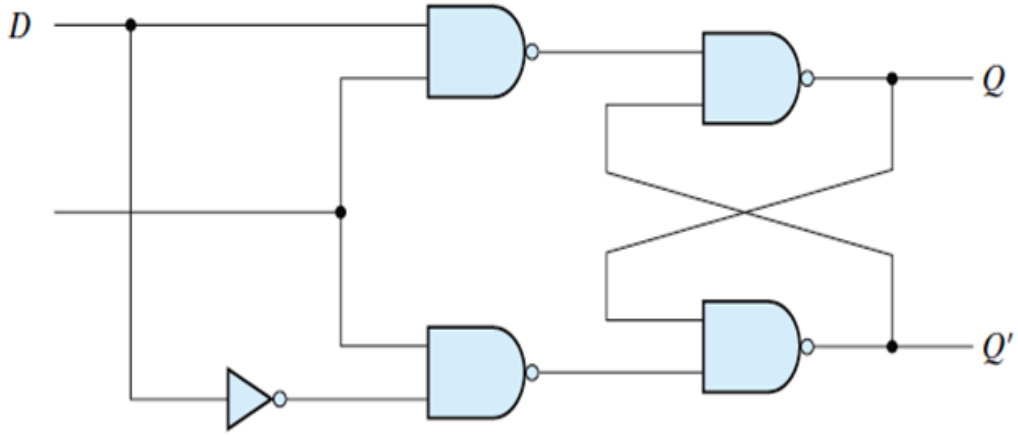


D Flip Flop

The D stands for "data"; this flip-flop stores the value that is on the data line.



Clk



(a) Logic diagram

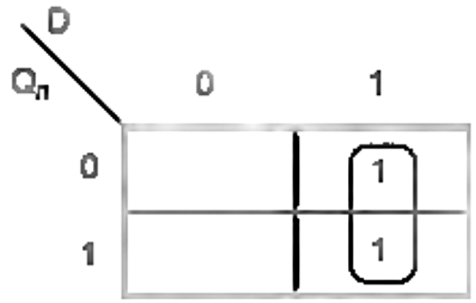
Clk	D	Next state of Q
0	X	No change
1	0	Q = 0; reset state
1	1	Q = 1; set state

(b) Function table

D flip-flop

characteristics Table

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1



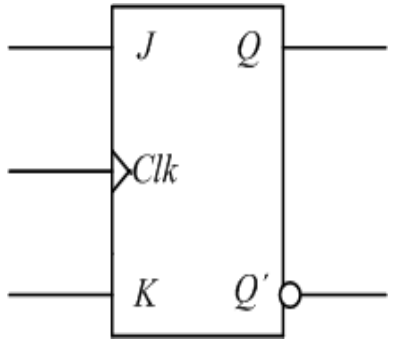
Excitation Table

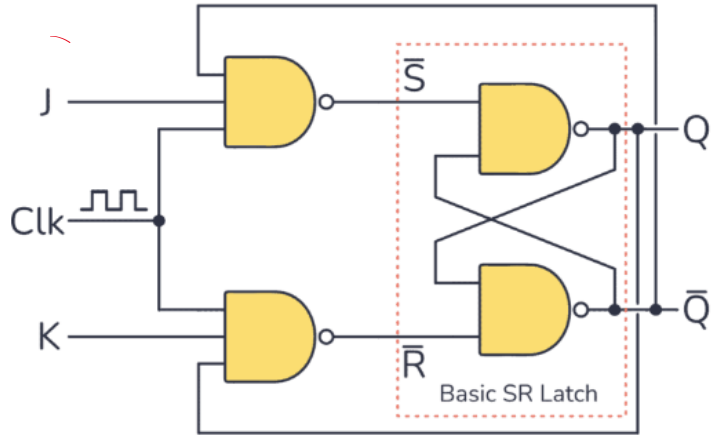
D Flip-flop		
Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	0
1	1	1

J K Flip Flop

J and K inputs of the JK flip-flop can be used to set, reset, or toggle the output, like this:

- J=1 and K=0 sets the output to 1
- J=0 and K=1 reset the output to 0
- J=1 and K=1 toggle the output





JK Flip-Flop basic circuit

J-K flip-flops

JK Flip Flop Truth Table

Truth Table			
clk	J	K	Q_{t+1}
0	x	x	Q_t (Memory)
1	0	0	Q_t (Memory)
1	0	1	0
1	1	0	1
1	1	1	Q'

- For CLK=1(Flip Flop is Enabled)
- For J=0, K=0 ➡ $\bar{S}$=1, $\bar{R}$=1 ➡ Latch Retains Values.
- For J=0, K=1
  - if $Q = 1, \bar{Q} = 0$ ➡ $\bar{S}$=1, $\bar{R}$=0 ➡ Latch Resets.
  - If $Q = 0, \bar{Q} = 1$ ➡ $\bar{S}$=1, $\bar{R}$=1 ➡ Latch Retains Reset Mode.
- For J=1, K=0
  - If $Q = 1, \bar{Q} = 0$ ➡ $\bar{S}$=1, $\bar{R}$=1 ➡ Latch Retains Set Mode.
  - If$Q = 0, \bar{Q} = 1$ ➡ $\bar{S}$=0, $\bar{R}$=1 ➡ Latch Sets.
- For J=1, K=1
  - If $Q = 1, \bar{Q} = 0$ ➡ $\bar{S}$=1, $\bar{R}$=0 ➡ Set Mode Toggles.
  - If $Q = 0, \bar{Q} = 1$ ➡ $\bar{S}$=0, $\bar{R}$=1 ➡ Reset Mode Toggles.

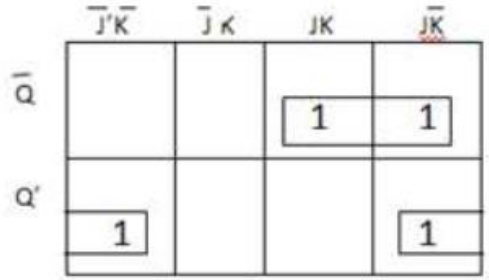
J K Flip Flop

characteristics Table				
Q(t)	J	K	Q(t+1)	Comment
0	0	0	0	No change
0	0	1	0	Clear Q
0	1	0	1	Set Q
0	1	1	1	toggle
1	0	0	1	No change
1	0	1	0	Clear Q
1	1	0	1	Set Q
1	1	1	0	toggle

Excitation Table

JK flip-flop			
Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

For $Q_{(t+1)}$

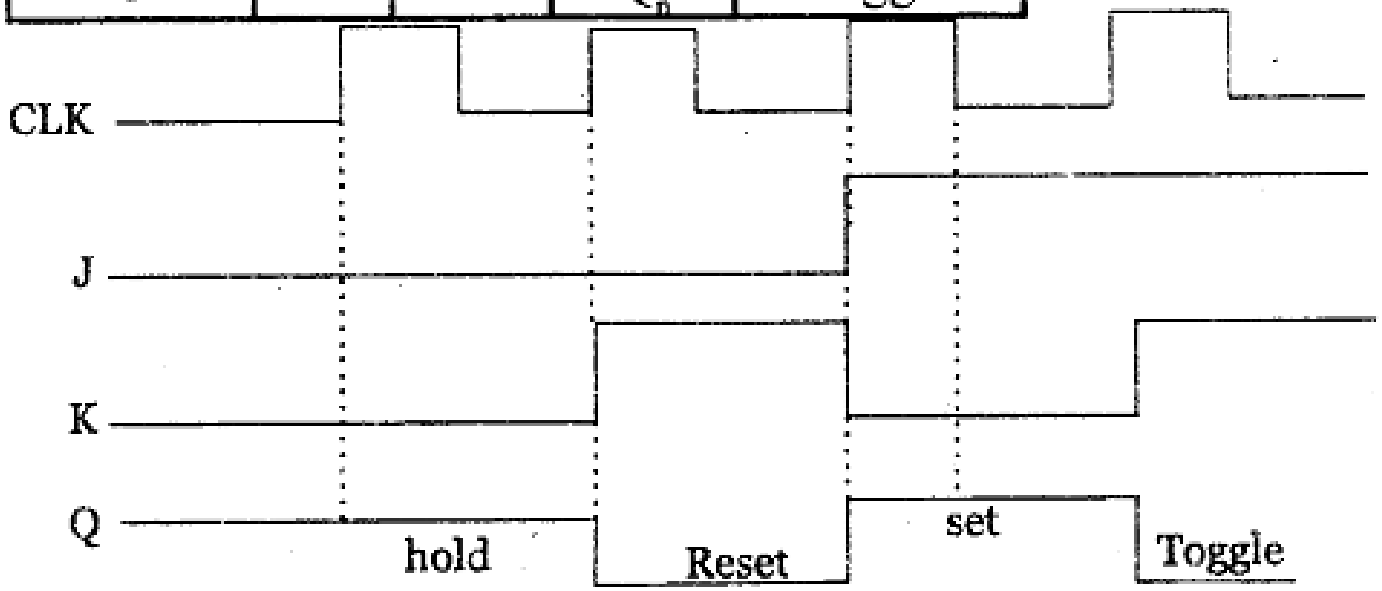


$Q_{t+1} = J\bar{Q} + \bar{K}Q$

J K Flip Flop

Truth table.

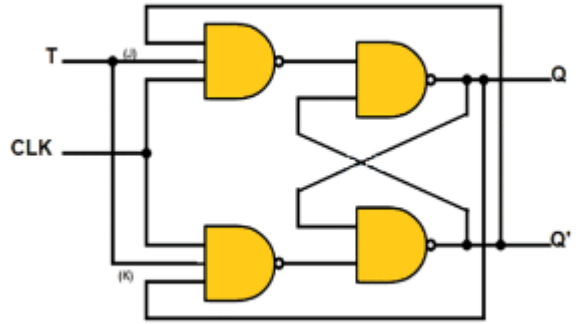
CLOCK	J	K	Q_{n+1}	Action
0	X	X	Q_n	No change
1	0	0	Q_n	No change
1	1	0	1	Reset
1	1	1	Q_n	Toggle



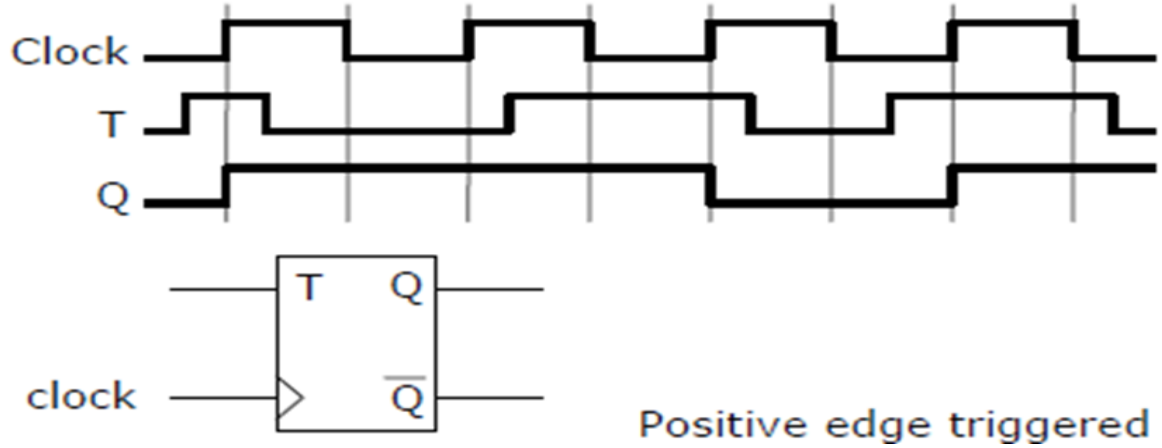
T Flip Flop

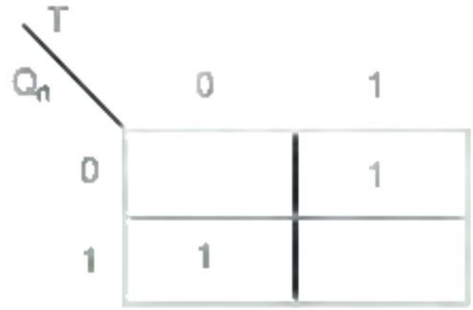
The name T derives from the behavior of the circuit, which 'toggles' its state when T=1

- This feature makes the T flip-flop a useful element when constructing counter circuits



Input	Present State	Next State
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

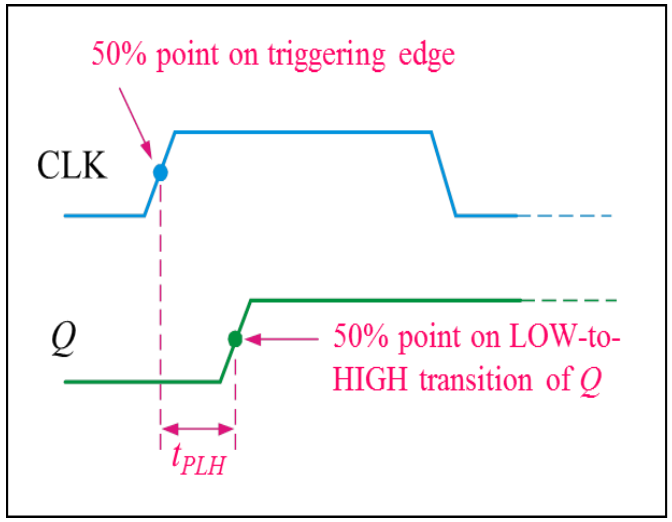


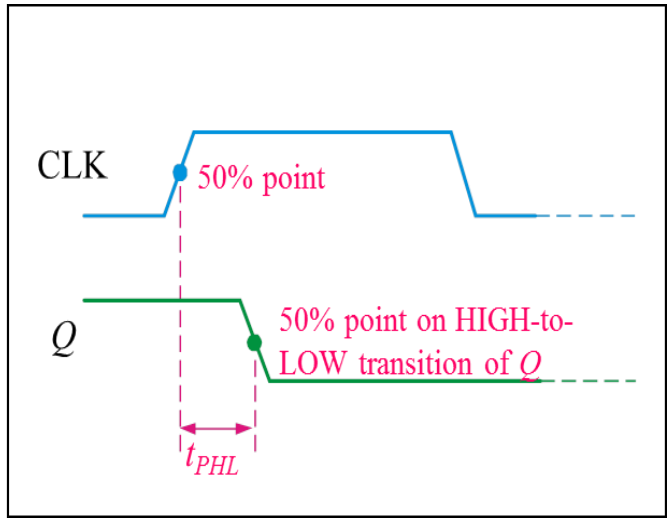


$$Q_{n+1} = T.\overline{Q_n} + \overline{T}.Q_n$$

Propagation Delay

Propagation delay time is specified for the rising and falling outputs. It is measured between the 50% level of the clock to the 50% level of the output transition

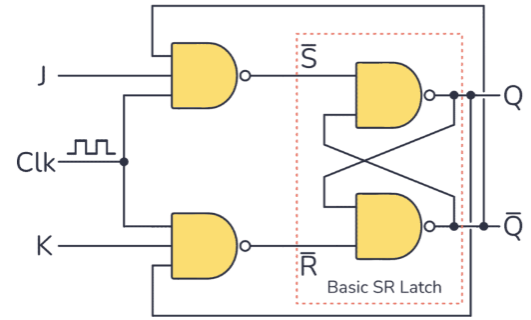




Race around condition

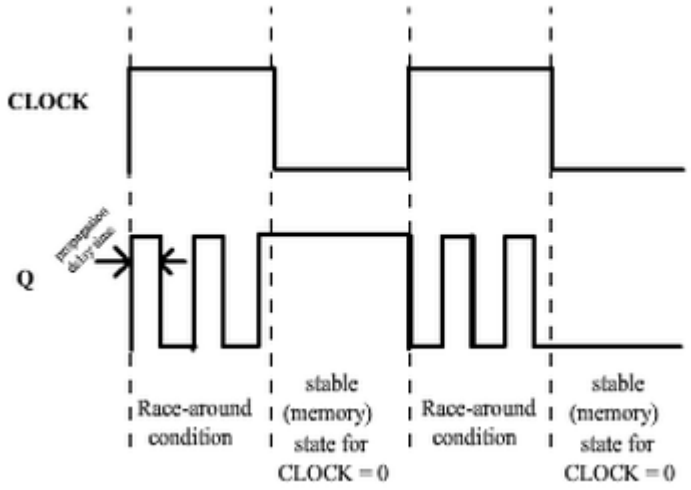
Truth table of JK flip flop was formed with the assumptions that inputs do not change during clock pulse.

- But this condition is not true because of feedback connections.
- Due to the feedback connection there is uncontrolled toggling at the output.



JK Flip-Flop basic circuit

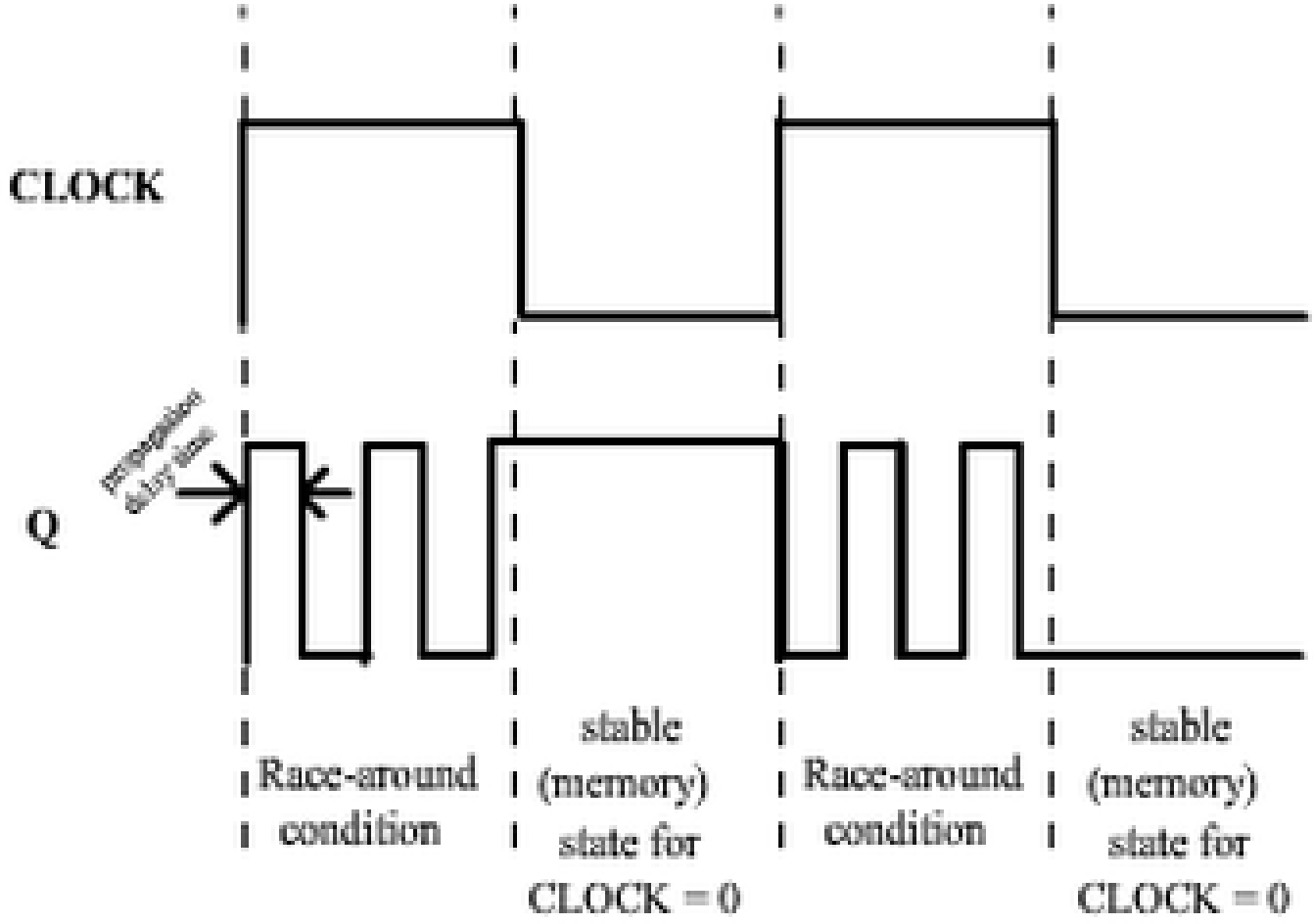
Race Around Condition In JK Flip-flop - For J-K flip-flop, if J=K=1, and if clk=1 for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop.

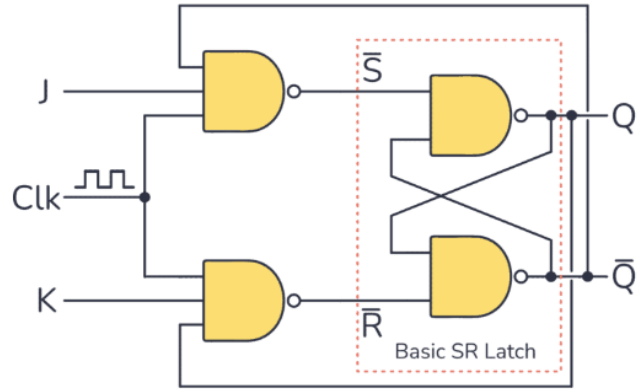


Solutions of Racing

1. Clock Pulse Duration≤ Propagation Delay of NAND gates (not feasible)
2. Edge triggered Flip flop
3. Master-Slave JK Flip flop

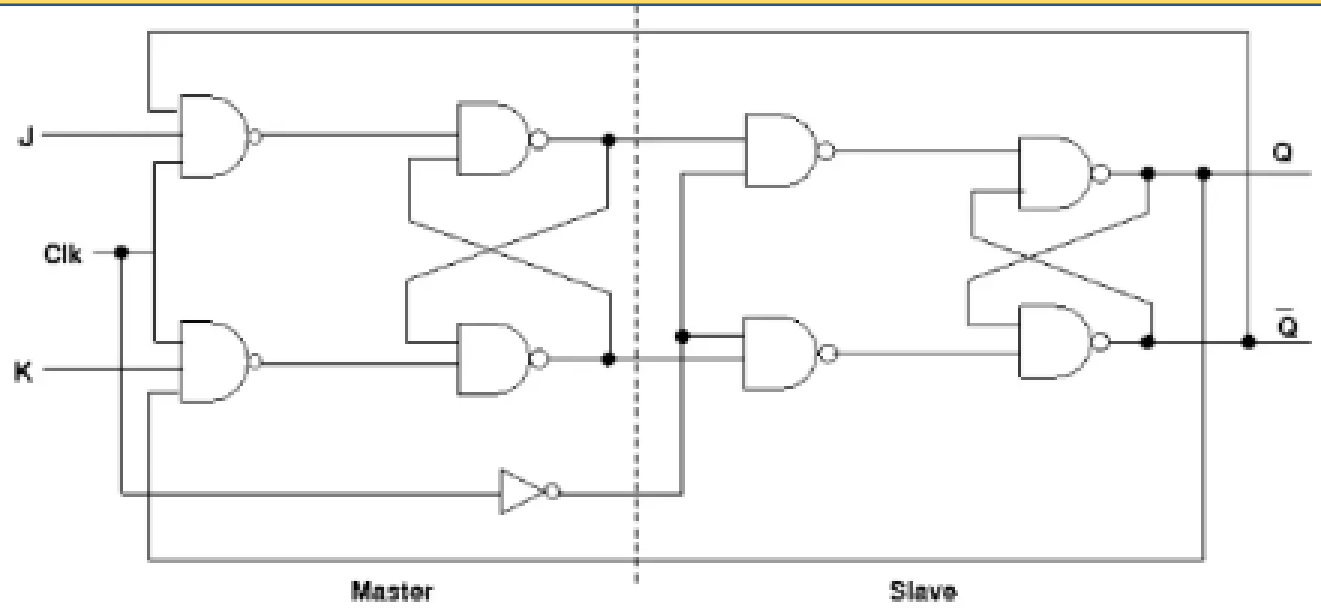
Race around condition





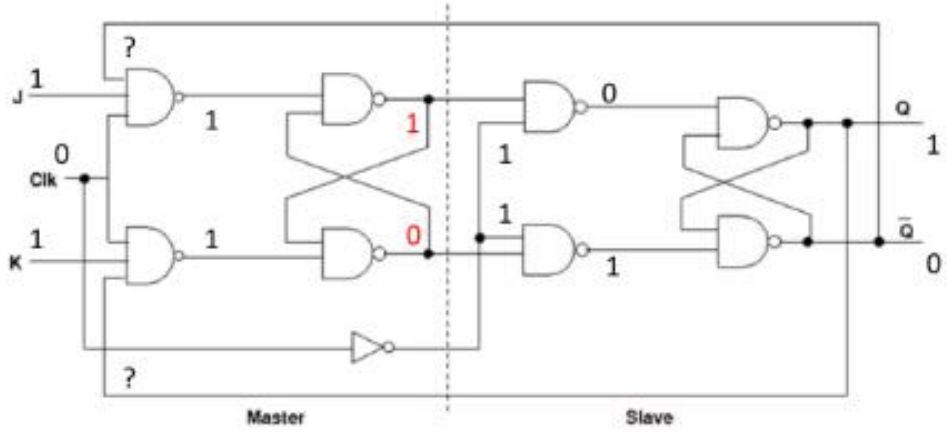
JK Flip-Flop basic circuit

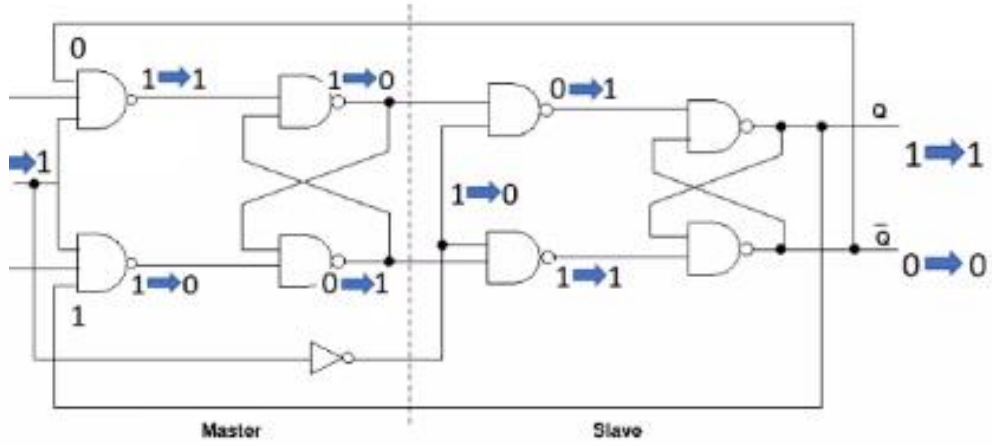
Master Slave J K Flip Flop



Master Slave JK flip flop has two cascaded SR flip flops with complemented clocks. Outputs of second SR flip flop fed back to the steering gates of first SR flip flop.

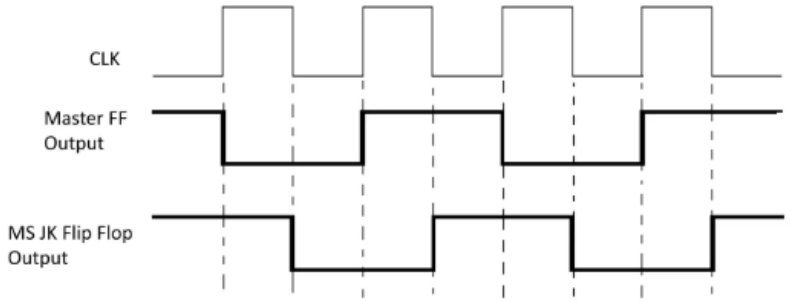
Master Slave J K Flip Flop





- Assumed the output of this Master flip flop latch is 1 and 0.
- When Clock input is '0' output of the inverter is '1', slave latch is then enabled and its output 'Q' is equal to the master latch output.

Timing Diagram of MS JK flip flop

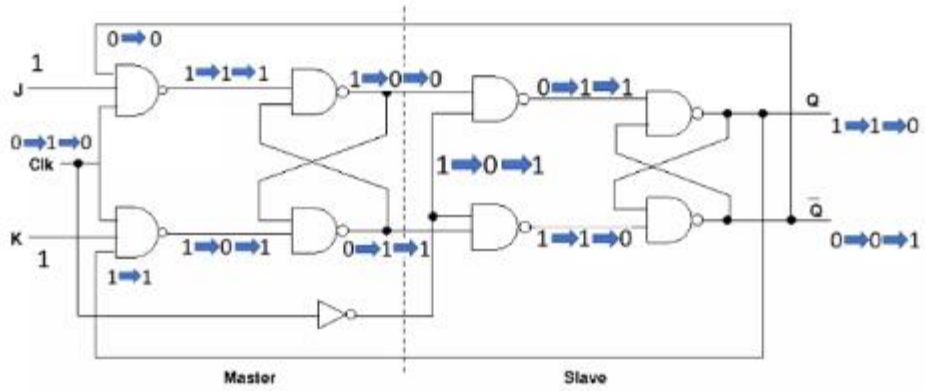


When clock is '1', master is enabled whose values, input value of master's SR latch controls the value stored in master.

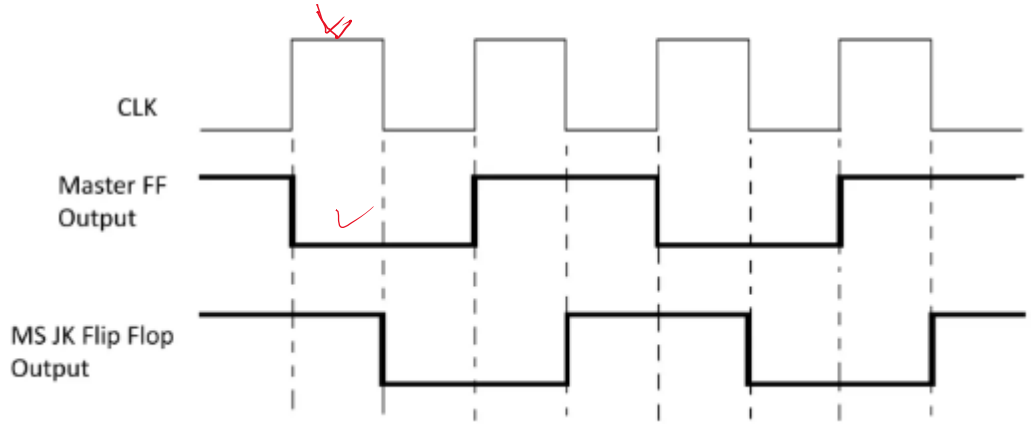
- Any change in external inputs (J,K) can change the output of master but can not change the slave output because it is getting inverted clock that is '0'.

Master Slave J K Flip Flop

Master Slave JK Flip Flop Operation



Timing Diagram of MS JK flip flop



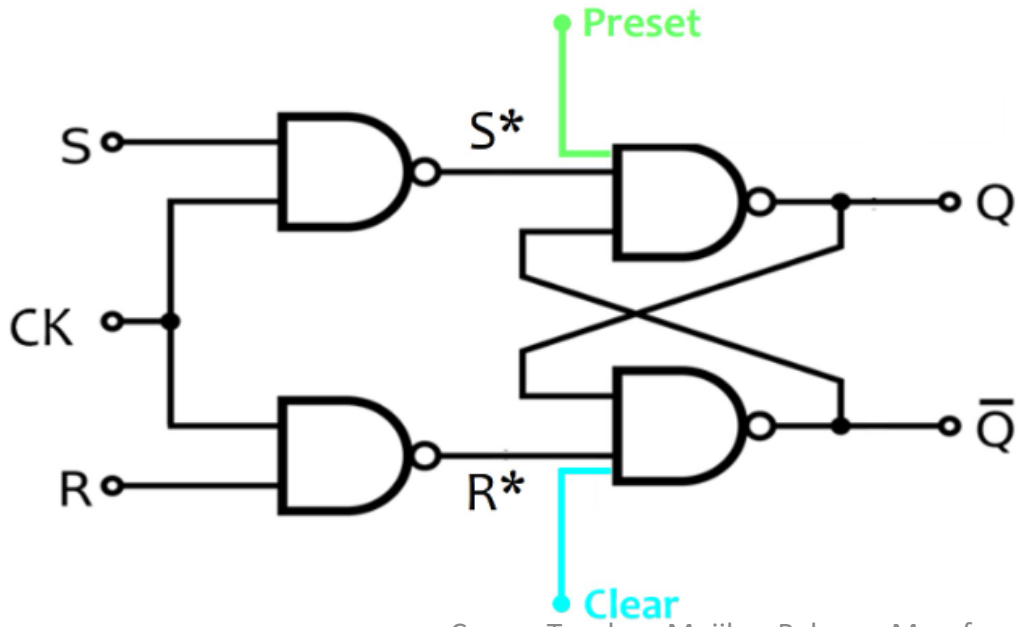
- When the clock input returns to zero, the master is disabled, at the same time slave is enabled and the current value of master is transferred to the output of flipflop

Preset and clear

Asynchronous inputs on a flip-flop have control over the outputs (Q and not-Q) regardless of clock input status.

These inputs are called the preset (PRE) and clear (CLR).

The preset input drives the flip-flop to a set state while the clear input drives it to a reset state.



Flip Flop conversion

Steps To Convert from One Flip Flop to Other :

1. Identify available and required flip flop.
2. Make excitation table for available flip flop and characteristics table for required flip flop.
3. Write Boolean expression for available flip flop.
4. Draw the circuit.

S R to JK flip flop conversion

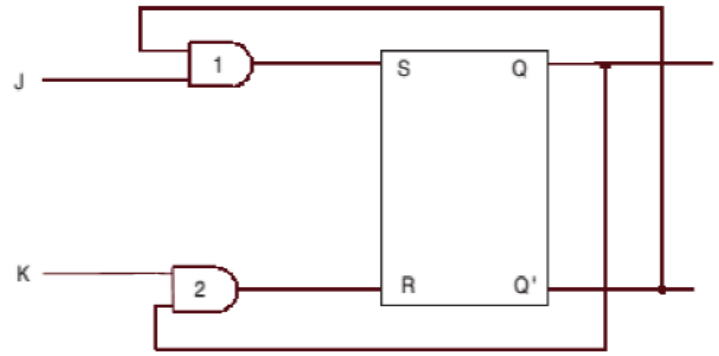
Step:1 S R is available and J K is required flip flop.

characteristics Table					
Q(t)	J	K	Q(t+1)	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

Step:2

Excitation Table

SR Flip-flop			
Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0



Step:3

For S

Q \ JK	J'K' (00)	J'K (01)	JK (11)	JK' (10)
Q' 0	0	0	1	1
Q 1	X	0	0	X

For R

Q \ JK	J'K' (00)	J'K (01)	JK (11)	JK' (10)
Q' 0	X	X	0	0
Q 1	0	1	1	0

Step:4

S = JQ'
& R = KQ.

D to SR flip flop conversion

Step:1 D is available and S R is required flip flop.

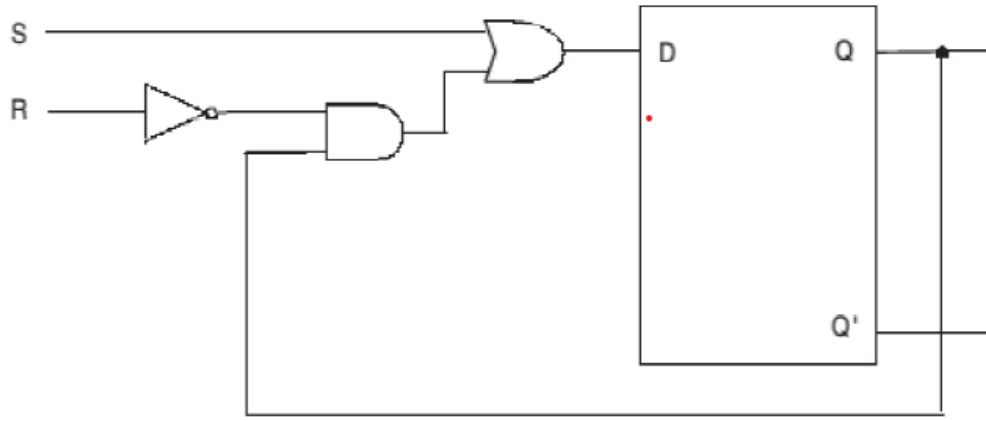
Step:2

characteristics Table

Q(t)	S	R	Q(t+1)	D
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	X	X
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	X	X

Excitation Table

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1



Step:4

Step:3

For D

Q	SR = 00 (S'R')	SR = 01 (S'R)	SR = 11 (SR)	SR = 10 (SR')
Q' 0	0	0	X	1
Q 1	1	0	x	1

D=S+R'Q.

D to T flip flop conversion

Step:1 D is available and T is required flip flop.

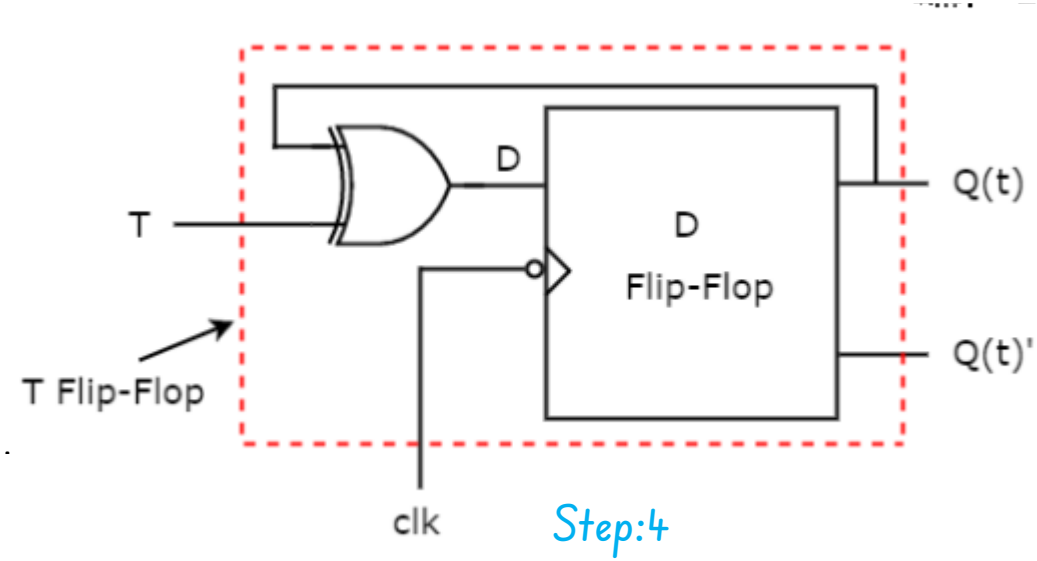
Step:2

characteristics Table

Q_t	T	Q_{t+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Excitation Table

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1



Step:4

Step:3

For D

Q \ T	T' = 0	T = 1
Q' = 0	0	1
Q = 1	1	0

D=TQ'+T'Q.

Assignment

Other flip flop conversion

1. .J K flip flop to T flip flop
2. .J K flip flop to D flip flop
3. D flip flop to T flip flop
4. D flip flop to JK flip flop
5. T flip flop to J K flip flop

Last Date of submission:
30-4-24

Project And report

Implement Boolean function using Breadboard, switches, fundamental Logic gate's IC(And,Or, Not)

1.(A'+B)C' (Group-1)

2.A'B+C' (Group-2)

3.(AB)'+C' (Group-3)

4.(A+B)'C' (Group-4)

5.(A'+B)'C (Group-5)

Project And report

Report must contain:

1.Truth Table

2.Proteus Design

A.Design Boolean function using the fundamental gates

B.Design Boolean function using Only Nand gate

C.Design Boolean function using only NOR gate

3.Handwriting Design

Implement Function using:

A. Multiplexer

B. Demultiplexer

4.Discussion