

## Counter:

- ✓ 1. Basics of counter
- ✓ 2. Asynchronous up counter
- ✓ 3. Asynchronous down counter
- 4. Modulo counter by Asynchronous counter
- ✓ 5. BCD counter
- ✓ 6. 2 bits synchronous counter using JK flip flop
- ✓ 7. 3 bits synchronous counter using T flip flop
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- ✓ 9. Ring counter
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- ✓ 11. Arbitrary sequence counter ✓
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## Counter

Counter - Counter is used for counting pulses and also we can use it as frequency divider.

Two types of counter: 1. Up counter 2. Down counter

Up counter: It will count  $[0, 1, 2, \dots, N]$  [Incremental]

Down counter: It will count  $[N, N-1, \dots, 2, 1, 0]$  [Decremental]

Classification of counters: ① Synchronous counter

② Asynchronous counter

Synchronous counter: Memory elements are having same clock pulse.

Asynchronous counter: Memory elements are having different clock pulse.

For  $n$  bits counter, Maximum counter =  $2^n$

⇒ For 3 bits counter: It will count (000 to 111)

	$Q_2$	$Q_1$	$Q_0$	
	0	0	0	
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
	1	0	1	
	1	1	0	
	1	1	1	

↑      ↓

Up counter      Down counter

$2^3 = 8$  counts

- Each clock output representing state of counter
- State will change with respect to frequency clock and it will change in sequence.

$Q_2 \quad \underline{0000} \boxed{1} \boxed{1} \boxed{1} \boxed{1} \quad f/8$

$Q_1 \quad \underline{00} \boxed{1} \boxed{1} \boxed{00} \boxed{1} \boxed{1} \quad f/4$

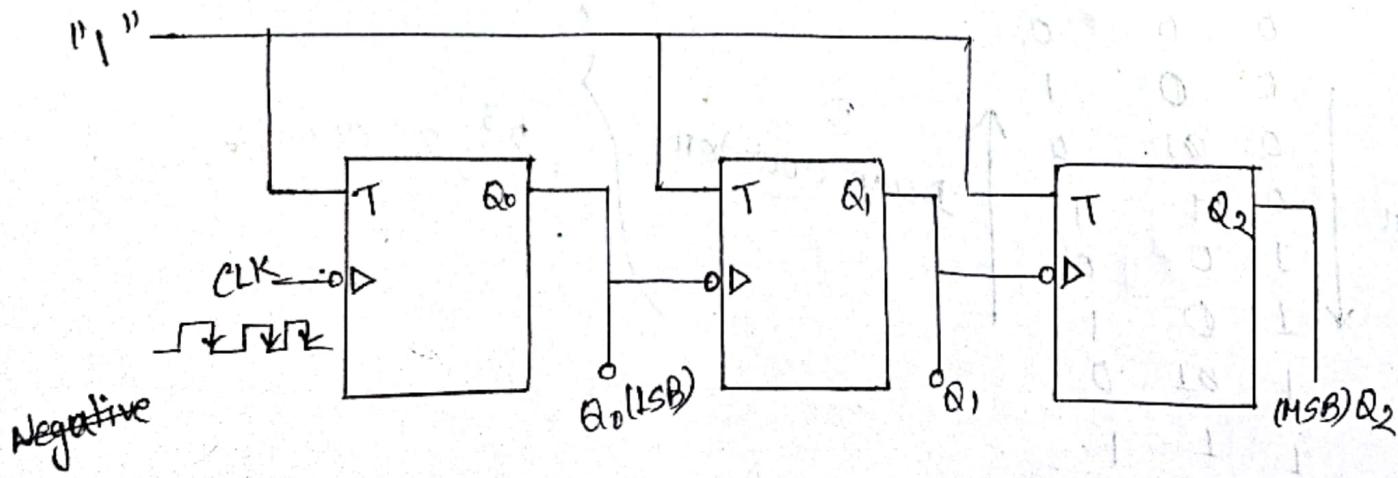
$Q_0 \quad \underline{0} \boxed{1} \boxed{0} \boxed{1} \boxed{0} \boxed{1} \quad f/2$

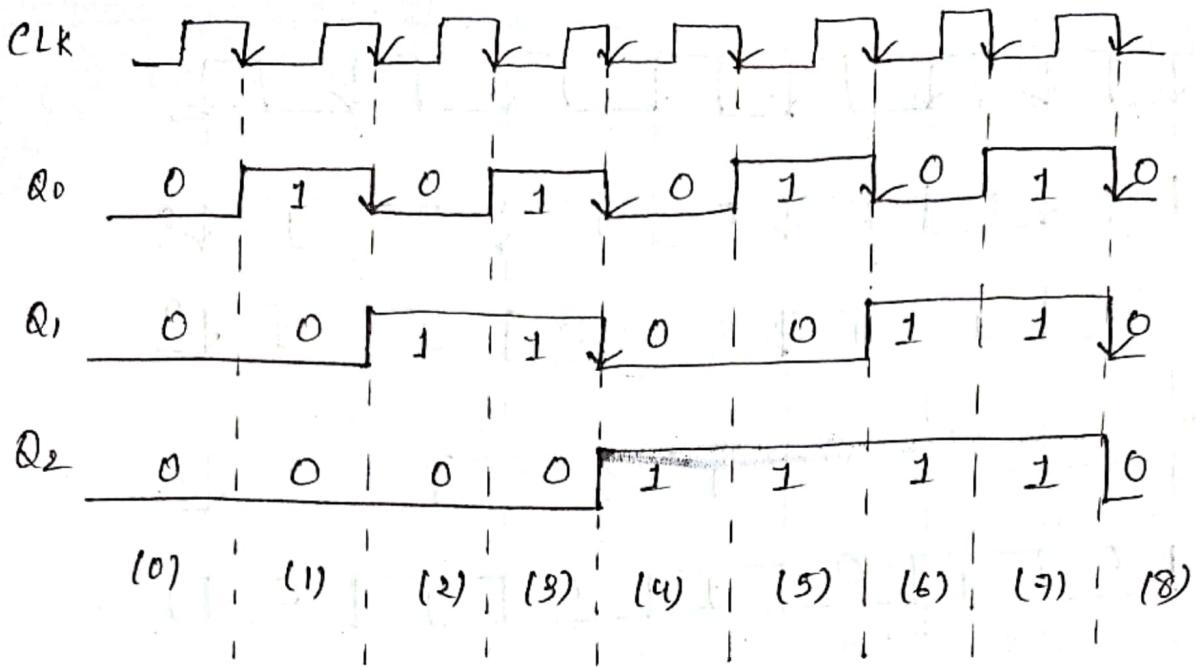
CLK  f

(state respect to clock)

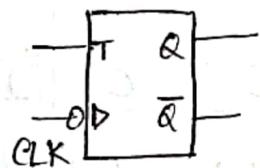
### Asynchronous (Ripple) up counter:

- In asynchronous counter, we don't provide same clock signal to all memory elements.
- In T FF output will Toggle, when  $T=1$  and clock Trigger.
- negative edge trigger clock, Toggling will happen in negative edge.

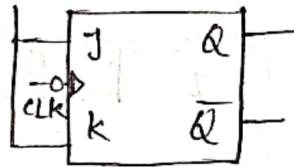




(1)



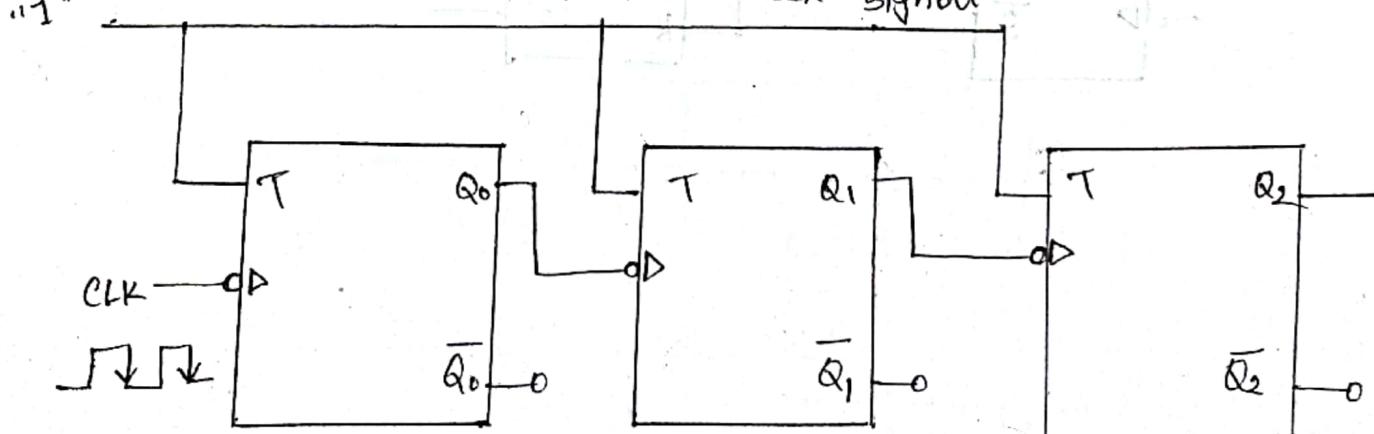
$\Rightarrow$

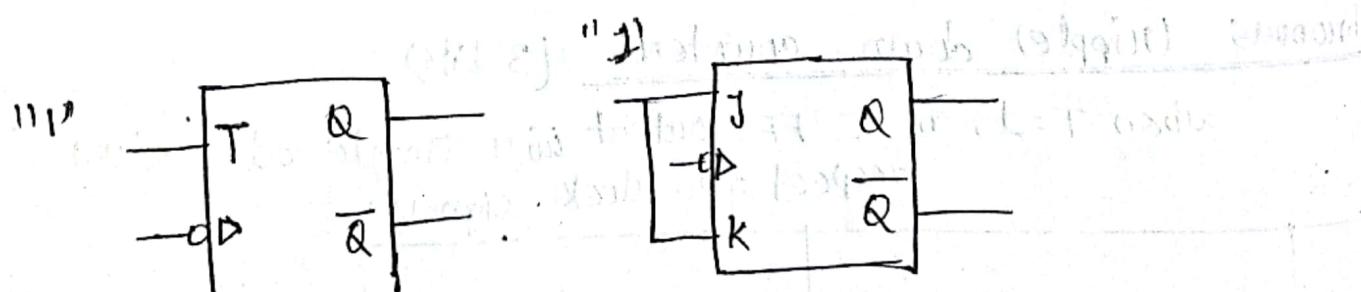
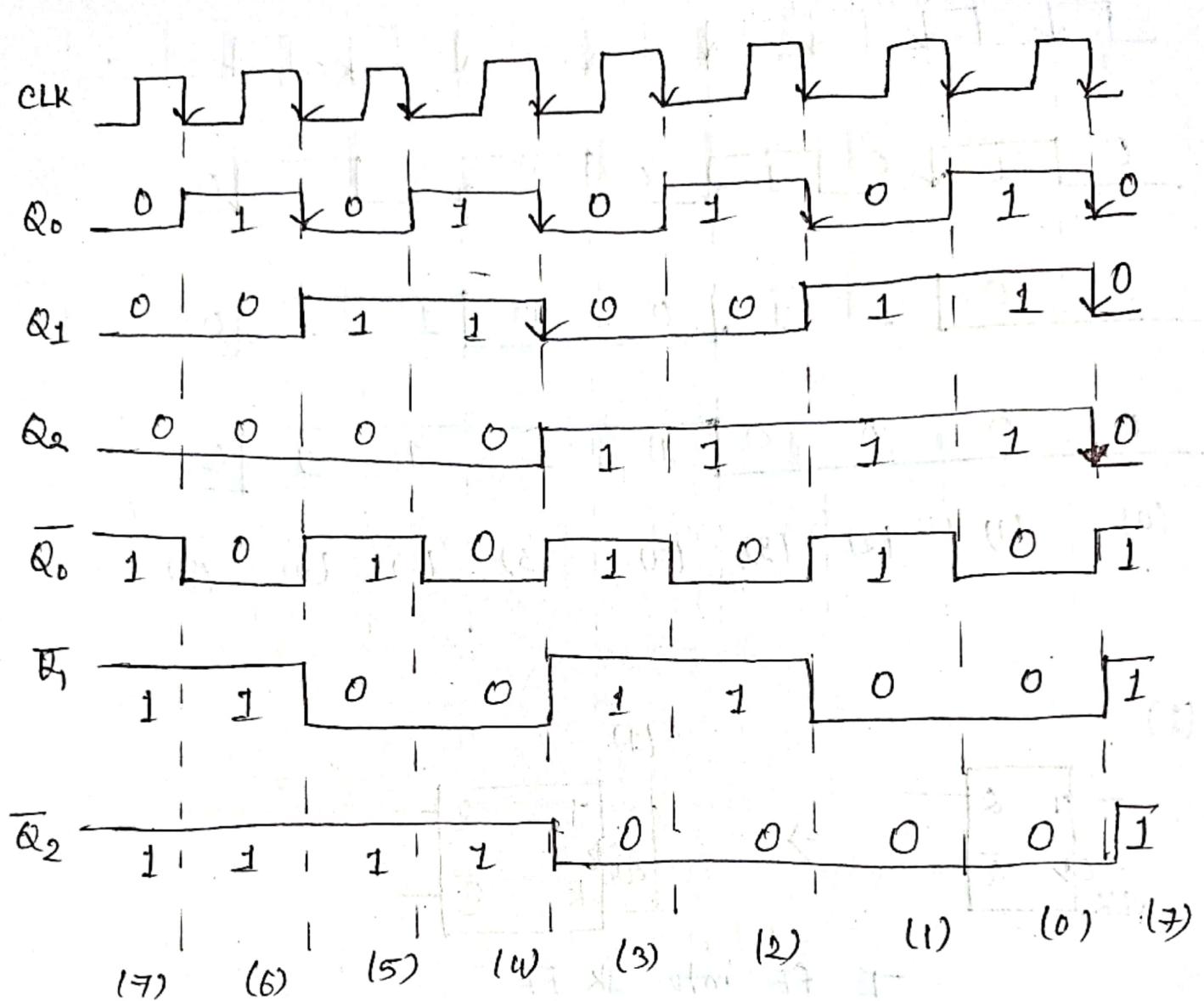


T FF into JK FF

### Asynchronous (ripple) down counter: (3 bits)

when  $T=1$ , in T FF output will toggle at output with respect to clock signal.





## Modulo 8 counter by Asynchronous counter:

By 2 bits counter, at max we can have mod 4 counter.

By 3 bits counter, at max we can have mod 8 counter.

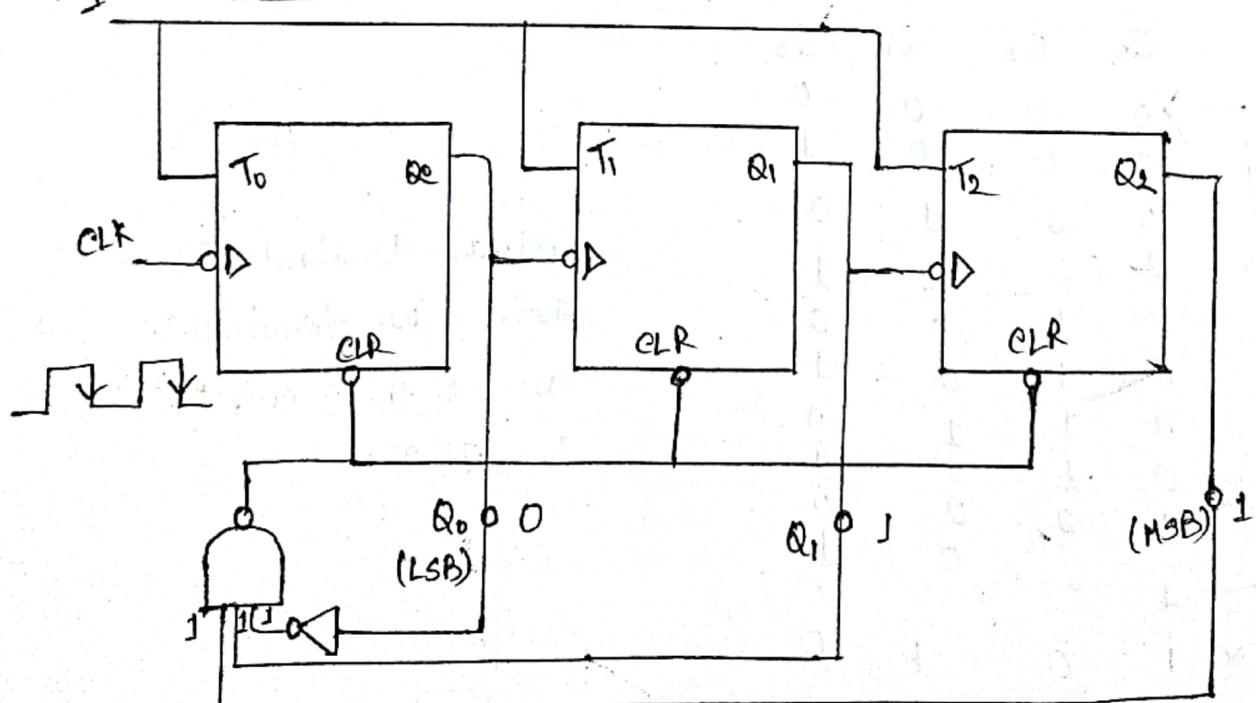
By 4 bits counter, at max we can have mod 16 counter.

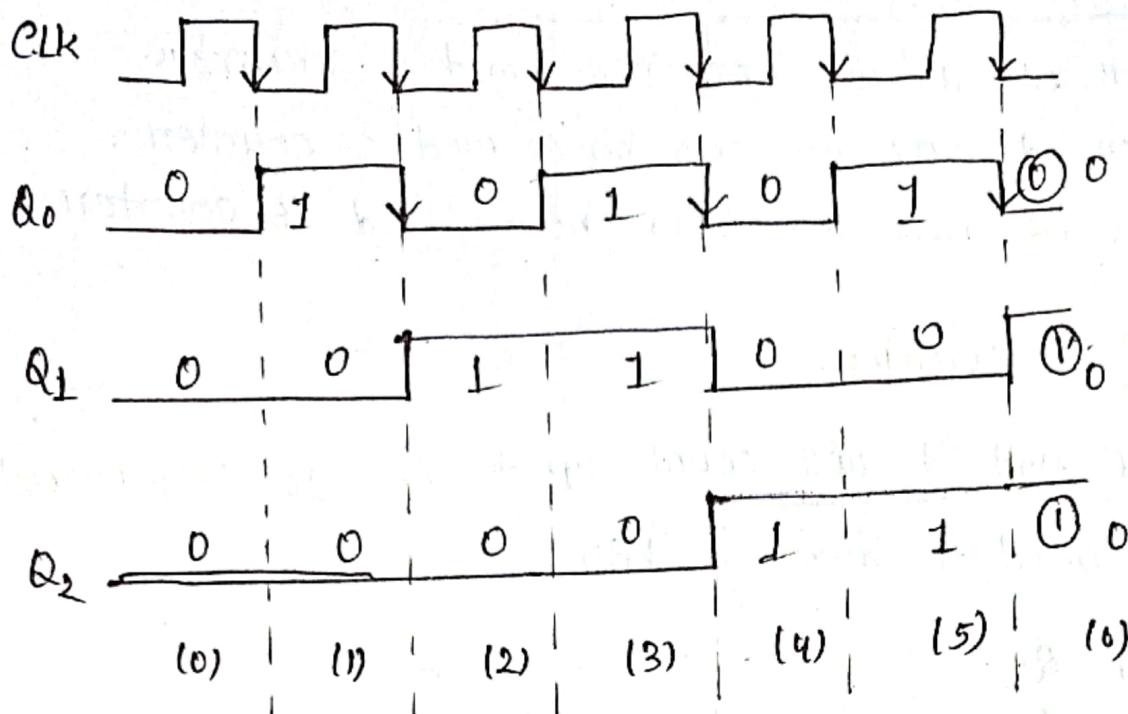
## Ex: Design modulo 6 counter.

It start from 0 and it will count up to 5. To represent 5 at least we need to have 3 bits

	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

once it complete this count up to 5 again it restart from 0.





### BCD counter (Decade counter):

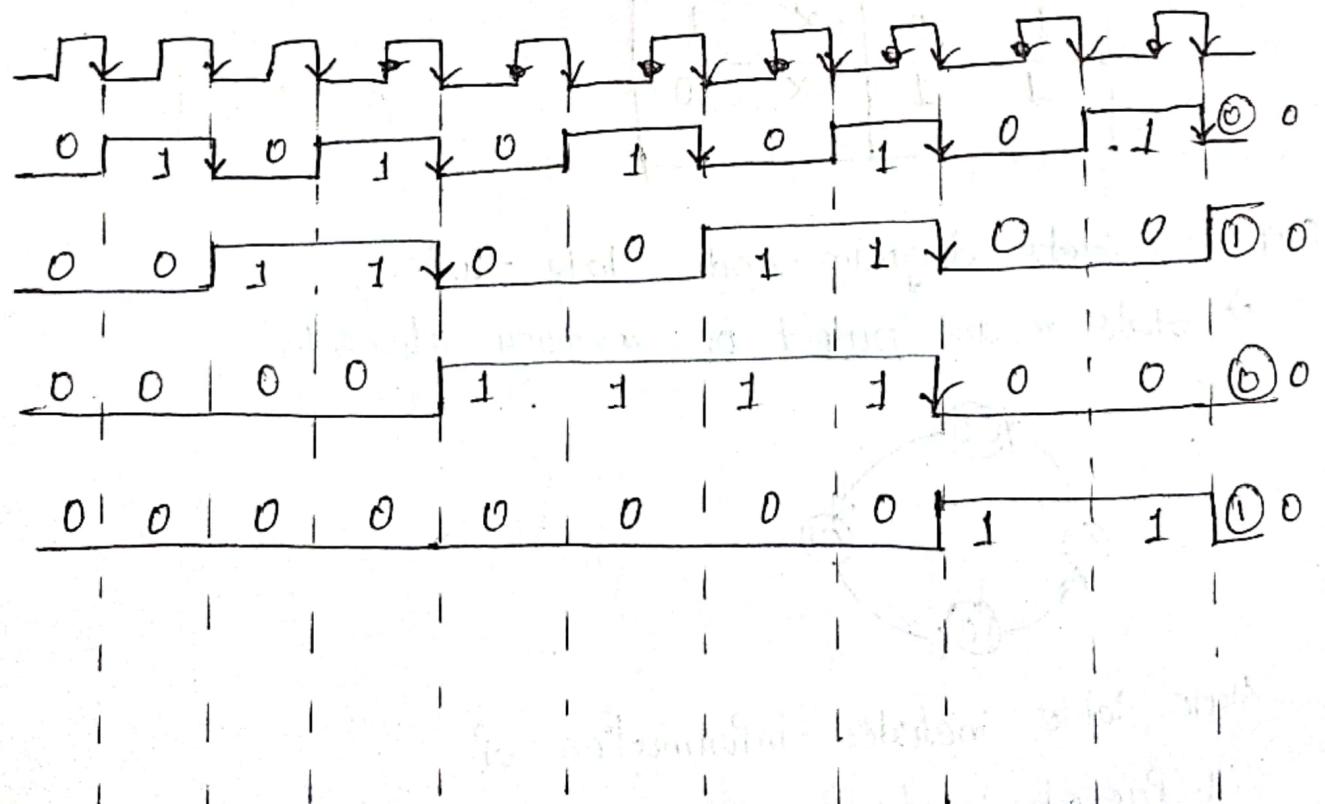
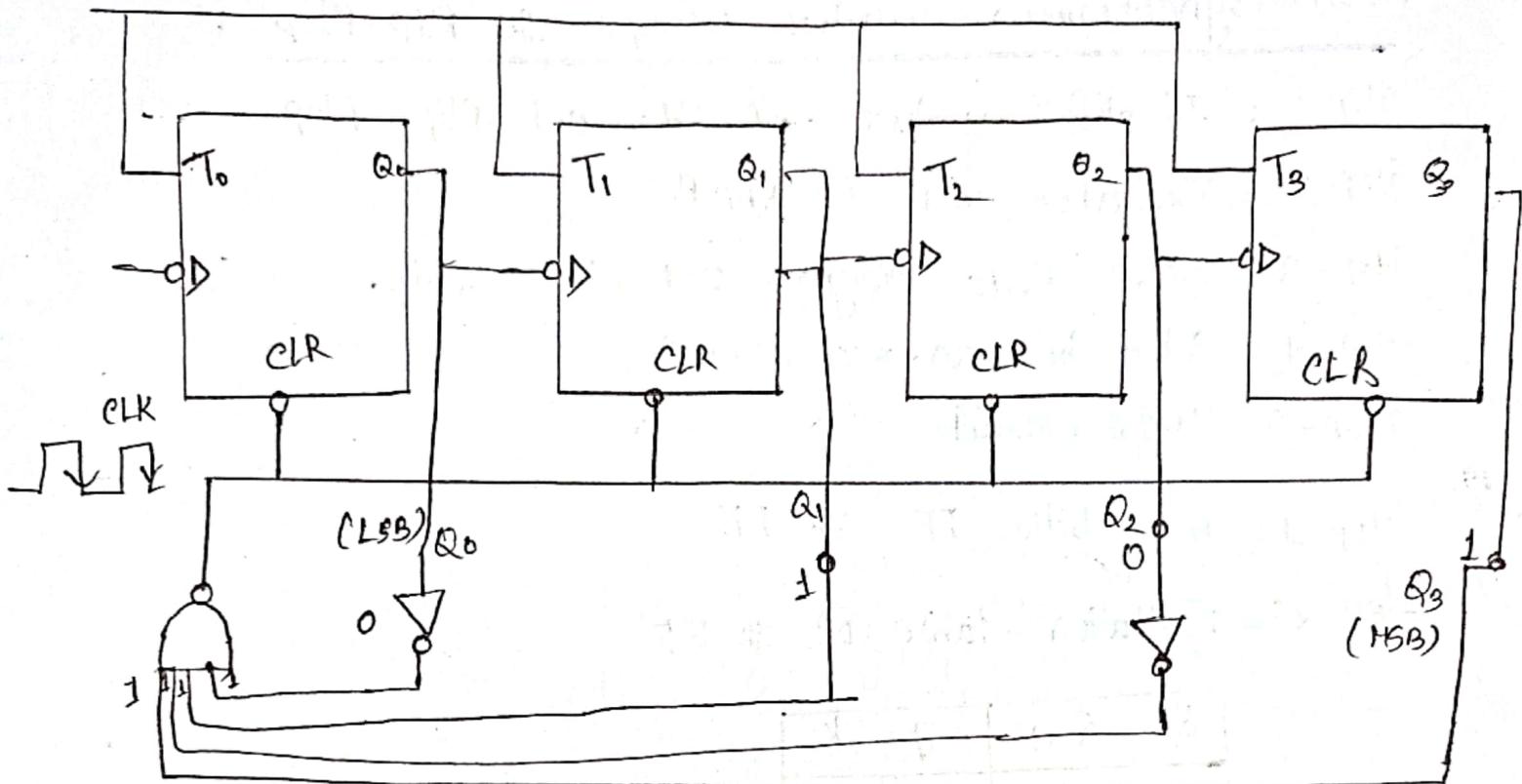
In BCD counter, It counts (0 to 9)

To count (0 to 9), It takes 4 bit

Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
x	1	0	0

clear terminal is active low terminal if CLR = 0 then output will be Q=0

"g"



2 bits synchronous counter using JK flip-flop

Step-1 : Identify number of bits and flip-flop

Step-2 : Excitation table of flip-flop

Step-3 : Make state diagram and state Table.

Step-4 : Solve boolean expression.

Step-5 : Make circuit.

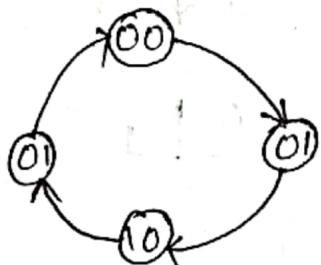
Step-1 :  $n = 2$  bits,  $FF = JK$  FF

Step-2 : Excitation table of JK FF

$Q_n$	$Q_{n+1}$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 : State diagram and state table.

→ State means output of memory elements.



State table includes information of

1. Preset state
2. Next state
3. Inputs of Flip Flop

$Q_1$	$Q_0$	$Q_1^+$	$Q_0^+$	$\oplus$	$J_1$	$K_1$	$J_0$	$K_0$
0	0	0	1		0	x	1	x
0	1	1	0		1	x	x	1
1	0	1	1		x	0	1	x
1	1	0	0		x	1	x	1

$Q_0 \ Q_1$   
excitation  
table

Step: 4- Find boolean expression.

$J_1$	$Q_0$	
$Q_1$	0	1
0	0	1
1	x	x

$K_1 \ Q_0$		
$Q_1$	0	1
0	0	1
1	0	1

$J_0 \ Q_0$		
$Q_1$	0	1
0	1	x
1	1	x

$K_0 \ Q_0$		
$Q_1$	0	1
0	x	1
1	x	1

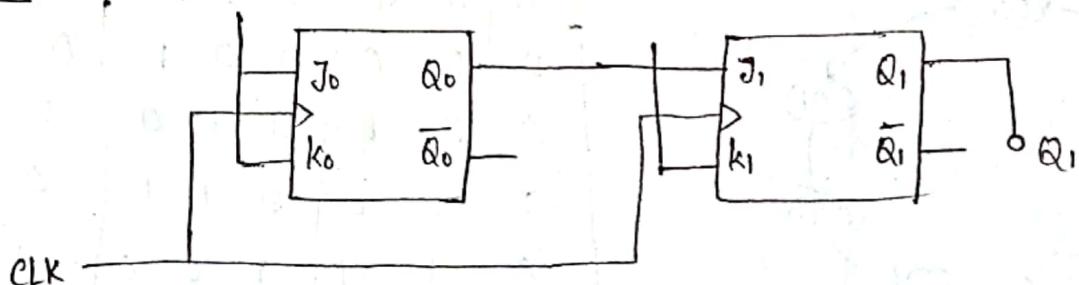
$$J_1 = Q_0$$

$$K_1 = Q_0$$

$$J_0 = 1$$

$$K_0 = 1$$

Step: 5-



clock is same, means synchronous counter.

3 bits synchronous counter to using T FF:

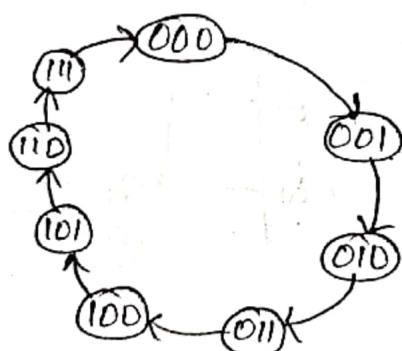
Steps are same as 2 bits.—

Step 1 -  $n = 3$  bits, FF = T FF

Step 2 - Excitation table of T FF

$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 3 - State of circuit means output of circuit.  
state diagram explains output transition diagram.



$Q_2$	$Q_1$	$Q_0$	$Q_2^+$	$Q_1^+$	$Q_0^+$	$T_2$	$T_1$	$T_0$
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Step: 4

		$T_2 = Q_1 Q_0$	
		00	01
$Q_2$	00	0	1
	01	0	1

		$T_1 = Q_0$	
		00	01
$Q_2$	00	0	1
	01	0	1

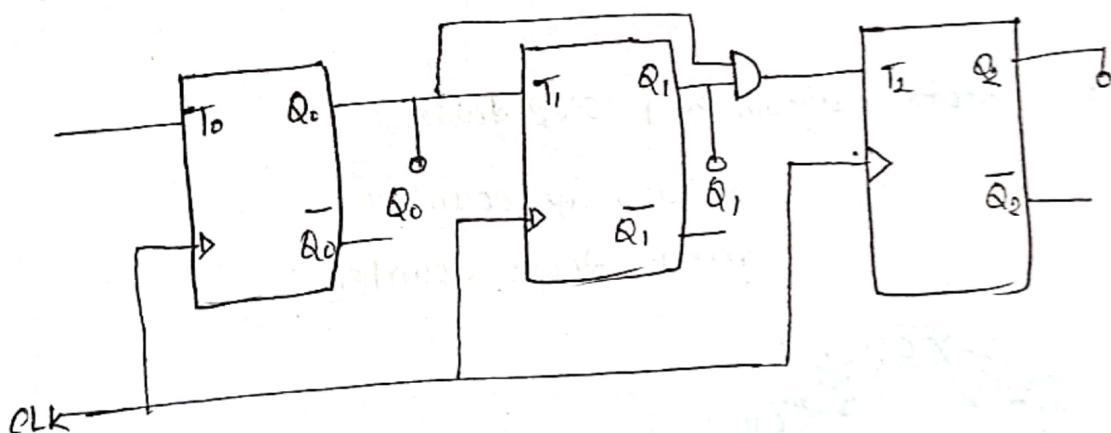
$$T_2 = Q_1 Q_0$$

$$T_1 = Q_0$$

$$T_0 = 1$$

$$\bar{T}_0 = 1$$

Step-5



### 3 bits synchronous updown counter:

Steps are same as before - (we selected T FF)

Step-1: Step-1:  $n=3$  bits,  $FF = T FF$

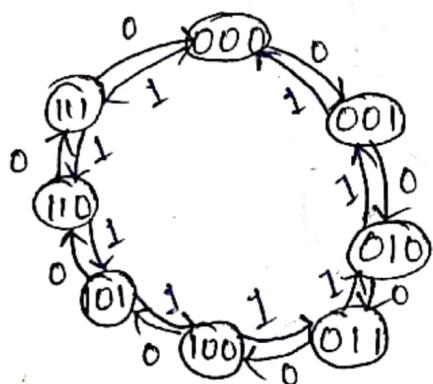
Step-2: Excitation table of T FF

$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

Step-3: State diagram and step table

$m=0$ , up counter

$m=1$ , down counter



$m$	$Q_2$	$Q_1$	$Q_0$	$Q_2^+$	$Q_1^+$	$Q_0^+$	$T_2$	$T_1$	$T_0$
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	1	0	0	0	1

Step: 4

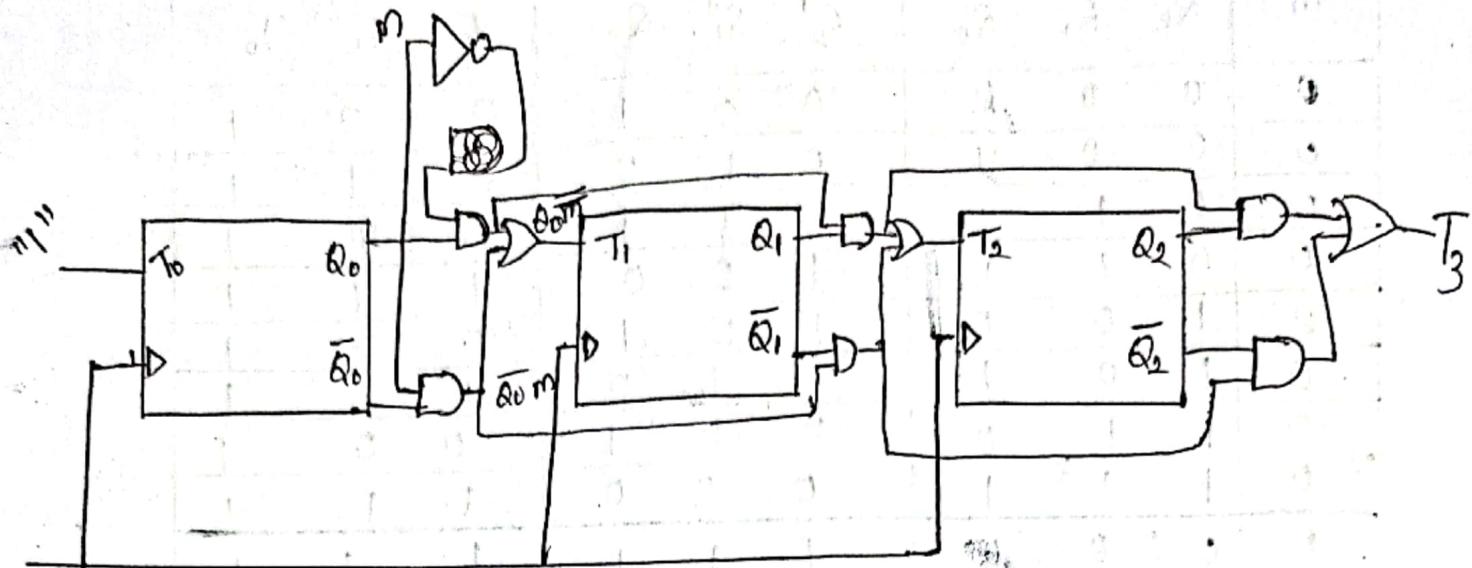
$$T_0 = 1$$

$Q_1 Q_0$	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1

$$T_1 = \overline{Q_0}m + \overline{Q}_0\overline{m}$$

$Q_1 Q_0$	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	1	1	0	0
10	0	0	0	0

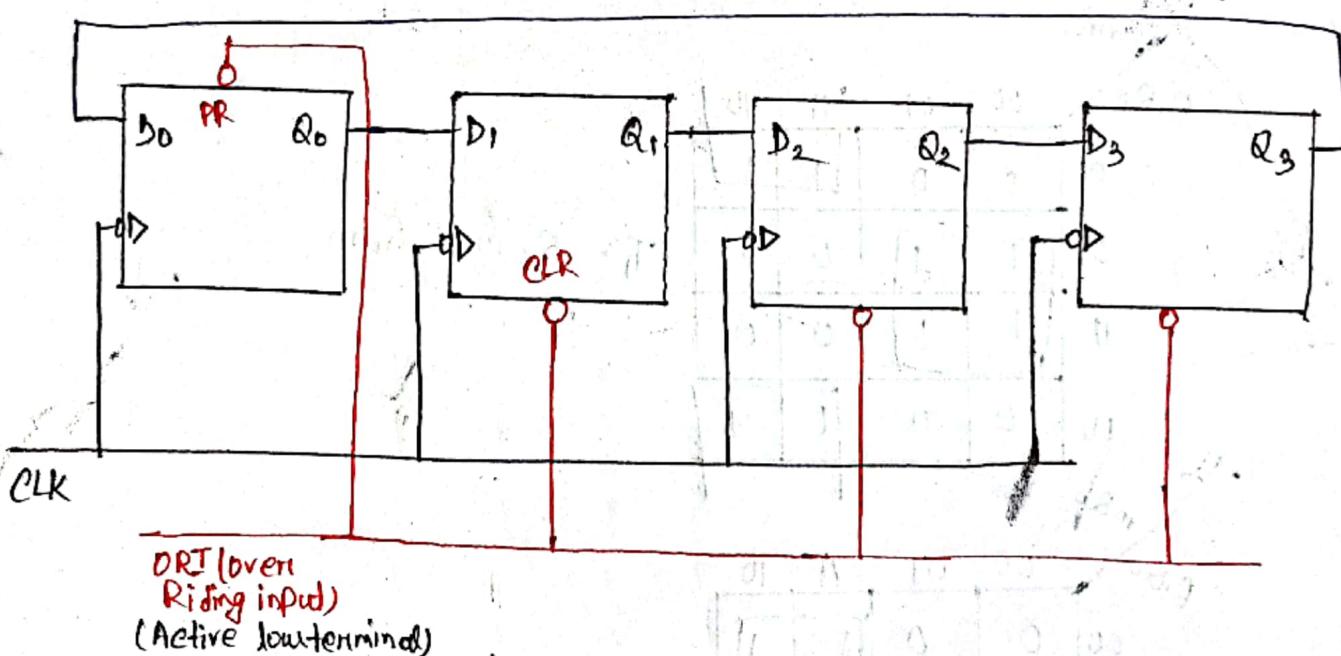
$$T_2 = Q_1 Q_0 \overline{m} + \overline{Q}_1 \overline{Q}_0 m$$



Ring Counter: It is application of shift register.

$$\begin{aligned} \text{No of states} &= \text{no of bits} \\ &= \text{no of FF} \end{aligned}$$

[For n bit counters  
total states =  $2^n$ ]



④ To initialize 1st state, we provide ORI (over Riding input)

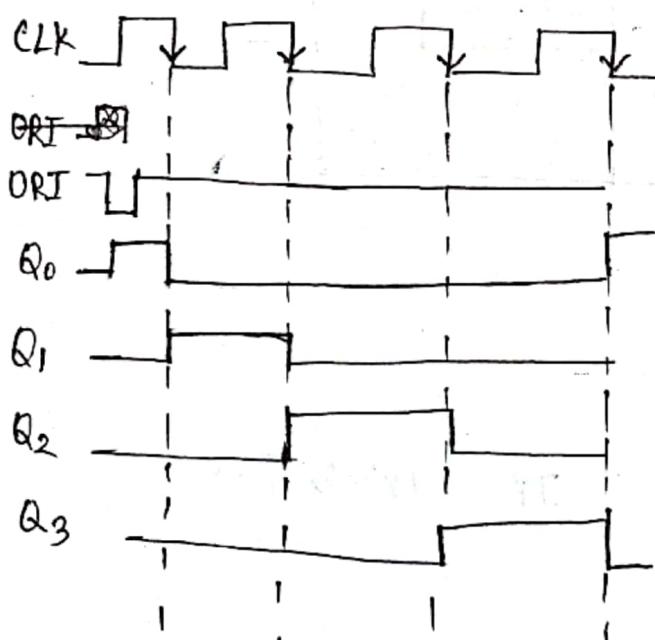
If  $PR = 0, Q = 1$

If  $CLR = 0, Q = 0$

## Application of shift register

ORI	CLK	$Q_0$	$Q_1$	$Q_2$	$Q_3$
-	X	1	0	0	0
1	↓	0	1	0	0
1	↓	0	0	1	0
1	↓	0	0	0	1
1	↓	1	0	0	0

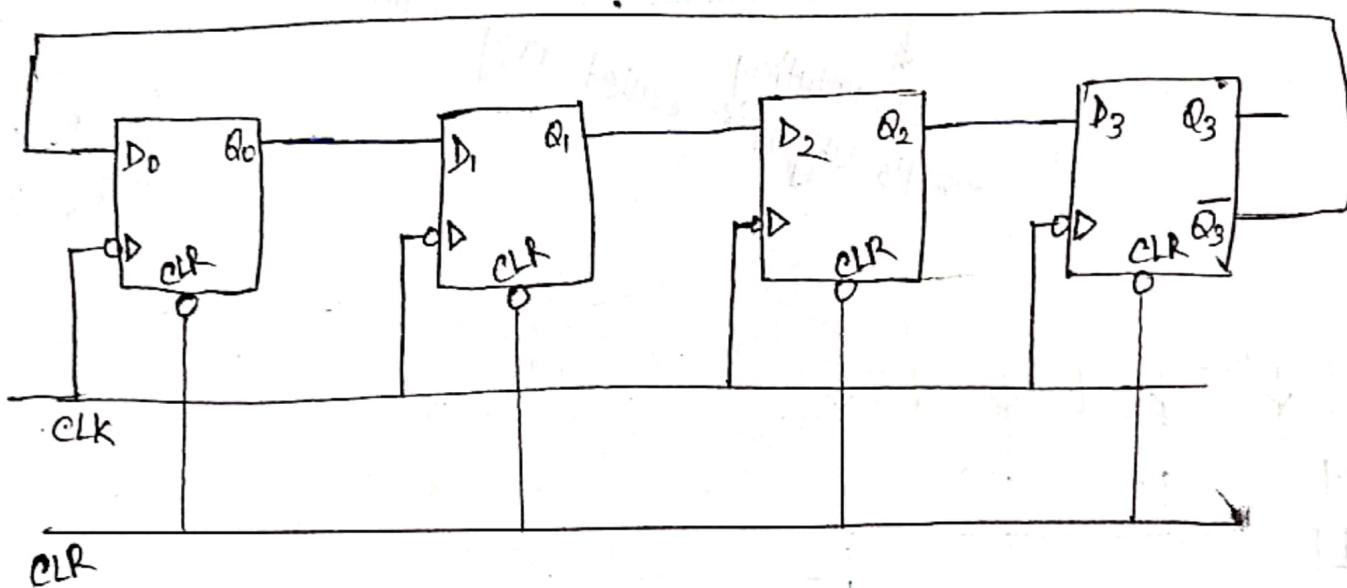
It's rotating  
That's why it is called ring counter.



# Johnson's counter | Twisted Ring counter / Switch Tail Ring counter:

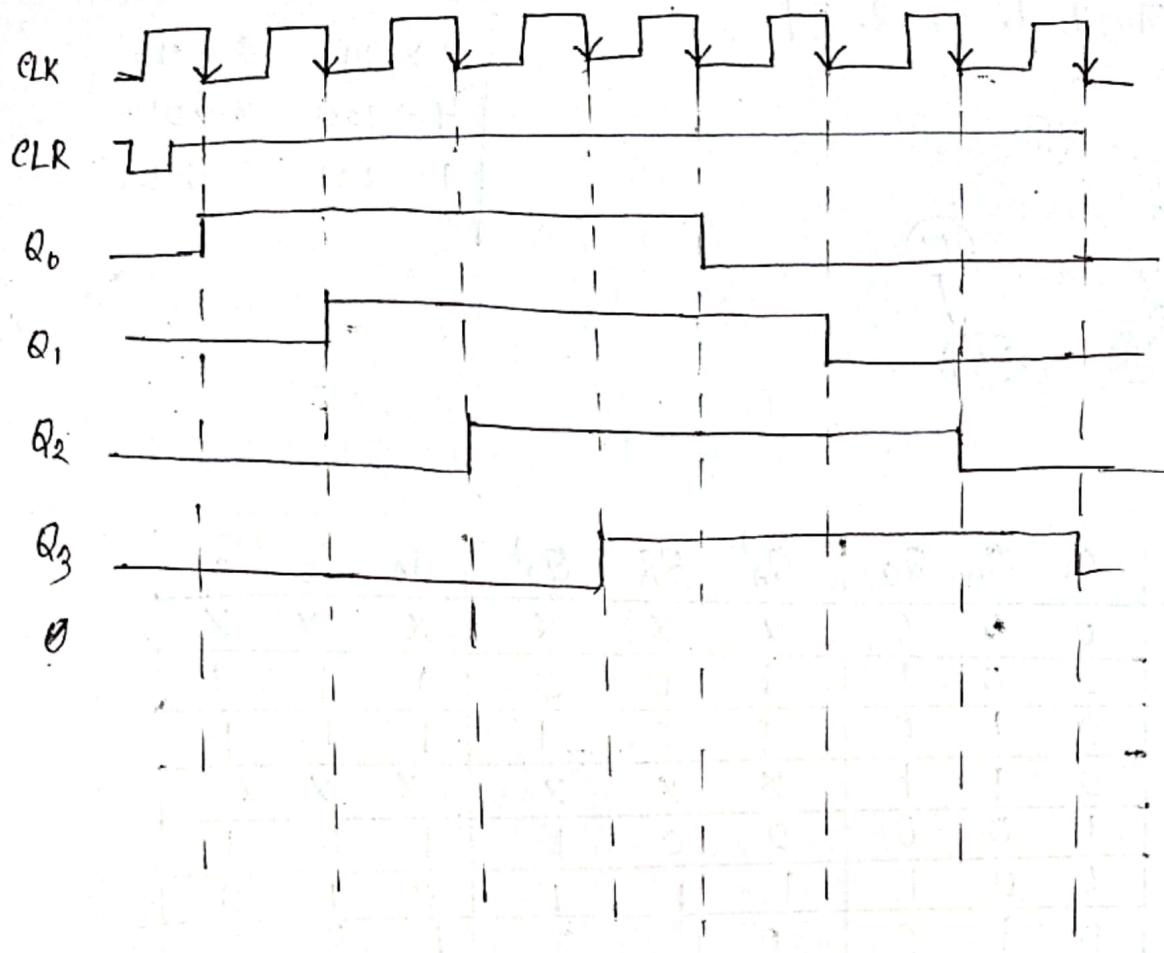
It is application of shift register

$$\begin{aligned} \text{No of states} &= 2 \times \text{No of FF} \\ &= 2 \times \text{No of bits} \end{aligned}$$



CLR	CLK	$Q_0$	$Q_1$	$Q_2$	$Q_3$
1	X	0	0	0	0
1	↓	1	0	0	0
1	↓	1	1	0	0
1	↓	1	1	1	0
1	↓	1	1	1	1
1	↓	0	1	1	1
1	↓	0	0	1	1
1	↓	0	0	0	1
1	↓	0	0	0	0

If  $CLR = 0, Q = 0$



### Arbitrary sequence counter (Example-1)

→ Make an <sup>given</sup> arbitrary sequence counter which counts from

7, 4, 1, 6, 2, 5

(Steps are same as  
synchronous counter)

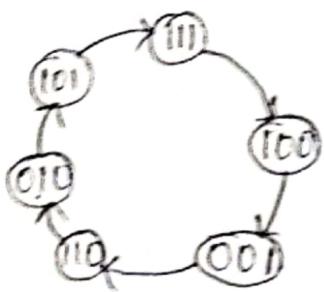
Step-1: No of FF = 3

Flip Flop = T Flip Flop

Step-2: Excitation table of T FF

$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

Step-3: [7, 4, 1, 6, 2, 5]



$7 \rightarrow 111$	$6 \rightarrow 110$
$4 \rightarrow 100$	$2 \rightarrow 010$
$1 \rightarrow 001$	$5 \rightarrow 101$

$Q_A$	$Q_B$	$Q_C$	$Q_A^+$	$Q_B^+$	$Q_C^+$	$T_A$	$T_B$	$T_C$
0	0	0	x	x	x	x	x	x
0	0	1	1	1	0	1	1	1
0	1	0	1	0	1	1	1	1
0	1	1	x	x	x	x	x	x
1	0	0	0	0	1	1	0	1
1	0	1	1	1	1	0	1	0
1	1	0	0	1	0	1	0	0
1	1	1	1	0	0	0	1	1

Step-4:

$T_A$   $\overline{Q_A} \& Q_B$

$Q_C$	00	01	10	11
0	x	1	1	1
1	1	x	0	0

$$T_A = \overline{Q_A} + \overline{Q_C}$$

$T_B$   $\overline{Q_B} \& Q_A$

$Q_C$	00	01	10	11
0	x	1	0	0
1	1	x	1	1

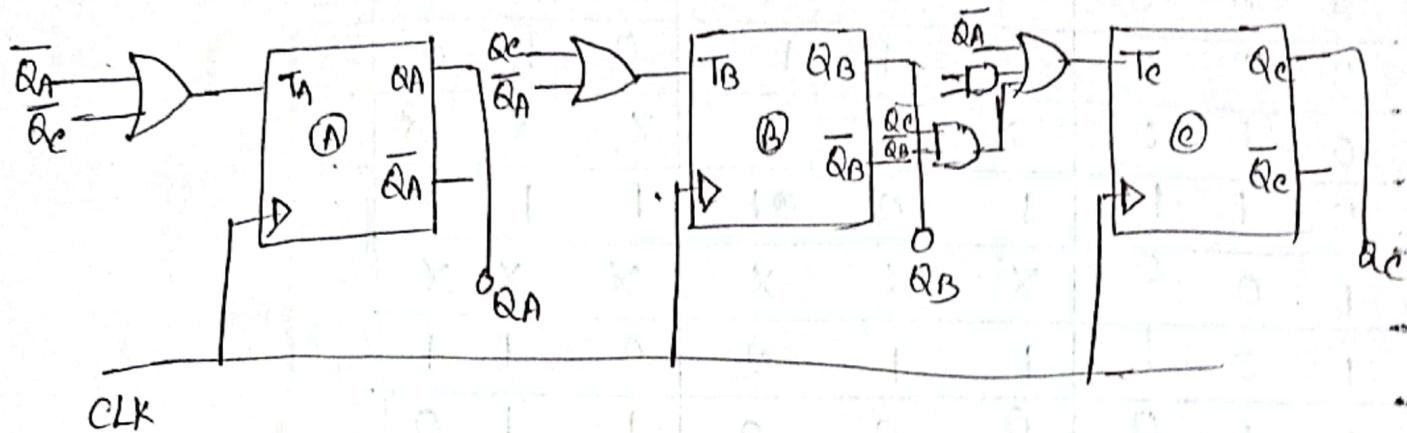
$$T_B = Q_C + \overline{Q_A}$$

$T_C$   $\overline{Q_A} \& Q_B$

$Q_C$	00	01	10	11
0	x	1	0	1
1	1	x	1	0

$$T = \overline{Q_A} + Q_C Q_B + \overline{Q_C} \overline{Q_B}$$

Step-5:



### Arbitrary sequence counter (Example-2)

⇒ Make a counter for given sequence 0, 1, 3, 5, 6

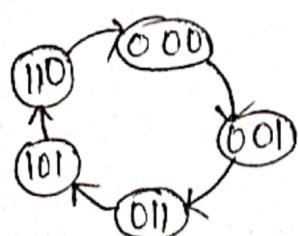
Step:1 - Total bits = Total FF = 3

Flip Flop = T Flip Flop

Step:2 - Excitation table of T FF

$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

Step:3 -



0 → 000
1 → 001
3 → 011
5 → 101
6 → 110

$Q_A$	$Q_B$	$Q_C$	$Q_A^+$	$Q_B^+$	$Q_C^+$	$T_A$	$T_B$	$T_C$
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	X	X	X	X	X	X
0	1	1	1	0	0	1	1	0
1	0	0	X	X	X	X	X	X
1	0	1	1	1	0	0	1	1
1	1	0	0	0	0	1	1	0
1	1	1	X	X	X	X	X	X

Step 4:

$\overline{Q_A} \overline{Q_B}$	00	01	10	11
$Q_C$	0	X	1	X
1	0	1	X	0

$$T_A = Q_B$$

$\overline{Q_A} \overline{Q_B}$	00	01	10	11
$Q_C$	0	X	1	X
1	1	1	X	1

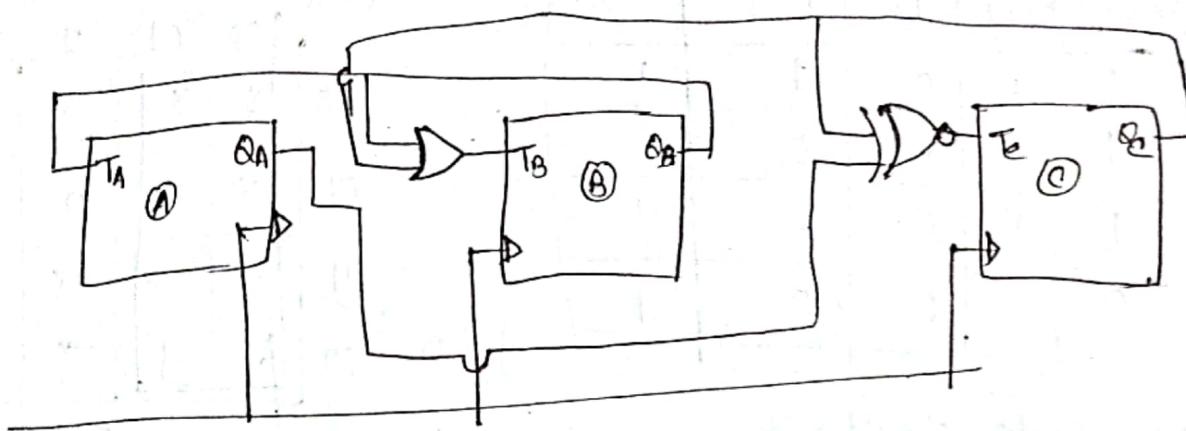
$$T_B = \overline{Q}_C + \overline{Q}_B$$

$\overline{Q_A} \overline{Q_B}$	00	01	10	11
$Q_C$	1	X	0	X
1	0	0	X	1

$$T_C = Q_C Q_A + \overline{Q}_C \overline{Q}_A$$

$$\rightarrow \text{XOR } Q_A \oplus Q_C$$

Step 5:



CLK

### Sequence Generator: (Example-1)

Generate sequence of 10110 ...

→ No of flip flop can be identify by  $L \leq 2^n - 1$

where  $L =$  length of sequence

$n =$  Number of flip flop minimum

Hence,  $L = 5$

$$\therefore 5 \leq 2^n - 1$$

$$\Rightarrow 5 + 1 \leq 2^n$$

$$\Rightarrow 6 \leq 2^n$$

$$\Rightarrow n = 3 \quad [n = 3 \text{ means } 3 \text{ ff}]$$

A	B	C	D	F (Feedback)
1	0	1	1	0
0	1	0	1	1
1	0	1	0	1
1	1	0	1	0
0	1	1	0	1

$F = \overline{A} + \overline{D}$

F	AB	CD	00	01	11	10
0	00	x	x	x	x	x
1	01	x	1	0	x	
x	11	x	x	x	0	
1	10	x	1	x	1	

→ Here, state should not repeat. If state is repeating then we should add one more FF.

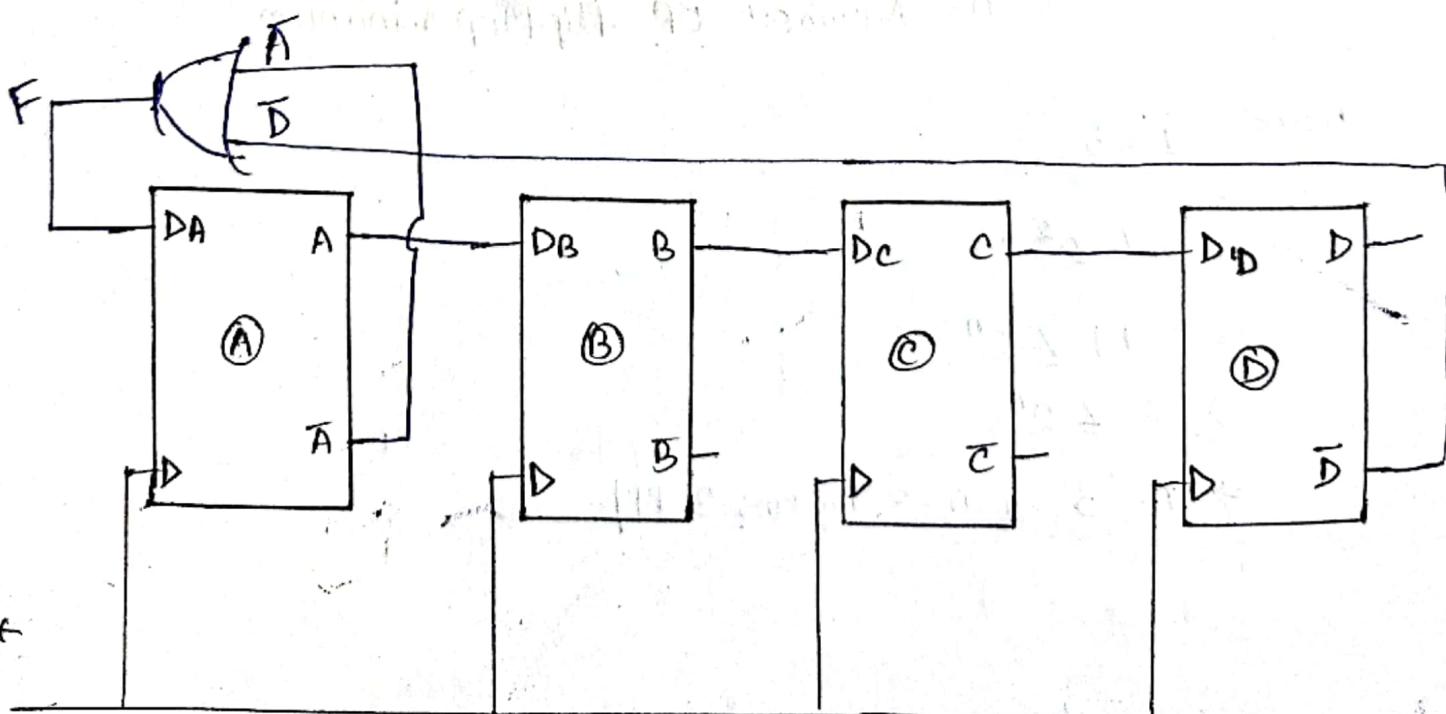
④ [ 1st ৰ ABC মৰ ক্ষমতি, Then state (10) ]

repeat হ্যাতু তাই আবশ্য D ad ক্ষমতি ]

D ad ক্ষমতি এখ আবশ্য বেল state Repeat

হ্যাতু তাই আবশ্য মোট FF Ad ক্ষমতি তা, Total FF = 4(A B C D)

Then Feedback connect কৰা



Example-2 : Generate sequence of 110010

$$L \leq 2^n - 1$$

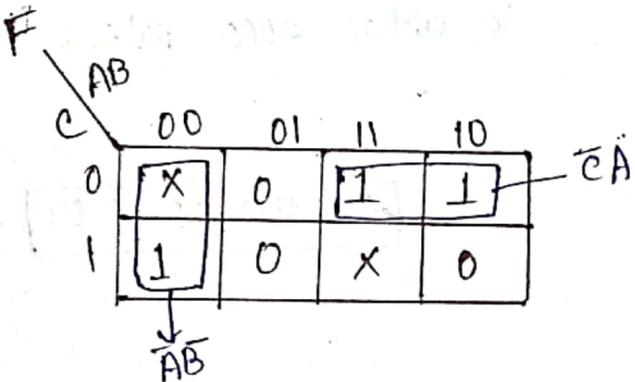
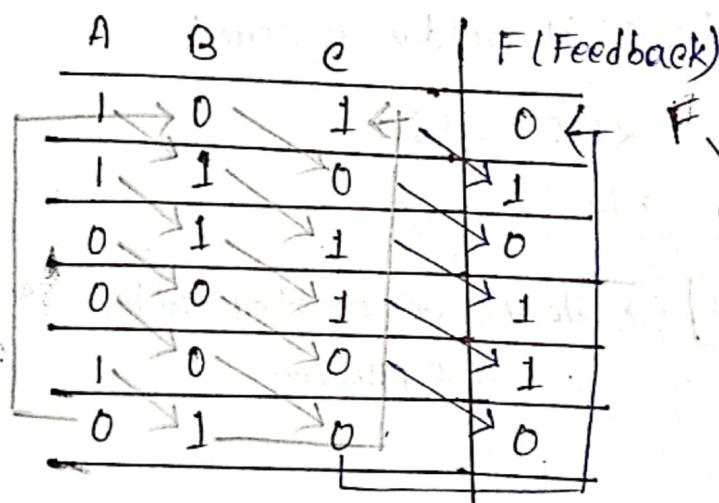
$$\text{Hence } L = 6$$

$$6 \leq 2^n - 1$$

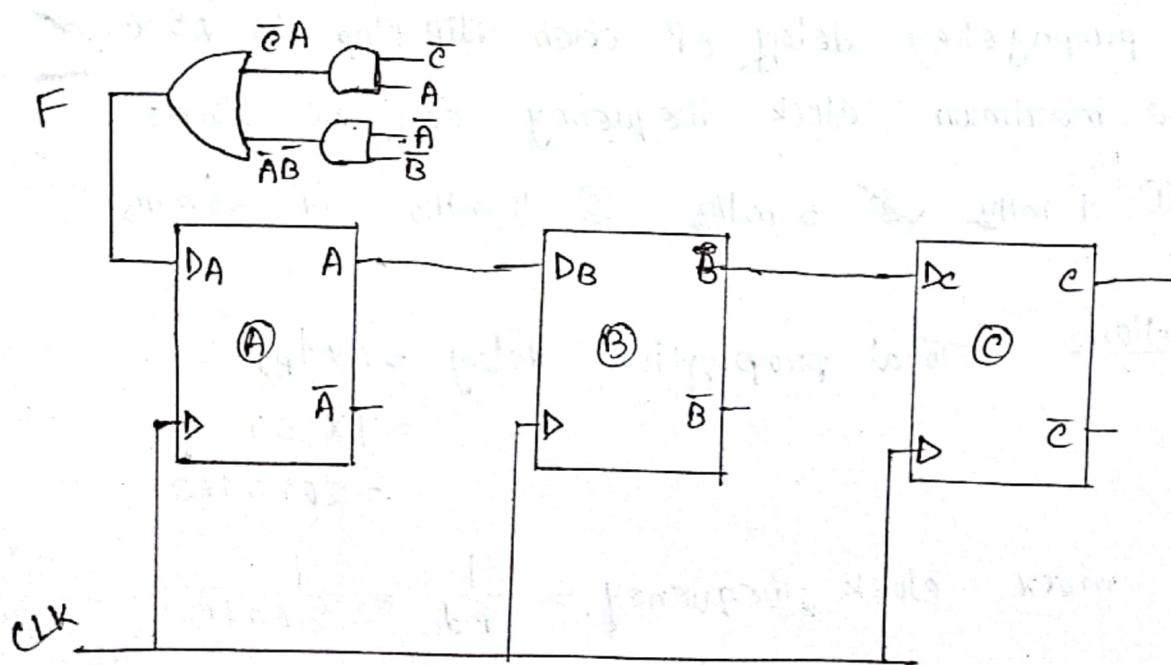
$$\Rightarrow 6 + 1 \leq 2^n$$

$$\Rightarrow 7 \leq 2^n$$

$$\Rightarrow n = 3$$



$$F = \bar{C}A + \bar{A}\bar{B}$$



### Examples on counter:

① If counter is having 10 FF. J<sub>t</sub> is initially 0. what count will it hold after 2060 pulses.

Solution: 10 FF means it is 10 bits counter.

$$\text{For 10 bits counter total count} = 2^{10} \\ = 1024$$

→ After 1024 pulses it holds 0 count.

→ After 1024 (2048) pulses, it holds 0 count.

$$\text{So after 2060 pulses} = 2060 - 2048$$

$$= 12$$

0 0 0 0 0 0 1 1 0 0 → status of counter after  
2060 pulses.

② A 4 bits mod 16 counter is made by JK FF. If propagation delay of each flip flop is nsec. The maximum clock frequency can be used.

- ① 4 mHz    ② 5 mHz    ③ 10 mHz    ④ 20 mHz

Solution: Total propagation delay  $\rightarrow n \times t_{pd}$   
 $= 4 \times 50$   
 $= 200 \text{ nsec}$

$$\text{max clock frequency} \rightarrow \frac{1}{P.D} = \frac{1}{200 \text{ nsec}} = \frac{10^9}{200} \\ \rightarrow 5 \text{ mHz}$$

③ A certain JK Flip Flop has propagation delay of  $t_{pd} = 12$ . The largest ripple counter that can operate at 10 mHz is

- ① mod 16 ② mod ⑧ ~~③~~ mod 256 ④ mod 128

Solution: Total propagation delay =  $\frac{1}{f} = \frac{1}{10\text{mHz}} = 100 \text{ nsec}$

$$n = \frac{\text{total propagation delay}}{t_{pd}}$$

$$= \frac{100}{12}$$

$\approx 8$  bits

$$\begin{aligned} \text{mod} &= 2^n \\ &= 2^8 \end{aligned}$$

$$= 256$$

mod- 256 counter