



আন্তর্জাতিক ইসলামী বিশ্ববিদ্যালয় চট্টগ্রাম
الجامعة الإسلامية العالمية شيتاغونغ
International Islamic University Chittagong

LAB REPORT/Assignment

Student Identity:

Name:	Intahadul Hoque
ID:	C221059
Semester:	Spring'23
Section:	3BM
Department:	CSE

Experiment Information:

Experiment No:	01
Experiment Name:	Counter, RAM, ROM, memory unit, magnitude comparator, Carry look Ahead related p. solve
Course Code:	CSE-2323
Course Title	Digital EE logic Design
Date of Experiment:	5/19/2023
Date of Submission:	31/05/2023

Submitted to:

--

Remarks:

--

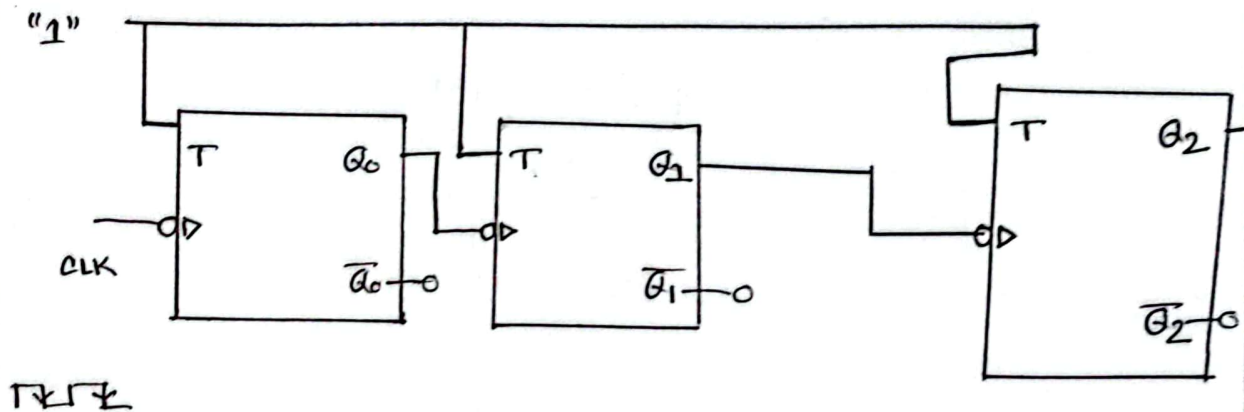
TOPIC - counter

1a Design an asynchronous ripple-down counter.

(Act - 22)

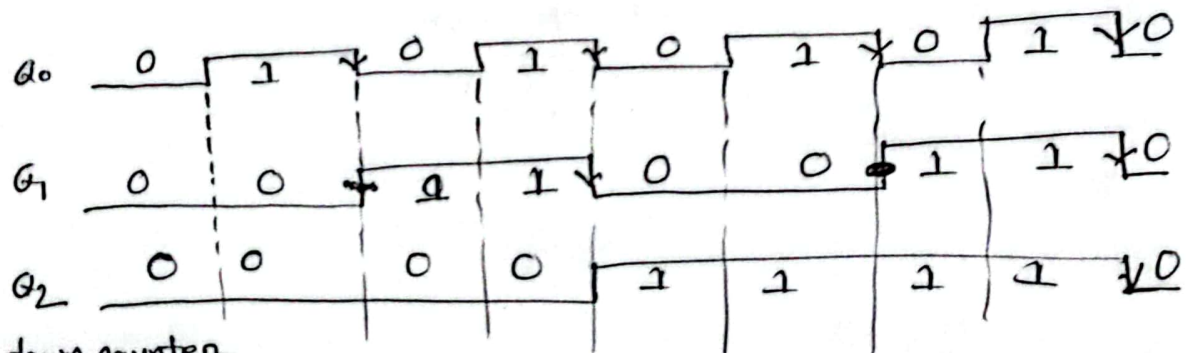
Soln:-

(sp - 22)

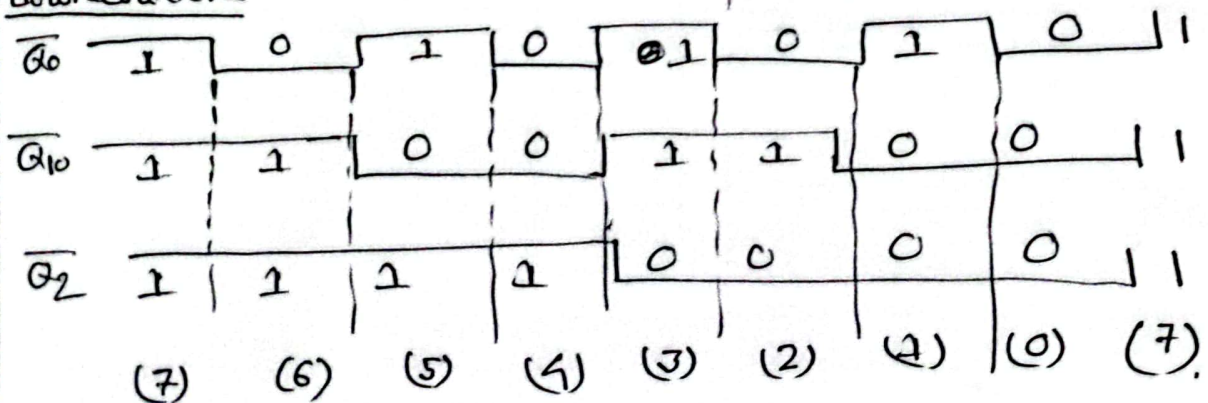


TrkTr

CLK



down counter

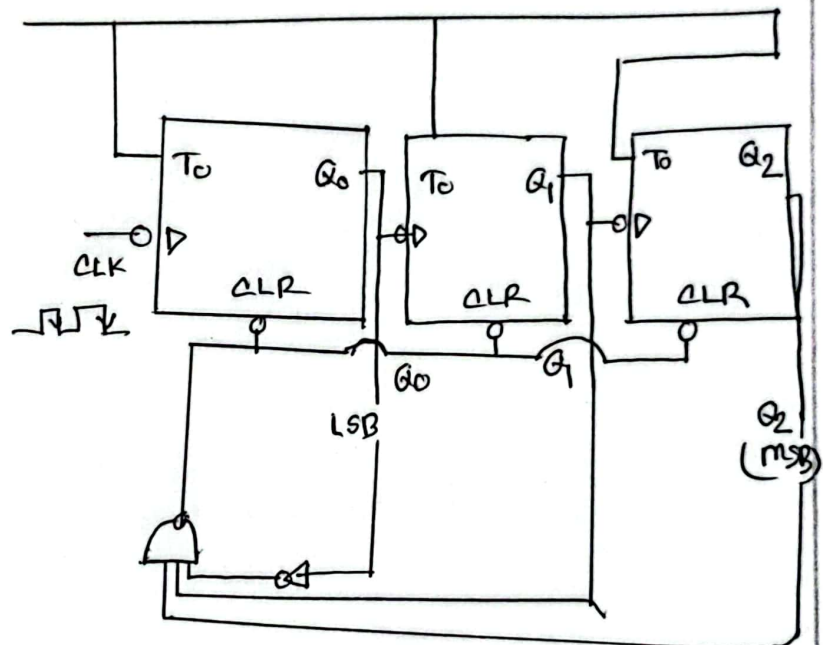


2. (a) Design a modulo counter by asynchronous counter. (Aut-22) (Sp-22)

Ex: Modulo 6 counter.

It starts from 0 and it will count up to 5.

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0



CLK	↓	↓	↓	↓	↓	↓	↓	↓	↓
Q_0	0	1	0	1	0	1	0	1	0
Q_1	0	0	1	1	0	0	1	0	0
Q_2	0	0	0	0	1	1	1	0	0
	(0)	(1)	(2)	(3)	(4)	(5)	(6)		

3(a) Design a 2 bits synchronous counter by JK

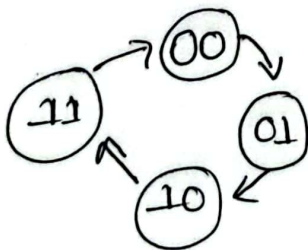
Flip-Flop. [Au- 22]

There are 2 bits . So, Flip-Flop = JK Flip Flop.

Excitation table of JK Flip-Flop :-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

State diagram :-



State table :-

Q_1	Q_0	Q_1^+	Q_0^+	J_1	K_1	J_0	K_0
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

Now, finding boolean expression :-

J_1

Q_0	0	1
Q_1	0	1
	X	X

$J_1 = Q_0 \oplus 1$

K_1

Q_0	0	1
Q_1	0	1
	X	X

$K_1 = Q_0$

J_0

Q_0	0	1
Q_1	0	1
	1	X

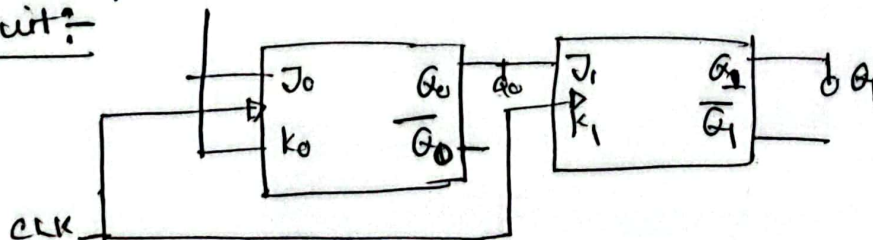
$J_0 = 1$

K_0

Q_0	0	1
Q_1	0	1
	X	1

$K_0 = 1$

Circuit :-



4(a) Design counter using SR flip flop with repeated

binary sequence : 0, 1, 3, 2, 6, 4, 5, 7. (Au-22) (Sp-22)

Total bits = total flip flop = 3

flip flop required = T flip flop.

Excitation Table of T flip flop:

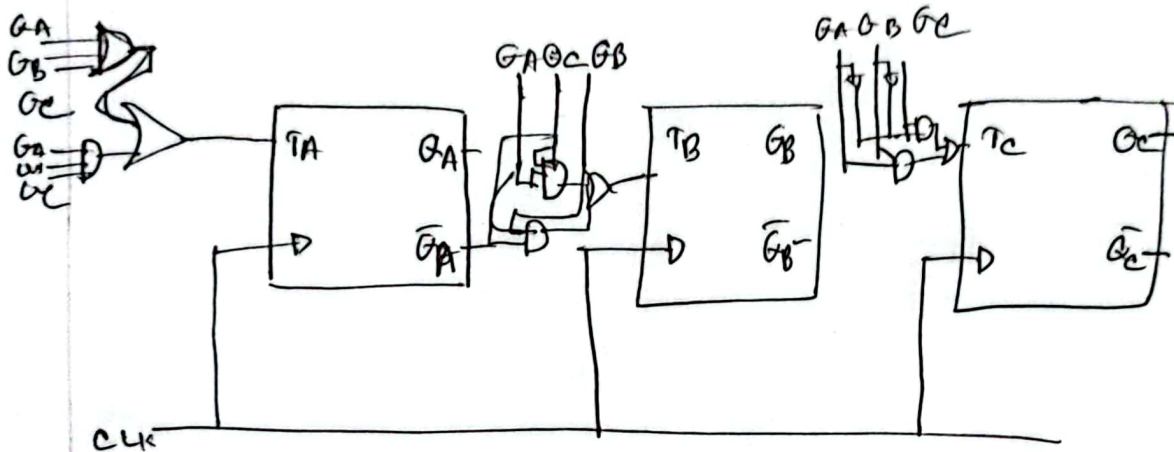
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

state table (0, 1, 3, 2, 6, 4, 5, 7)

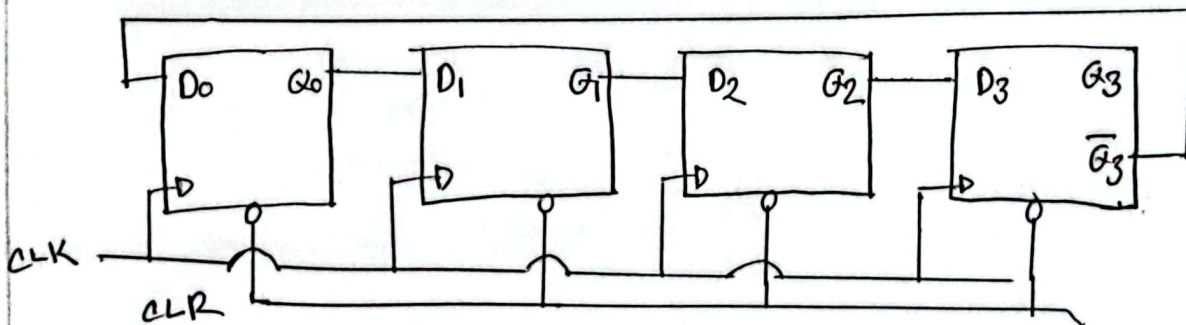
Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	0	0
0	1	1	0	1	0	0	0	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	1	0	1	0
1	1	0	1	0	0	0	1	0
1	1	1	x	x	x	x	x	x

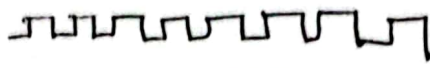
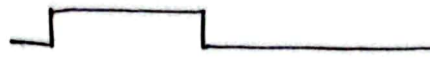



T _A				T _B				T _C			
Q _A Q _B Q _C				Q _A Q _B Q _C				Q _A Q _B Q _C			
000	0	0	0	000	0	0	0	000	1	0	1
001	0	0	0	001	1	0	0	001	1	0	1
010	0	0	1	010	0	0	1	010	1	0	1
011	0	0	1	011	0	1	0	011	1	0	1
100	0	1	0	100	0	1	0	100	1	0	1
101	0	1	1	101	0	1	1	101	1	0	1
110	0	1	1	110	1	0	0	110	1	0	1
111	0	1	1	111	1	0	1	111	1	0	1

$$T_A = Q_A Q_B Q_C + \bar{Q}_A \bar{Q}_B \bar{Q}_C \quad T_B = Q_A Q_C + \bar{Q}_A \bar{Q}_B \bar{Q}_C \quad T_C = \bar{Q}_A \bar{Q}_B Q_C + Q_A Q_B$$



4(b) Design Johnson's counter.



CLR	CLK	Q ₀	Q ₁	Q ₂	Q ₃	
W	X	0	0	0	0	<u>wave form</u>
1	↓	1	0	0	0	clk 
1	↓	1	1	0	0	Q ₀ 
1	↓	1	1	1	0	Q ₁ 
1	↓	1	1	1	1	Q ₂ 
1	↓	0	1	1	1	Q ₃ 
1	↓	0	0	1	1	
1	↓	0	0	0	1	
1	↓	0	0	0	0	

1(B) Design a J-K Flip Flop and show its characteristic equation, characteristic table and logic diagram. (Sp-22).

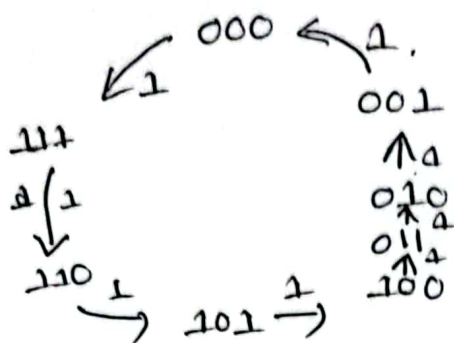
5(b) Design 3bit down counter with T-Flip Flop. (Autum-19)

Given that, $n = 3$ bits Flip Flop = T Flip Flop.

Excitation table of T Flip Flop:-

Q _n	Q _{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

$m=1$, Down counter.



state table :-

m	G_2	G_1	G_0	G_2^+	G_1^+	G_0^+	T_2	T_1	T_0
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	1	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	1	0	0	0	1

G_2	G_1	G_0	T_2	G_2	G_1	G_0	T_2	G_2	G_1	G_0	T_2
00	01	11	10	00	01	11	10	00	01	11	10
1	0	1	0	1	0	1	0	1	0	1	0
1	1	0	1	1	1	0	1	1	1	0	1

$T_0 = 1$.

$$T_1 = \overline{G_1}$$

$$T_2 = \overline{G_2}$$

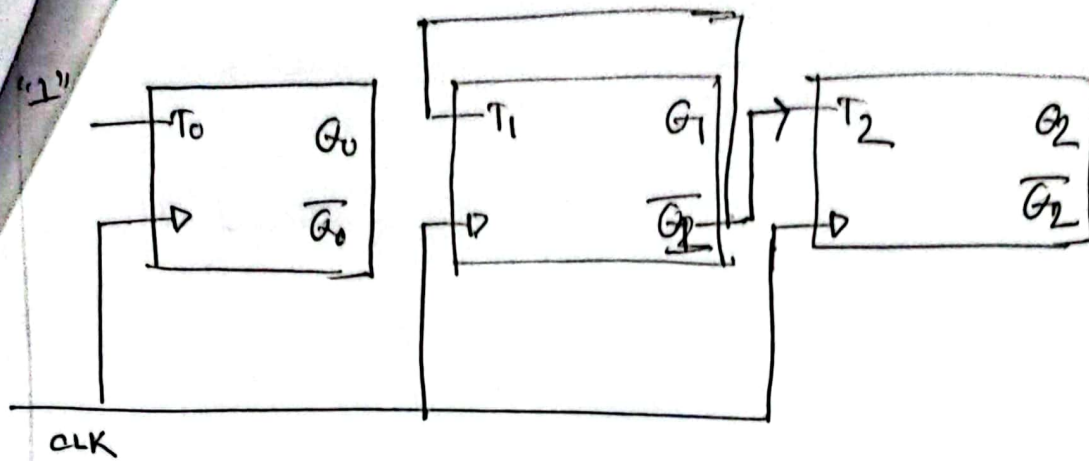


Fig. 1 :- circuit diagram.

TOPIC : RAM & ROM

(5a) Define Rom [Sp-22]

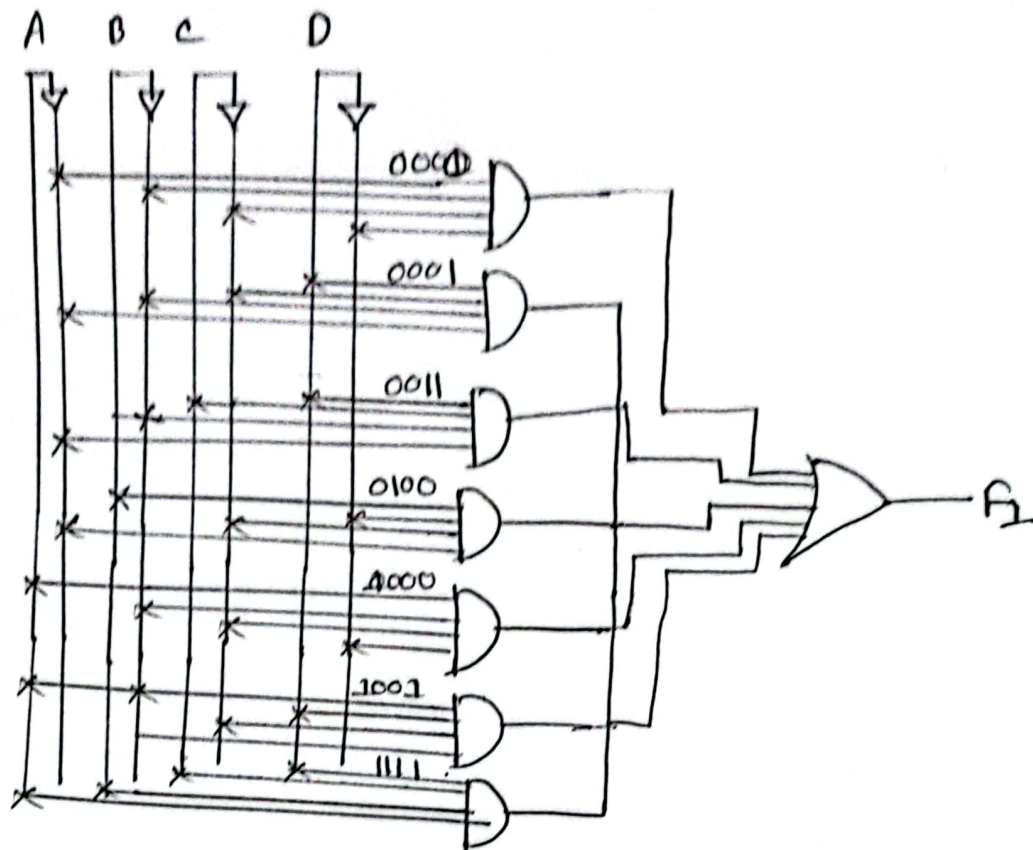
A Rom is essentially a memory device in which a fixed set of binary information is stored.

5(b) Implement the function with

Rom . $F(x, y, z) = \sum (0, 1, 3, 4, 8, 9, 15)$

max bits needed = 4 bits

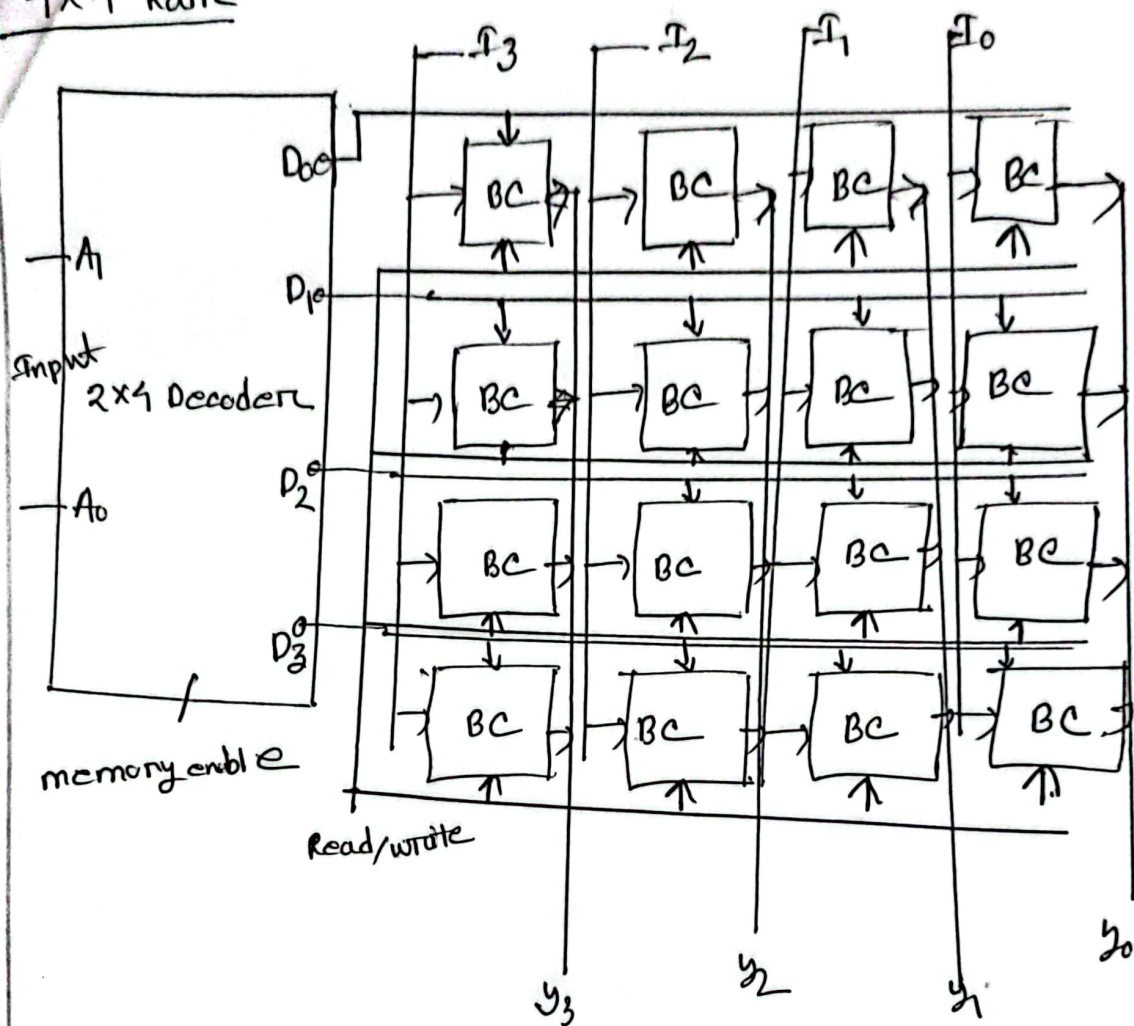
Now, designing the function with Rom.



3C what is memory cell? Design 4×4 Ram and describe its operation. (Autum-19).

Memory Cell:- The memory is the fundamental building block of computer memory. The memory cell is an electronic circuit that stores one bit of binary information and it must be set to be store logic 1 and reset to store a logic 0.

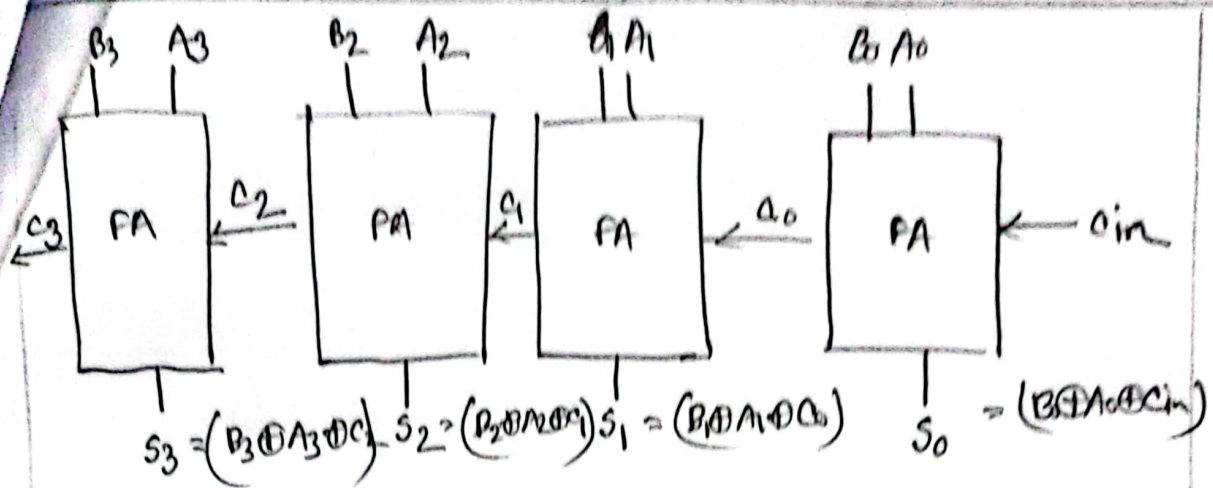
4x4 Ram



Topic : Look Ahead carry generators
; Comparator & Sequential circuit

1(a) Design a look ahead carry generator

for 3 bit full adder.



$B_1 A_1 c_0$	c_1
0 0 0	0
0 0 1	0
0 1 0	0
0 1 1	1
1 0 0	0
1 0 1	1
1 1 0	1
1 1 1	1

$$c_1 = B_1 A_1 c_0 + B_1 A_1 \bar{c}_0 + B_1 \bar{A}_1 c_0 + \bar{B}_1 A_1 c_0$$

$$c_1 = B_1 A_1 (c_0 + \bar{c}_0) + c_0 (B_1 \bar{A}_1 + \bar{B}_1 A_1)$$

$$c_1 = B_1 A_1 + (B_1 \oplus A_1) c_0$$

$$c_i = B_i A_i + (B_i \oplus A_i) c_{i-1}$$

$\underbrace{\quad}_{\text{Carry generator}} + \underbrace{\quad}_{\text{Carry propagator}}$

for $i=0$

$$c_0 = G_0 + P_0 c_{in}$$

for $i=1$

$$c_1 = G_1 + P_1 c_0$$

$$= G_1 + P_1 [G_0 + P_0 c_{in}]$$

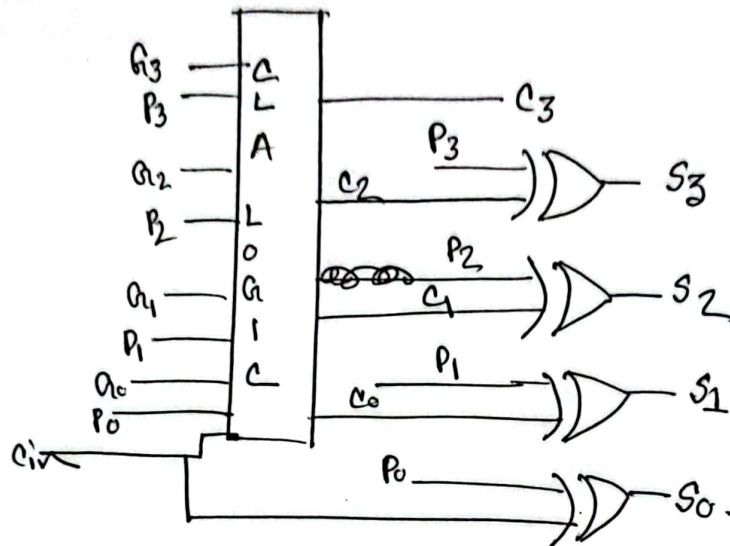
$$c_2 = G_2 + P_2 c_1$$

$$= G_2 + P_2 [G_1 + P_1 [G_0 + P_0 c_{in}]]$$

$$= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_1 P_2 P_0 c_{in}$$

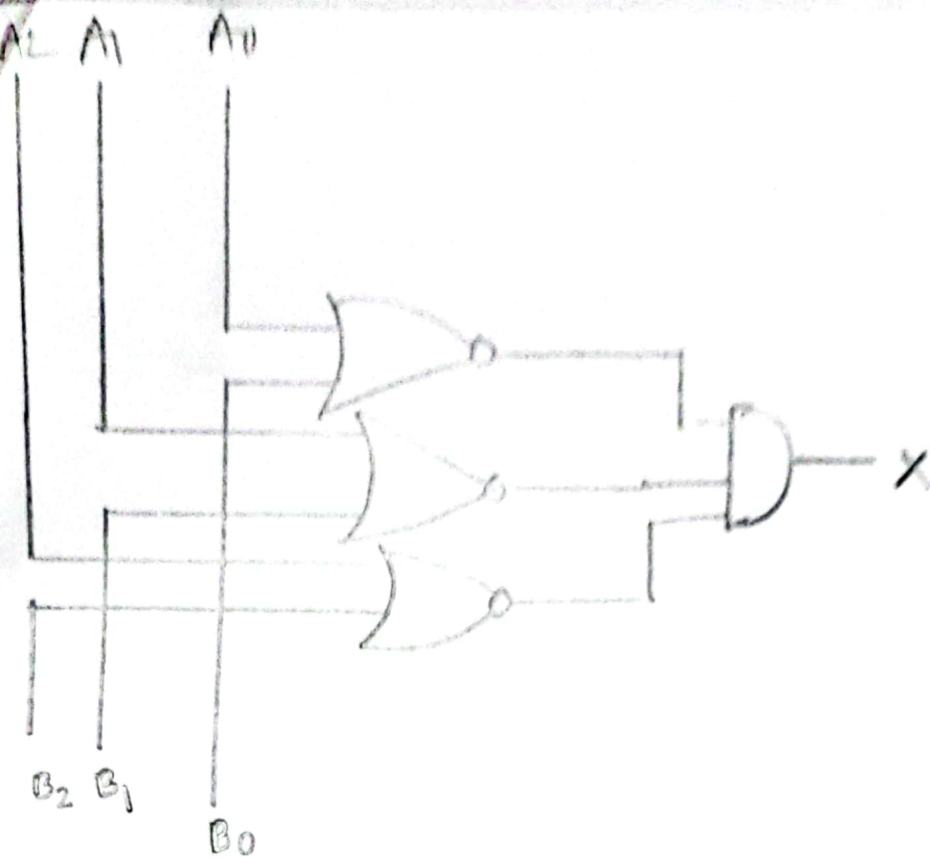
$$C_3 = G_3 + P_3 C_2$$

$$= G_3 + P_3 (G_2 + P_2 C_1)$$



2(b) Design a circuit that compares two 3-bit numbers A and B, if they are equal the circuit has one output n so that $n=1$ if $A=B$, and $n=0$ if $A \neq B$. Show the output providing data into the circuit [Aut-22]

Circuit that compare 3 bit numbers :-



$$X = (A_0 \odot B_0) \cdot (A_1 \odot B_1) \cdot (A_2 \odot B_2)$$

A_2	A_1	A_0	B_2	B_1	B_0	X
0	0	0	0	0	0	1
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	0
0	0	0	1	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1