Bismillahhir Rahmanir Rahim

আন্তর্জাতিক ইসলামী বিশ্ববিদ্যালয় চট্টগ্রাম

الجامعة الإسلامية العالمية شيتاغونغ

International Islamic University Chittagong

Lab Report 02 on

Intel 8086 Microprocessor's Internal Architecture

Submission Date & Day
23 August, 2022 (Tuesday)

Course Title: Microprocessor, Microcontrollers & Embedded System

Course Code: CSE-3524

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Experiment No.: 02

Experiment Name: Intel 8086 Microprocessor's Internal Arcchitecture.

Introduction: 8086 Microprocessor is an enhanced version of 8085 microprocessor that was designed by intel by 1976. It is a 16-bit mp having 20 address lines and 16 data lines that provides upto 1MB storage.

Abstract: This experiment aims to know the internal architecture of intel 8086 mp in details.

Features of 8086 MP: The most powerful features of 8086 microprocessor are given in the following-

- It has an instruction queue, which is capable of storing 6 instruction byte from the memory resulting in faster processing.
- It was the first 16-bit processor having 16 bit ALU, 16 bit registers, internal data bus and 16 bit external data bus.

- It uses two stages of pipelineing i.e fetch stage and Execute stage, which improves perfomence.
- Fetch storage can prefetch up to 6 bytes of instruction and storage them in the queue.

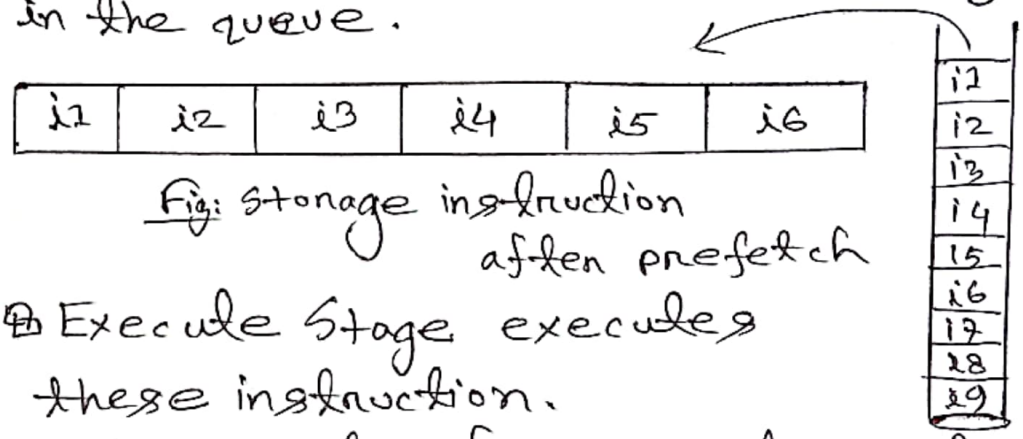

Fig: Storage instruction after prefetch

- Execute Stage executes these instruction.
- It consists of 29,000 transistors.

Memory Segmentation:

- To increase execution speed and fetching speed, 8086 segments the memory.
- It's 20 bit address bus can address 1MB of memory, it segements it into 4 x 64 KB segments.
- 8086 works only with four (4) ~~KB~~ x 64 KB segments within the whole 1MB memory.

The internal architecture of intel 8086 microprocessor is devided into 2 units

01] The Execution Unit (EU)

02] The Bus Interface Unit (BIU)

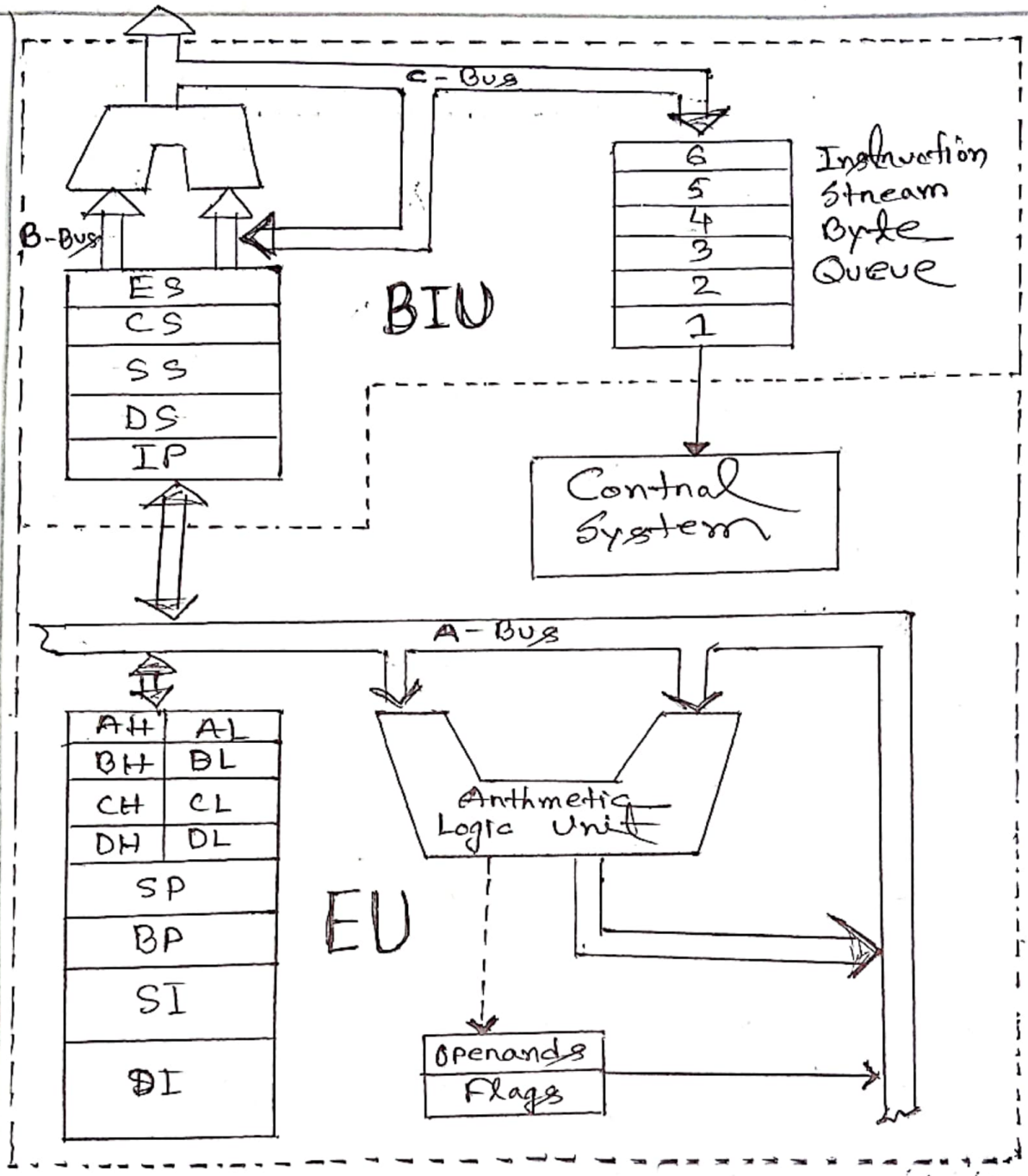

Fig: Internal Architecture of 8086 MP

Execution Unit:

The main components of the EU are General purpose registers, the ALU, special purpose registers Instruction Registers and Instruction Decoder and the flag/status Register.

ⓐ Fetches instructions from the queue in BIU, decodes and executes arithmetic and logical operations using ALU.

ⓑ Sends control signals for internal Data transfer operations within microprocessor.

ⓒ Sends request signals to the BIU to access the external module.

ⓓ It operates with respect to T-States (clock-cycles) and not machine cycles.

8086 has four 16 bit general purpose registers AX, BX, CX and DX. Store intermediate values during execution. Each of these have two 8 bit parts (higher and lower).

- AX register: It holds operands and results during multiplication and division operation. Also an accumulator during string operation.
- BX register: It holds memory address (offset address) in indirect addressing modes.
- CX register: It holds count for instruction like loops, rotate, shift and string operation.
- DX register: It is used AX to hold 32 bit values during multiplication and division.
- ALU (Arithmetic Logic Unit) (16 bit): performs 8 and 16 bit arithmetic and logic operation.

BUS Interface Unit:

It provides the interface of 8086 to external memory and I/O Devices via the System Bus. It performs various machine cycles such as memory read, I/O read etc. to transfer data between memory and I/O devices.

BIU performs the following function-

ⓐ It generates the 20 bit physical address for memory access.

ⓑ It fetches instruction from the memory.

ⓒ It transfers data to and from memory and I/O devices.

ⓓ maintains the 6 byte prefetch instruction queue (supports pipelining).

The BIU mainly contains the 4 segment registers, the instruction pointer, a prefetch queue and an address generation circuit.

- Code Segment register: It holds the base address for code segment. All programs are stored in the code segment and accessed via the IP (instruction pointer).
- Data Segment register: It holds the base address for Data segment.
- Stack Segment register: It holds the base address for stack segment register.

- Extra Segment register: It holds the base address for the extra segment.

Instruction Pointer (IP):

⇒ It is a 16 bit register. It holds the offset of the next instructions in the code segment.

⇒ IP is incremented after every instruction byte is fetched.

⇒ IP gets a new value whenever a branch instruction occurs.

⇒ CS is multiplied by 10H to give 20 bit physical address of the code segment.

⇒ Address of the next instruction is calculated as CS × 10H + IP.

Example:

CS = 4321H IP = 1000H
then CS × 10H = 43210H + offset
= 44210H

- Address Generation Circuit:

⇒ The BIU has a physical address generation circuit.

⇒ It generates the 20 bit physical address using segment and offset address using formula:

Physical Address
= Segment address × 10H + offset address

- 6 byte prefetch Queue:

⇒ It is 6 byte queue (FIFO)

⇒ Fetching the next instruction (by BIU from CS) while executing the current instruction is called pipelining.
⇒ gets flushed whenever a branch instruction occurs.

Discussion: This was our second lab of this semester. Students were introduced with the intel 8086 microprocessor kit. The outcomes of this lab experiment may written as follows -

⇒ The students became familian with the intel 8086 microprocessor.

⇒ The students knew about the internal architecture of intel 8086 microprocessor

⇒ The students were introduced and learnt about the EU and BIU of intel 8086 mp and how its each part works.

Hope this experiment will helps the students to do further experiments of Microprocessor, microcontrollen and embedded system lab, with the mentioned 8086 mp kit.

End.

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