International Islamic University Chittagong

Department of Computer Science and Engineering

B.Sc. in CSE, Final Examination, Autumn 2022

Course Code: **CSE-2323** Course Title: **Digital Logic Design**

Time: 2 hours 30 minutes Full Marks: 50

(i) The figures in the right-hand margin indicate full marks

(ii) Course Outcomes and Bloom's Levels are mentioned in additional Columns

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Group A

[Answer the questions from the followings]

1.	a)	Convert SR to T Flip-flop. Convert JK to SR, T to SR, and D to SR Flip-flop. Define the basic difference between Latch & Flip Flop.	CO2	A	5
		Or,			
1.	a)	Design an asynchronous ripple-down counter.	CO2	A	5
1.	b)	Design a J-K flip-flop and show its truth table, characteristic table, excitation table, and logic diagram.	CO1	U	5
2.	a)	Design a modulo counter by asynchronous counter.	CO2	U	5
2.	b)	Design a 5X32 decoder with four 3x8 decoders and a 2x4 decoder. Use a block diagram.	CO3	A	5
		Or,			
2.	b)	Design a circuit that compares two 3-bit numbers, A and B, to check, if they are equal. The circuit has one output x so that x=1 if A=B, and x=0 if A≠ B. Show the output by providing data into the circuit.	CO3	A	5

Group B

[Answer the questions from the followings]

3.	a)	Design a 2 bits synchronous counter by JK Flip Flop.	CO2	A	5
3.	b)	Implement the output Sum of a Half adder by S-R flip flop.	CO3	N	5
4.	a)	Design a counter using SR flip flops with the repeated following binary sequence: 0, 1, 3,2, 6,4,5,7.	CO2	A	5
4.	b)	Design Johnson's counter.	CO3	N	5
5.	a)	Define ROM.	CO1	U	2
5.	b)	Define Moore's state machine with an example.	CO2	A	8
		Or,			
5.	a)	Define register. Define the functions of the universal shift registrar.	CO1	U	2
5.	b)	A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. How many selection inputs are there in each multiplexer? What sizes of multiplexers are needed? How many multiplexers are there on the bus?	CO2	E	8

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International Islamic University Chittagong

Department of Computer Science and Engineering

B. Sc. in CSE

Semester Final Examination, Spring 2022

Course Code: **CSE 2323** Course Title: **Digital Logic Design**

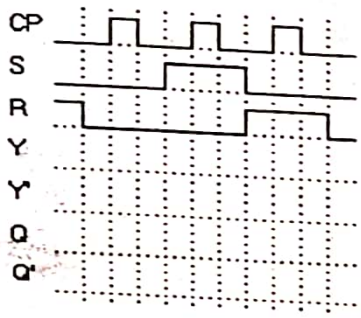
Time: 2 hours 30 minutes Full Marks: 50

The figures in the right-hand margin indicate full marks

Part A

[Answer the questions from the followings]

1.	a)	Design a look-ahead carry generator for a 3-bit full-adder.	CO2	A	5
		Or,			
1.	a)	Design a asynchronous ripple down counter.	CO2	A	5
1.	b)	Design a J-K flip-flop and show its characteristic equation, characteristic table, and logic diagram.	CO1	U	5
2.	a)	Enter the expected timing diagram for the signals Y, Y', Q, and Q' for a master slave S-R flip flop.	CO2	U	5



2.	b)	Design a 5X32 decoder with four 3x8 decoder and a 2x4 decoder. Use a block diagram.	CO3	A	5
		Or,			
2.	b)	Design a circuit that compares two 3 bit numbers, A and B, to check, if they are equal. The circuit has one output x, so that x=1 if A=B, and x=0 if A≠ B. Show the output by providing data into the circuit.	CO3	A	5

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Part B

[Answer the questions from the followings]

3.	a)	Design a sequential circuit with JK flip-flops to satisfy the following state equations: A(t+1)=A'B'CD+A'B'C+ACD+AC'D' B(t+1)=A'C+CD'+A'BC' C(t+1)=B D(t+1)=D'	CO2	A	5
3.	b)	Design a 2 bits synchronous counter by JK Flip Flop.	CO2	A	5
4.	a)	Design a counter using SR flip-flops with the repeated following binary sequence: 0, 1, 3,2, 6,4,5,7.	CO2	A	5
4.	b)	Design Johnson's counter	CO3	N	5
5.	a)	Define ROM.	CO1	U	2
5.	b)	Implement the functions $F(w,x,y,z)= \sum(0,1,3,4,8,9,15)$ with ROM.	CO2	A	8
		Or,			
5.	a)	Define register. Define the functions of universal shift registrar.	CO1	U	3
5.	b)	A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. How many selection inputs are there in each multiplexer? What size of multiplexers are needed? How many multiplexers are there in the bus?	CO2	E	7

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International Islamic University Chittagong

Department of Computer Science and Engineering

Final Examination, Autumn 2019

Course Code: CSE 2305 **Course Title: Digital Logic Design**

Total Marks: 50 **Time: 2 hours 30 minutes**

[Answer any *two* set of questions from **Group-A** and any *three* set of questions from **Group-B**; Separate answer script must be used for Group-A and Group-B.]

Group-A

a) A BCD adder can be constructed with two binary adders, one OR gate and two AND gates. Justify the statement with a necessary figure and example. 5

b) Briefly describe the function of a multiplexer with a real-life example. 5

a) Construct a 4-to16 decoder by joining 2-to-4 decoders with enable input. 5

b) Implement the following function with a multiplexer: 5
$F(A,B,C,D)=\sum(0,1,3,4,8,9,15)$

a) Implement a full adder with a decoder and OR gates. The adder inputs are A, B, and C. The adder produces outputs S and C. 5

b) A sequential circuit has two *JK* flip-flops A and B, two inputs x and y, and one output z .The flip-flop input equations and circuit output equation are 5

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$
$$J_B = A'x \qquad K_B = A + xy'$$
$$z = Ax'y' + Bx'y'$$

i. Derive the state equations for A and B.

ii. Tabulate the state table.

iii. Draw the state diagram.

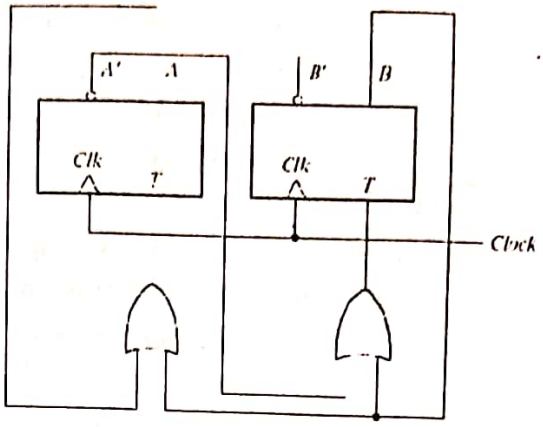
Group-B

a) How can you serially transfer data from one register to another register? Briefly describe with a necessary example. 4

b) Write the basic differences between a register and a counter. 2

c) What is a memory cell? Design a 4 × 4 RAM and describe its operation. 4

5. a) Derive the state table, state diagram and state equations of the following sequen diagram.



b) Design a *3-bit* down counter with *T* flip-flop. 5

6. a) Design a *bidirectional* shift register and explain its operation. 5

b) Suppose there are 4-bit four data registers A, B, C and D. Design a circuit to copy 4-bit data from any of the registers to other register. Show the block diagram and explain its operation for copying the data from register A to D. 5

7. a) Design a combinational circuit using a ROM. The circuit accepts a four-bit number and outputs a binary number equal to the square of the input number. 6

b) What are the steps to draw a PLA programming table? 2

c) Differentiate between the PROM, PAL and PLA. 2

International Islamic University Chittagong

Dept. of Computer Science & Engineering (CSE)

B.Sc. in CSE, Semester Final Examination, Spring 2018

Course Code: CSE 2305 **Title:** Digital Logic Design

Total Marks: 50 Time: 2 hours 30 Minutes

Group - A

1. a. Define parallel adder. Design a 4-bit parallel adder with the solution of carry propagation problem. **5**

   b. A combinational circuit is defined by the following three Boolean functions: **5**

$$F_1 = (X+Y)' + XYZ$$
$$F_2 = (X+Z)' + X'YZ$$
$$F_1 = XY'Z + (X+Z)'$$

   Design the circuit with a decoder and external OR gates.

2. a. i. Design a 16-to-1 multiplexer using 4-to-1 multiplexers only. **5**

   ii. Using two 2-to-4 decoders, design a logic circuit to realize the following Boolean function

   F(A,B,C) = Σ(0, 1, 4, 6, 7).

   b. Design a combinational circuit that compare two 4-bit numbers A and B to check if they are equal. The circuit has one output x, so that x=1 if A=B and x=0 if A is not equal to B. **5**

3. a. How does *JK* flip-flop remove the indeterminate states of *S-R* flip-flop? Design a *JK* flip-flop and show its characteristic equation, characteristic table, logic diagram and timing diagram. **5**

   b. What is flip-flop triggering problem? Describe the master-slave JK flip-flop with timing diagram. **5**

Group-B

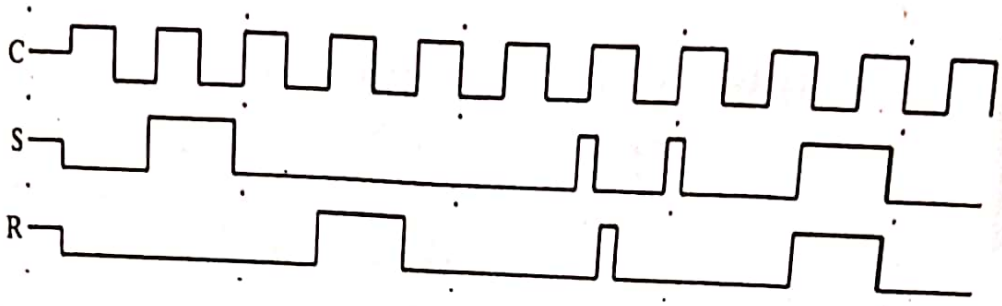
4. a. Consider a 128x8 ROM. How many address and words are consisted in this ROM. Specify the each word size in bit. Design a ROM with AND-OR-INVERT gates with the following function: **5**

$$F(X, Y) = \sum(2, 4, 5)$$
$$F(X, Y) = \sum(1, 5, 7)$$

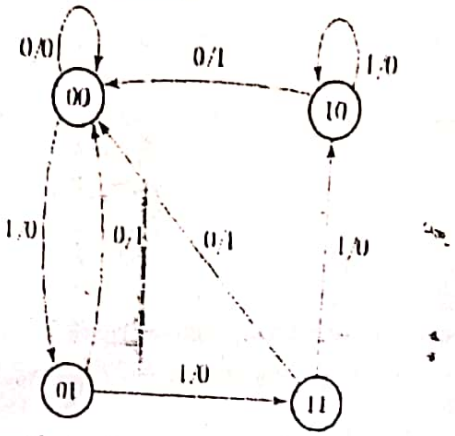
   b. If the present (ABC) state is 110, and the input X=0; what will be the next state if the flip flops input functions are as follows: **5**

$JA = B'X$	$KA = 1$
$JB = A + C'X'$	$KB = XC' + CX'$
$JC = AX + A'B'X'$	$KC = X$

5. a. Describe the behavior of master-slave flip-flop with respect to the following timing diagrams. **5**



b. Define the state diagram and state equation. 5



From the above state diagram derived the

i. State table
ii. Excitation table
iii. State equations

6. a. Design a 4-bit asynchronous counter with *JK* flip-flops and explain its operation with timing diagram 5

b. Design a *3-bit* Up-Down counter with *T* flip-flop. 5

7. a. Define register. Draw the memory logic diagram. Construct a RAM for 4 word of 5 bit each. 5

b. Design a sequential circuit described by the following state equations using JK flip-flops. 5

$$A(t+1) = xAB + yA'C + xy$$
$$B(t+1) = xAC + y'BC'$$
$$C(t+1) = x'B + yAB'$$

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International Islamic University Chittagong

Dept. of Computer Science & Engineering (CSE)

B.Sc. in CSE, Semester **Final Examination, Autumn 2017**

Course Code: CSE 2305 **Title:**Digital Logic Design

Total Marks: 50 Time: 2 hours 30 Minutes

Group – A

Answer any two set of Questions

1. a. Define parallel adder. Design a combinational circuit for 1-bit binary numbers A=A0 and B=B0. The outputs are F, G, and H, where F is 1 if A>B, G is 1 if A=B, and H is 1 if A<B. 5

   b. What is the carry propagation problem of *parallel* Adder? What could be the solution of carry propagation problem of *parallel* adder? 5

2. a. What are the basic differences between sequential and combinational logic? How PLA recover the limitations of ROM? Compare the total link of the PLA with respect to ROM. 5

   b. What is flip-flop :riggering problem? Describe the master-slave JK flip-flop with timing diagram. 5

3. a. Define de-multiplexer. Design a multiplexer using the following function: 5
   $F(A, B, C, D) = \sum(0, 3, 5, 6, 8, 10, 12, 13, 14)$
   Where, A, B and D are selection line.

   b. A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations: 5

$$D_A = x'A + XY$$
$$D_B = x'B + XA$$
$$Z = XB$$

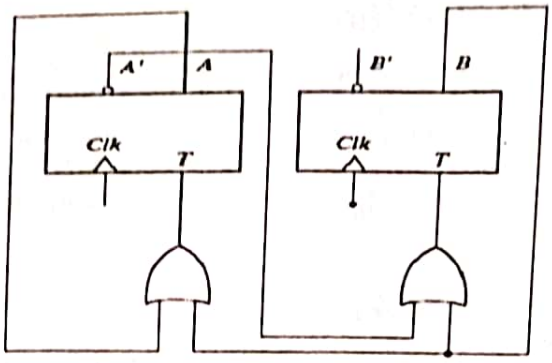
   (i)Draw the logic diagram of the circuit.
   (ii)Derive the state table.
   (iii)Derive the state diagram.

Group-B

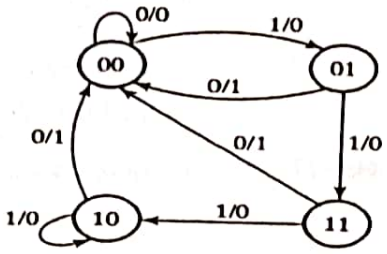
Answer any three set of Questions

a. Design a 4-bit register. How many flip-flop values are complemented in an 8-bit binary ripple counter to reach the next count value after: 5
(i)11111111? (ii)01100011?

b. Derive the state table, state diagram and state equations of the following sequential diagram. 5



5. a. Define the state table and state equation. 5



From the above state diagram derived the

i. State table
ii. Excitation table
iii State equations

b. Design a 4-bit asynchronous counter with *JK* flip-flops and explain its operation with timing diagram. 5

6. a. Write down the advantages of PLA over ROM. Implement the following functions using PLA. 5

F1(A,B,C)= Σ(3,5,6,7)
F2(A,B,C)= Σ(0,2,4,7)

b. What is a memory cell? Design a 4x4 RAM and describe its operation with example 5

7. a. Show the basic difference between binary and BCD ripple counter with truth table? Draw the logic diagram of the BCD counter with a count enable input. 5

b. Design a sequential circuit with two *D* flip-flops *A* and *B* and one input *X*.When *X*=0, the state of the circuit remains the same. When *X*=1, thecircuit goes through the state transitions from 00 to 10 to 11 to 01, back to00, and then repeats. 5

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